1 Application

Blue-Angel-compliant PFC-controlled switch-mode power supplies up to 150 watts.

2 Features

- PulseTrain™ regulation allows voltage, current and PFC to be controlled independently
- Primary-only feedback eliminates optoisolators and simplifies design
- No loop compensation components required
- ±1% regulation over a 100:1 load variation
- Built-in soft-start
- Adaptive pulseTrain regulation keeps the bulk capacitor voltage below 400V
- Operates in critical discontinuous conduction mode (CDCM)
- Low start-up and supply current
- Reduced EMI noise
- SO-8 package

3 Benefits

- Ideal for single-stage, single-switch power factor correction (PFC)
- Enables 97% power factor correction resulting in EN6100-3-2 compliance
- SmartSkip mode provides low standby dissipation of the power supply enabling Blue Angel Compliance
- Efficiency greater than 85% across line and load variation
- Universal input (85-270V, 50-60 Hz)
- Low parts count
- Reduced design time due to the elimination of loop compensation design

4 Description

The iW2202 is a digital switching mode power supply controller for PFC applications. Its is typically used with the PFC-corrected BIFRED *(Boost Integrated with Flyback Rectifier/Energy storage DC/DC*) topology, shown in Figure 1. The BIFRED topology is a single-stage, single-switch topology that combines a boost converter with an isolated flyback converter, achieving power-factor correction with a low parts count.

An iW2202-based power supply looks like a resistor to the AC line. Unlike attempts to control the BIFRED topology with analog controllers, the all-digital iW2202 provides a near-unity power factor without placing high voltage stresses on the bulk capacitor.

The iW2202 uses a proprietary new digital control technology called pulseTrain™ to achieve efficiencies in excess of 85% across a wide load range, and across the universal input range of 85-270VAC, 50-60 Hz.

Internally, the iW2202 uses *real-time waveform analysis* to determine crucial circuit parameters. The reflected secondary voltage of the flyback transformer is sensed at precisely calculated times to determine the secondary voltage, the transformer reset time, and the ideal zero-voltage switching point Measurements are performed during the OFF time of every cycle, and the results determine what is done on the next cycle. The dynamic response time of the circuit is less than half a cycle.

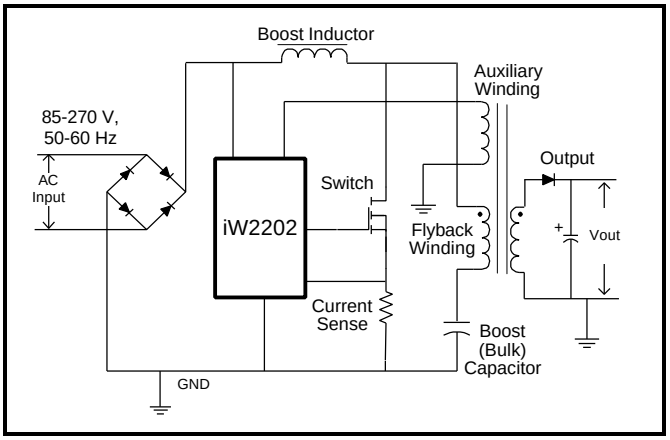
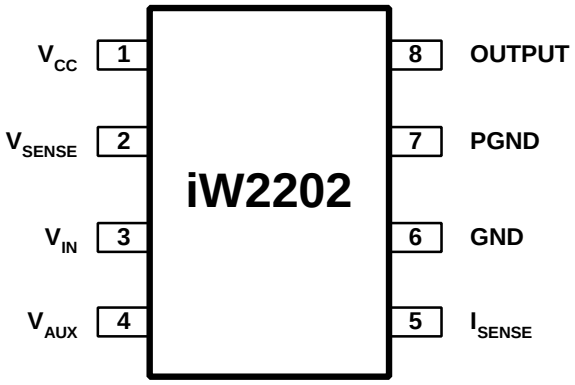


Figure 1. iW2202 system concept

5 Pin Description



Pin #	Name	Type	Pin Description
1	V_{CC}	Power Input	Power supply for control logic and voltage sense for power-on reset circuitry
2	V_{SENSE}	Analog Input	Secondary voltage sense (when used with optional secondary opto-isolator feedback). Tied to V_{AUX} in normal configuration
3	V_{IN}	Analog Input	Line voltage sense. Used to monitor rectified line voltage for PFC control
4	V_{AUX}	Analog Input	Feedback voltage from auxilary winding. Used to monitor output voltage waveform
5	I_{SENSE}	Analog Input	Primary current sense. Used for cycle-by-cycle peak-current control
6	GND	Signal Ground	Analog/digital ground
7	PGND	Power Ground	Power ground
8	OUTPUT	Digital Output	Gate driver for external MOSFET switch.

6 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Supply voltage	0	15	V
Input voltage on V_{SENSE}, V_{IN}, V_{AUX}, I_{SENSE}	-0.3	6.3	V
Power dissipation at $T_A \leq 25°$ C		800	mW
Storage temperature (T_{STG})	-65	150	°C
Lead temperature, while soldering for ≤ 10 seconds		300	°C

7 Electrical Characteristics

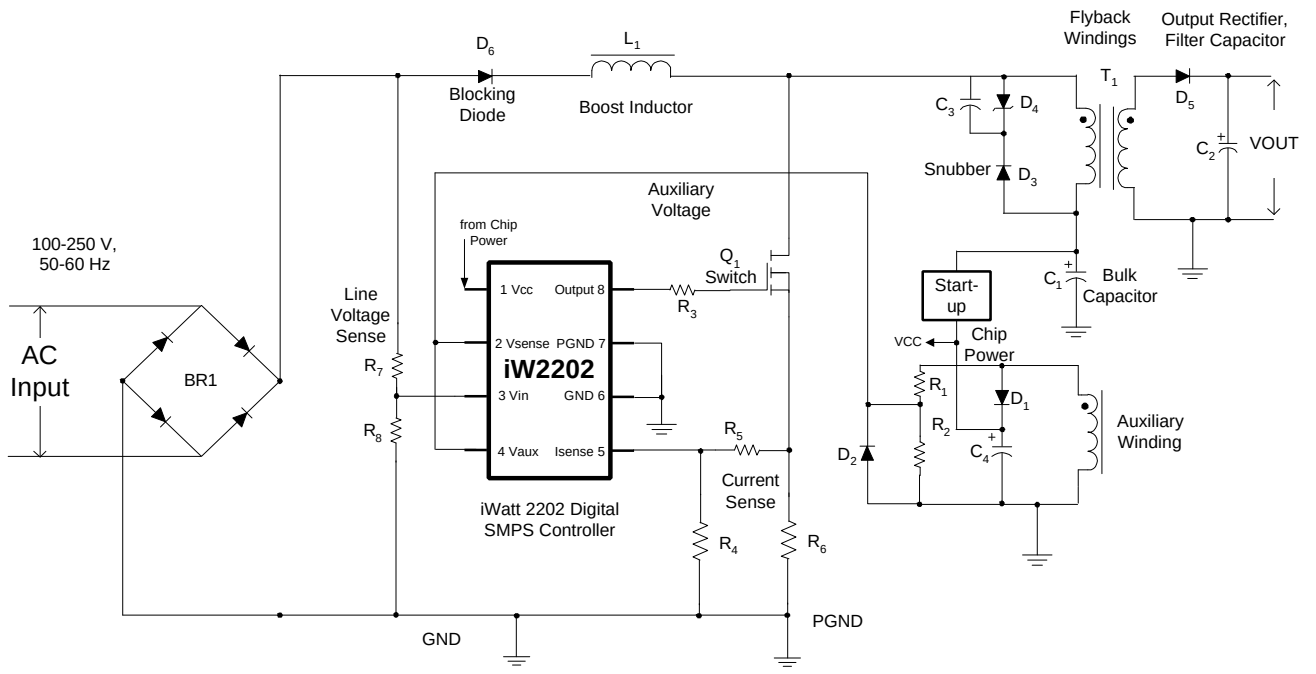
Unless otherwise specified, these specifications apply for V_{CC} = 12V, $T_A \leq 70$ °C. (See Note 1.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
FEEDBACK / AUXILIARY / PFC SECTION (Pins 2, 3, and 4)						
V_{IR}	Input voltage range		0		5	V
I_{IR}	Input current range			0.1	1	µA
V_{REF}	Internal voltage reference (Note 2)		1.182	1.2	1.218	V
ISENSE SECTION (Pin 5)						
	I_{SENSE} buffer gain		4.75	5	5.25	V/V
	Input voltage		0		5	V
	Input current			0.1	2	µA
V_{SD}	Output shutdown voltage (Note 3)		1.5		5	V
OUTPUT SECTION (Pin 8)						
V_{OL}	Output low level	I_{SINK} = 200mA		0.5	1	V
		I_{SINK} = 20mA		0.2	0.4	V
V_{OH}	Output high level	I_{SOURCE} = 200mA	10	11		V
		I_{SOURCE} = 20mA	10	11		V
t_R	Rise time (Note 4)	T_A = 25 °C, C_L = 1500pF		30	50	nS
t_F	Fall time (Note 4)	T_A = 25 °C, C_L = 1500pF		30	50	nS
t_{ON_MAX}	Maximum switch ON time (Note 5)		5.1	6	6.9	µS
START-UP SECTION (Pin 1)						
V_{SU}	Start-up threshold (Note 1)		13.5	14	14.5	V
	Min operating voltage after turn-on		9.5	10	10.5	V
SUPPLY VOLTAGE SECTION (Pin 1)						
I_{SU}	Start-up current	V_{CC} = 13V		0.5	1	mA
I_{CC}	Supply current (operating)	$10 \leq V_{CC} \leq 13.2$		12		mA
V_{UVP}	Under-voltage protection		7	7.8	8.6	V
V_{OVP}	Over-voltage protection		V_{SU}+1.0			V

Notes:

1. VCC must be brought aboe the start-up threshold before setting to its operating value (nominally 12V).
2. V_{REF} is the internal voltage reference. It is not brought out to a pin.
3. When the voltage on the ISENSE pin exceeds V_{SD}, all gate pulses are suppressed.
4. Not tested, but guaranteed by design.
5. The switch will be turned off after this amount of ON time if I_{PEAK} has not been reached, placing a lower limit on switching frequency.

8 Application Example



Item	Description
Q1	MOSFET switch.
L1, C1, D6	Boost converter section of the BIFRED boost/flyback system. The capacitor C1 provides the energy for the flyback transformer. See sections 11.4 and 12.7.
T1	The flyback winding provides power to the load. The reflected voltage on the auxiliary winding is used by the real-time waveform analysis circuit. The auxiliary winding also provides power for the iW2202.
D1, C4, Startup	Chip power supply.
R1, R2	Voltage divider to scale the auxiliary voltage to the appropriate value. Clamping diode D2 minimizes negative voltage on the Vaux pin. See section 12.6.
R7, R8	Voltage divider for the line voltage sense circuit. Fixed values: R7= 500K, R8=1K.
R4, R5, R6	Current sense circuit. Resistor values set the peak current. See section 12.3.1.

Figure 2. iW2202 -based power supply with single-stage, single-switch active PFC

9 Block Diagram

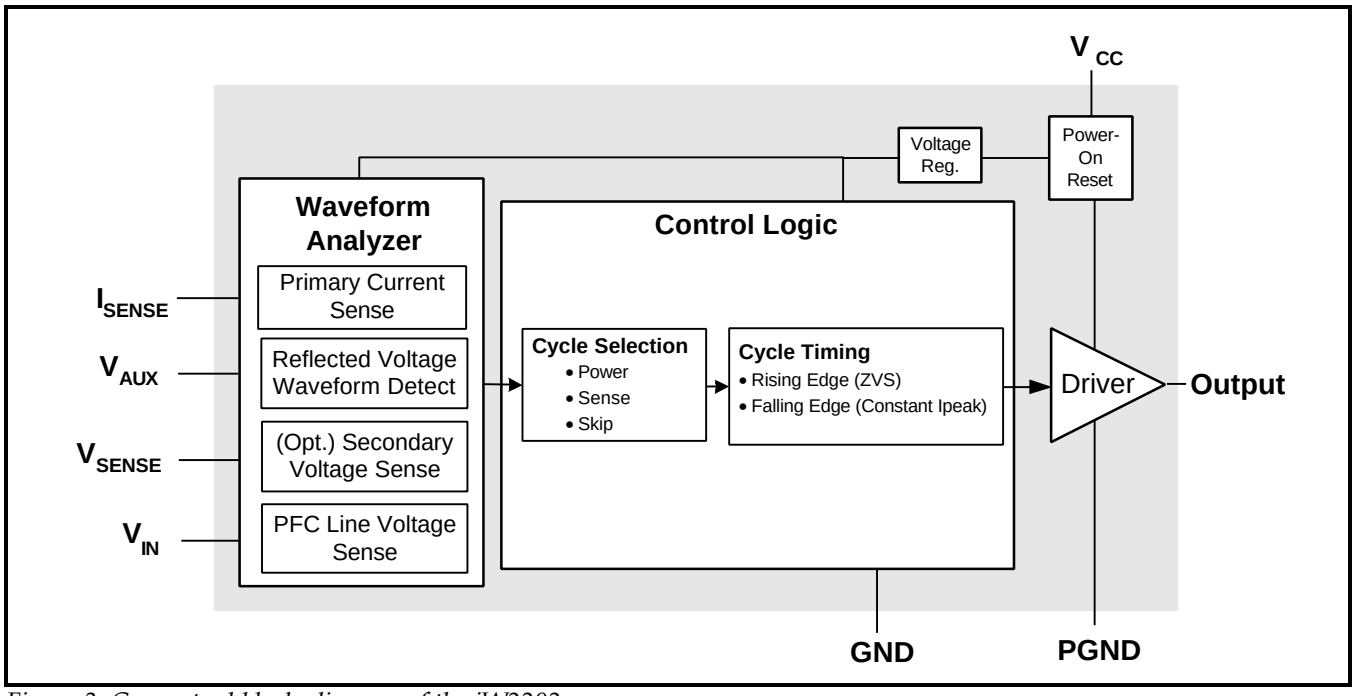


Figure 3. Conceptual block diagram of the iW2202

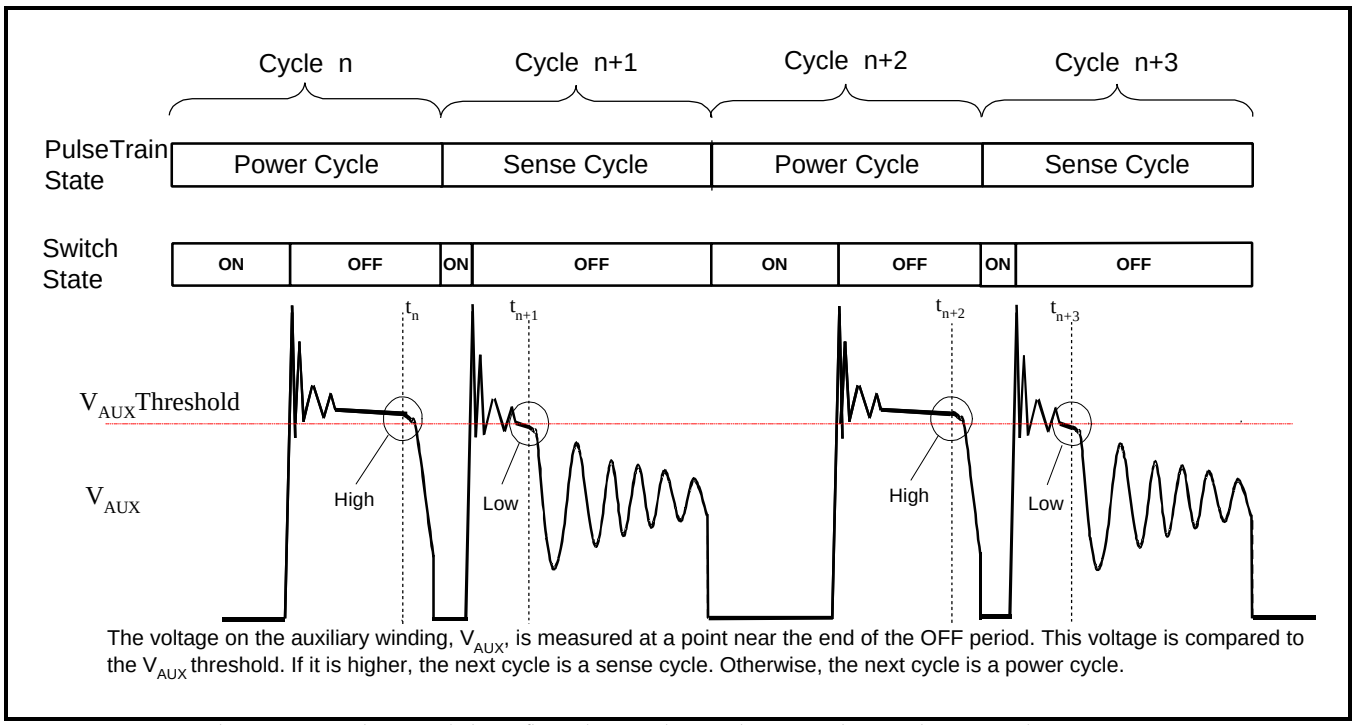


Figure 4. Power pulses, sense pulses, and the reflected secondary voltage on the auxiliary winding

10 PulseTrain Regulation

Rather than using pulse-width or pulse frequency modulation to achieve output voltage regulation, pulseTrain controls output voltage through the presence or absence of power pulses. If the output voltage is below the desired level, power pulses are emitted continuously until the desired level is reached. If the output voltage is higher than the desired level, *sense pulses* are sent instead of power pulses. A sense pulse has a much shorter ON time than a power pulse, and transfers much less energy. See Figure 4.

A sense cycle has the same period as the preceding power cycle, but the ON time is set to one-fourth that of the power cycle. Since primary current ramps linearly with ON time, the peak current of a sense pulse is also only one-fourth that of a power pulse. Thus, a sense cycle only transfers one-sixteenth as much energy as a power cycle.

Under most load conditions, regulation is achieved through a mix of power cycles and sense cycles. Under extremely low-load conditions, no power pulses are sent. Instead, sense cycles alternate with *skip cycles*.

It is important to recognize that pulseTrain does not depend on the precise width of the pulses to maintain regulation. If the output voltage is lower than the desired level, the next cycle will contain a power pulse. If the output voltage is above the desired limit, the next cycle will contain a sense pulse. The pulseTrain controller will optimize the ratio of power pulses to sense pulses to keep the output voltage constant. The frequency and duty cycle of the pulses can change, but this does not affect voltage regulation.

This situation is very different from the situation with analog technologies, such as PWM/PFM-based controllers, which are forced to attempt to meet all their goals through the adjustment of pulse geometry, which forces unwanted trade-offs.

As will be shown in the next section, pulseTrain modulation takes full advantage of its ability to pursue multiple simultaneous goals, combining the flexibility of pulseTrain regulation with the precision of real-time waveform analysis, resulting in ultra-fast dynamic response and simplified circuit design.

11 Real-Time Waveform Analysis

Figure 5 shows the effect of a sense pulse on the transformer's primary winding, measured at Vdrain. As you can see, this waveform contains quite a bit of ringing. This ringing is highly organized, consistent from cycle to cycle, and its onset pinpoints important events in the cycle.

In a flyback system, the reflected voltage seen during the switch's OFF time reveals the secondary voltage, plus additional circuit information, including leakage inductance, transformer reset time, resonant frequency, and secondary diode characteristics. All this information is easily read on an auxiliary winding. This information renders secondary feedback unnecessary.

The choice between reading the reflected voltage on the primary winding or on an auxiliary winding is somewhat arbitrary. If taken from the primary, the voltage centers around Vin (the instantaneous line voltage). If taken from an auxiliary winding, the voltage centers around zero. The auxiliary winding can also provide power for the device.

Real-time waveform analysis uses the information in the reflected voltage to extract secondary voltage and transformer reset time. These voltage measurements are made on *every cycle*, and each cycle's measurement determines the next cycle's pulse type.

Traditional voltage regulators use space-average sensing, averaging the voltage over multiple cycles. This causes the loss of a great deal of information and introduces delays, slowing the response of the controller and raising the issue of loop instability. Real-time waveform analysis, on the other hand, does not perform averaging, but determines the next cycle's switching decisions from the current cycle alone. The time delay between measurement and correction (dynamic response) is thus extremely short, being less than the OFF time of a single cycle. The system is inherently stable. There is no need for loop compensation.

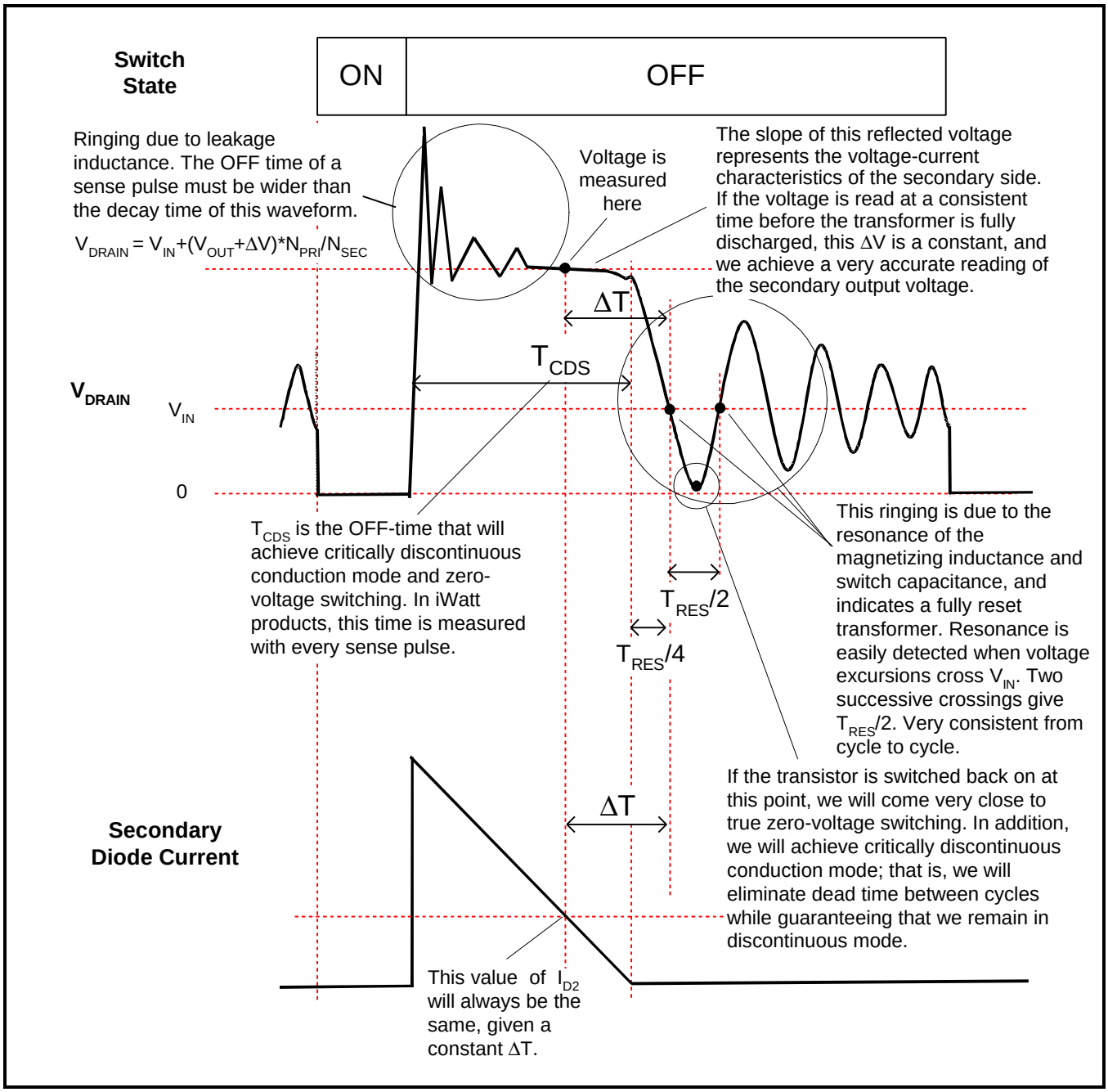


Figure 5. Information available to waveform analysis

11.1 Zero-Voltage Switching

PulseTrain achieves zero-voltage switching (ZVS) by using the resonance (ringing) that occurs in discontinuous-mode flyback circuits. This resonance occurs after the secondary current falls to zero, indicating the transition from power transfer to open-circuit conditions.

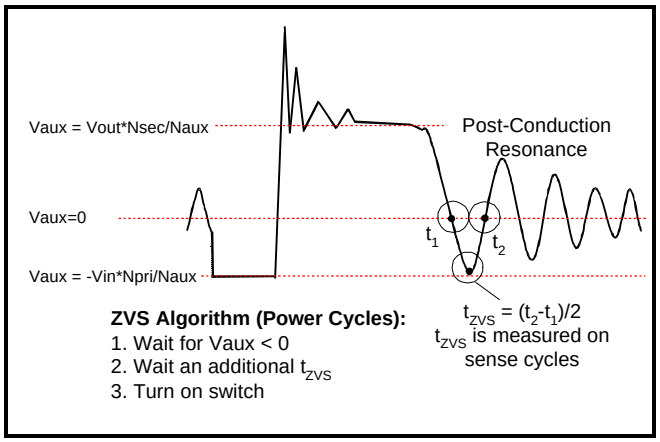


Figure 6. Auxiliary voltage and zero-voltage switching

As shown in Figure 5, post-conduction resonance is a damped oscillation that falls very close to zero volts on its first cycle. Zero-voltage switching can be achieved very easily, simply by measuring the resonant period on a sense cycle, and switching the output transistor when the voltage is closest to zero on subsequent power cycles.

The algorithm for ZVS is shown in Figure 6. On each power cycle, pulseTrain waits for the primary voltage to drop below V_{IN}, (on the auxiliary winding, this occurs when the voltage goes negative). This indicates that we are in the post-conduction resonance. After this event, the controller waits an additional ΔT that will take us to the minimum voltage, then turns on the switch for the next power or sense cycle. The time between the zero-crossing on the auxiliary winding and the minimum primary voltage is estimated as being one-half the time between the negative-going zero crossing and the positive-going zero-crossing, as shown in Figure 6. Given the geometry of the resonant signal, this estimate is extremely accurate.

By achieving zero-voltage switching, we also achieve *critically discontinuous conduction mode,* because we have turned the transistor back on immediately after the transformer's magnetic field has reset. This eliminates dead time between cycles, fully utilizing the output transformer. As a result, the transformer operates at lower flux levels than traditional technologies, resulting in lower core losses and thus higher efficiencies.

Because the waveform is being monitored in real time, critically discontinuous conduction mode is maintained across all variations in line and load conditions. In addition, this method of extracting maximum performance from the inductor is insensitive to component variations, since the circuit behavior is measured, not assumed.

11.2 Primary-Only Feedback

PulseTrain uses primary-only feedback, measuring the secondary voltage by analyzing its reflected voltage as seen by an auxiliary winding. This reflection reveals what is happening at the transformer secondary. However, the voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, the ΔV will also be small.

As shown in Figure 5, secondary current has a linear ramp down to zero. Zero secondary current is signaled (on the reflected voltage waveform) by the beginning of post-conduction resonance. Using resonance as a marker, is a simple matter to calculate a fixed ΔT that will pinpoint a time where secondary diode current is still flowing, but is very small. The exact value of ΔT is not crucial, so long as it places the measurement at a point where current is still nonzero. ΔT is recalculated on sense cycles.

Measuring voltage on sense cycles uses the same ΔT as on power cycles. Because the slope of the secondary current ramp is independent of ON time, the current at a fixed ΔT is the same, regardless of whether the cycle is a sense cycle or a power cycle.

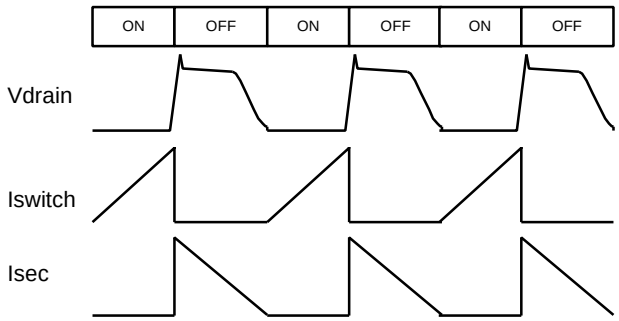
11.3 Constant Peak Current

Like the decision to turn the transistor on, the decision to turn the transistor off is controlled by real-time waveform analysis -- this time in the current domain. The maximum desirable primary current, Ipeak, is set with external resistors.

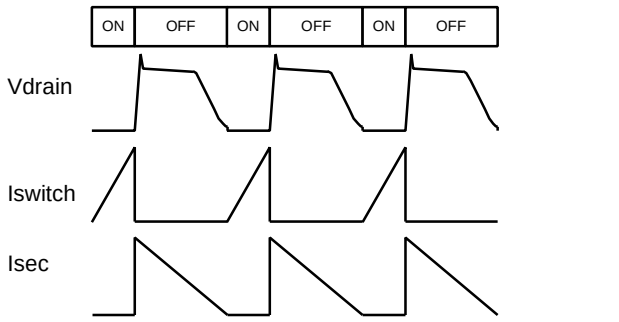
On every power cycle, the power transistor is kept on until the primary current ramps up to Ipeak. When this level is reached, the transistor is turned

off. Thus, the point at which the transistor is turned off is controlled by the current waveform, while the point at which it is turned on is controlled by the voltage waveform.

If the line voltage is very high, the current will ramp up quickly, and the ON time of the switch will be short. If the line voltage is very low, the current will ramp slowly, and the ON time will be long.



Low line voltage results in longer ON times before peak current is reached, resulting in long cycle times (and relatively low switching frequencies). Critically discontinuous mode is maintained.



High line voltage results in shorter ON times, because peak current is reached more quickly. Short ON times lead to short cycle times (high switching frequency). Critically discontinuous mode is maintained.

Figure 7. Constant peak current switching

Because of this, the output frequency of the pulseTrain regulator varies to accommodate changing line voltage.

The dynamic response to changing load conditions is very fast. The time between measurement and action is only a fraction of a power cycle. The voltage measurement comes during the switch OFF time of every cycle, and controls the ON time switching decision for the very next cycle. PulseTrain therefore reacts almost instantaneously to changes in load and line conditions.

The mechanism of real-time waveform analysis provides inherent stability without the need for loop compensation. The expense of loop compensation components and the design time they represent are eliminated.

11.4 Power Factor Correction

One very welcome result of the pulseTrain methodology is that topologies that have proven problematical with PWM/PFM controllers work smoothly with pulseTrain.

For example, the iW2202 is ideal for use in the inherently PFC-corrected *BIFRED (Boost Integrated with Flyback Rectifier/Energy Storage/DC-DC)* topology. The basic BIFRED topology uses a discontinuous mode boost converter to achieve PFC. The capacitor of the boost converter is used as a bulk capacitor to drive a flyback converter. BIFRED uses a single switch. See Figure 8.

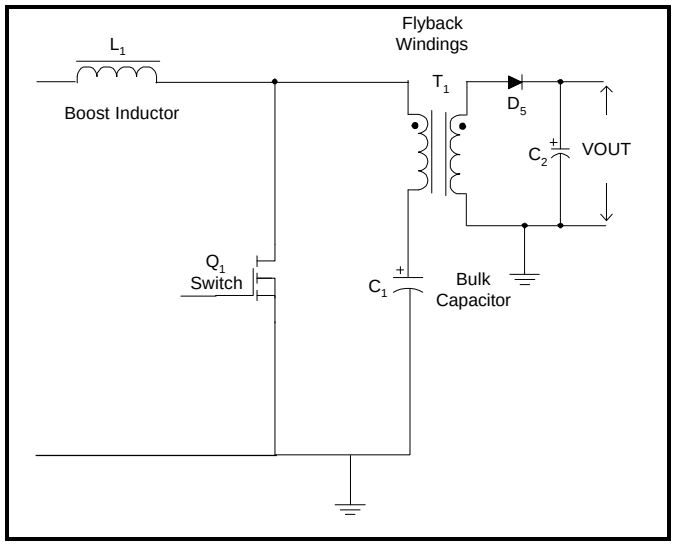


Figure 8. BIFRED circuit

The circuit operates as follows:

Switch on: Energy derived from the AC line is stored in the boost inductor. At the same time, energy derived from the bulk capacitor is stored in the primary of the flyback transformer.

Switch off: The energy in the flyback primary is transferred to the output. At the same time, the energy in the boost inductor is delivered to the bulk capacitor, charging it.

If the two inductors store the same amount of energy, on average, over the course of a half-cycle of the AC input, the voltage of the bulk capacitor will remain constant. The iW2202 achieves this goal, avoiding the problem of high voltage stresses on the bulk capacitor. With traditional controllers (such as modified PFM), the bulk capacitor voltages tend to

become very high under some line and load conditions. With the iW2202, the voltages remain under 400V at all times, allowing standard capacitors to be used. This is a direct benefit of using pulseTrain technology.

Both the boost stage and the flyback stage operate in discontinuous mode. This means that both inductors are fully reset once per switching cycle. The energy stored in the boost inductor is completely transferred to the bulk capacitor, and the energy stored in the flyback transformer is completely transferred to the load.

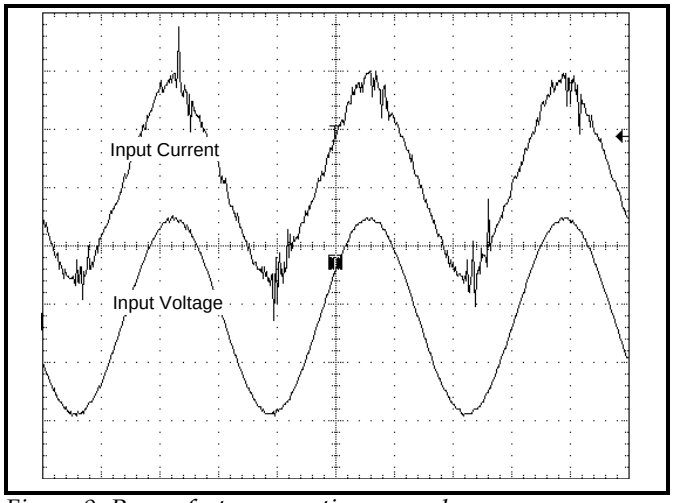


Figure 9. Power factor correction example

11.5 SmartSkip Mode

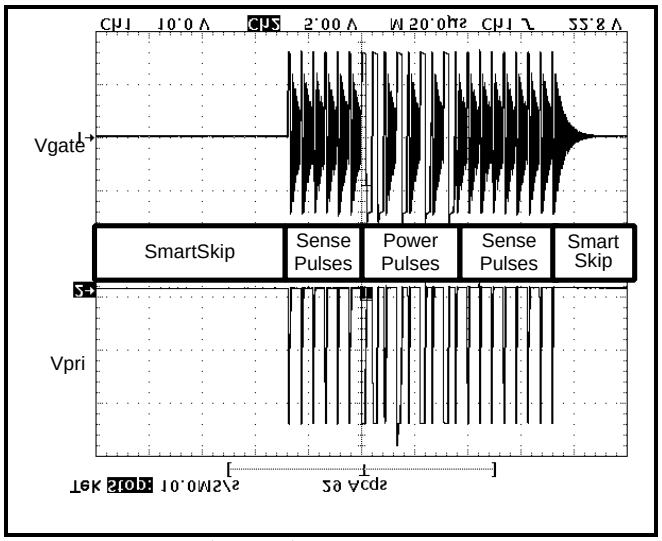


Figure 10. SmartSkip mode

As has already been mentioned, a sense pulse delivers one-sixteenth as much energy as a power pulse. A continuous stream of sense pulses thus delivers 6.25% of full load. If the load is lighter than this, the device enters *SmartSkip mode,* when the circuit alternates between sense pulses and no pulses at all.

Regulation is still maintained, since each sense pulse returns a precise measurement of output voltage. SmartSkip mode is entered automatically when the sense pulses reveal that the output voltage is remaining above the desired level, though no power pulses have been sent recently.

The depth of the SmartSkip mode (the ratio of skipped cycles to sense pulses) is increased or decreased, according to voltage and the current skip-mode depth. The depth of the SmartSkip mode is reduced automatically as the load increases.

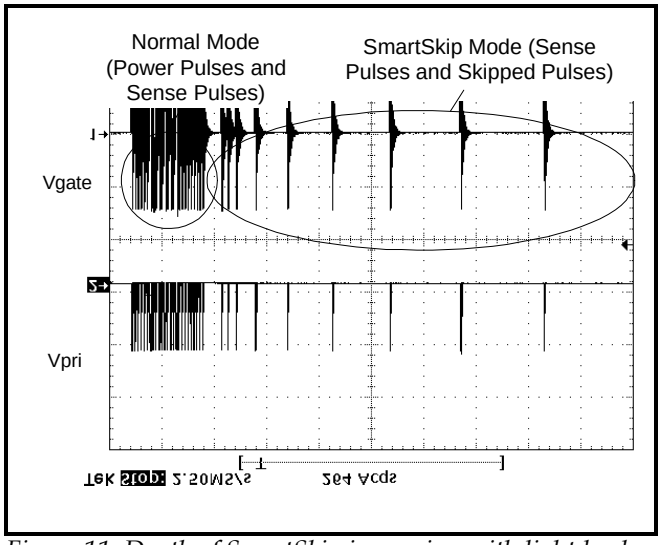


Figure 11. Depth of SmartSkip increasing with light load

11.6 Soft-Start and Protection

In pulseTrain, all output switching occurs as the result of the pulseTrain logic. If the logic is not up and running, the output switch is always off. Valid waveform analysis is available by the second power pulse. This reduces the problem of soft-start merely to the requirement that there be a reliable power-on reset mechanism.

Figure 12 shows what happens on the output at start-up. The first power pulse shows a clean current ramp, but the drain voltage reflects the fact that the transformer does not reset by the time the second pulse arrives, and thus is operating in continuous mode. This is also shown in the current on the second pulse, which starts at a non-zero value. However, pulseTrain's automatic peak current limiting causes the second power pulse to be much shorter than the first one. By the third cycle, the initial current has already fallen significantly, due to

the second cycle's shorter ON time. This trend will continue until, in a few cycles, the initial current is zero and the transformer is operating in critically discontinuous mode.

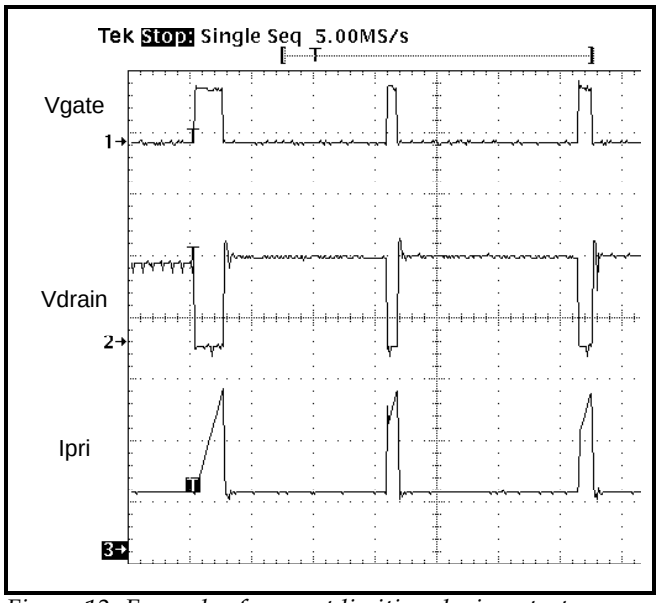


Figure 12. Example of current limiting during start-up

The nominal VCC voltage of the device is 12 volts. It requires a start-up voltage that reaches 14 momentarily, initiating a start-up sequence internally. The device protects itself from over-voltage by shutting itself down if VCC exceeds 15 volts. Its under-voltage lockout circuit will cause it to shut itself down if the voltage drops below 7.8 volts, and will remain shut down until the start-up voltage is seen again. Both over- and under-voltage shutdowns inhibit switching on the OUTPUT pin.

These mechanisms protect the device, while protecting the rest of the circuit indirectly.

Additional protection can be achieved with external sensors that shut down the iW2202 on a circuit fault. The best way of shutting down the iW2202 is to pull the Isense pin above 1.5V. This will inhibit output pulses.

12 Designing iW2202 -Based Power Supplies

The schematic in Figure 2 shows a typical iW2202 system. Choosing component values is a straightforward process, as shown in the example below.

12.1 Description

For this example, we are designing an 70W, 19V laptop computer power supply. It is a universal input supply supporting input line voltages of 85-265 VRMS, and operating in discontinuous flyback mode. To keep component costs low, we wish to use a switch with a maximum Vdrain of no more than 600V.

12.2 Primary Turns Ratio

The voltage across a flyback switch includes the input voltage plus the reflected secondary voltage:

Vd = Vin + N*Vout.

The turns ratio between the primary and secondary, N, is constrained by our desire to avoid stressing the switch. We use the maximum safe value of Vd and the highest input voltage for our worst-case calculation:

Vd_max = Vline_max + N*Vsec

N = (Vd_max – Vline_max)/Vsec

12.2.1 Example

If we use a 600V switch and derate it by 100V as a safety margin, we are left with 500V as our maximum drain voltage, Vd_max.

N = (500V-380V)/19.7V = 6.09 ≈ 6.

12.3 Ipeak Selection

We next need to calculate the peak current value we need to support worst-case operation. The constant peak current circuitry will keep the output switch on until this value is reached on every power cycle.

Iin is the average input current to the converter:

Iin = Po/(Vin*η)

Where η is the efficiency of the converter. Vsec is the secondary voltage. It differs from the output voltage,

Vout, by a fixed ΔV, where ΔV is the secondary diode drop. We will use 0.7V for ΔV, and thus a Vsec of 19.7V in our example.

The maximum input current we must support occurs at minimum supported line voltage:

Iin = Po/(Vin_min* η)

Vin_min = Vline_min*1.4142

Vline_min is the lowest supported RMS line voltage.

Full-load efficiency can be taken as a (slightly conservative) 0.80 for design purposes.

We need to convert the average input current Iin into a peak input current Ipeak. This depends on the duty cycle, D, of the switch and the shape of the primary current waveform (a triangle wave with a peak value of twice the average value):

Ipeak = 2*Iin/D

At low line voltage, D is:

D_ll = ton_ll/(ton_ll+toff_ll)

Ton_ll is the maximum on time, which we will set to 5.5 µs. (The device will limit the ON time to 6 µs if Ipeak is not reached.)

Since, in a critically discontinuous-mode flyback converter, the net transformer volt-seconds are zero:

Vpri*ton = N*Vsec*toff,

We can solve for toff:

toff_ll = Vin_min*ton_ll/(N*Vsec)

Example

Vin_min = 85*1.4142 = 120.21 V

toff_ll = 120.21*5.5x10^{-6}/(6*19.7) = 5.6x10^{-6}s

Iin = 70/(120.21*0.80) = 0.728 A

D_ll = 5.5x10^{-6}s/(5.5x10^{-6}s+5.6x10^{-6}s) = 0.495

f_sw = 1/(5.5x10^{-6}s+5.6x10^{-6}s) = 90 Khz

Ipeak = 2*0.728/0.495 = 2.94 A

12.3.1 Ipeak Resistors

The Ipeak resistors consist of a sense resistor (R6) and a voltage divider (R4 and R5). The Isense pin is a voltage amplifier with a gain of 5.0 that compares the amplified voltage to a reference of 1.2V.

Resistors R4, R5, and R6 are chosen to scale the voltage accordingly.

Example

We choose 0.1 Ω for R6.

The voltage across R6 at Ipeak is:

0.1*2.94 = 0.294 V.

We need the voltage at the Isense pin, Vc_pk, to be 1.2/5 or 0.24 when Ipeak is reached. If we choose R4 to be 2.2 K Ω, then

R5 = R4*(Ipeak*R6*gain – Vref)/Vref = 495

12.4 Primary Inductance

The inductance of the primary winding is based on the lowest supported line voltage, the longest ON time, and the peak current:

Lp = Vin_min * Ton_max/Ipeak

Example

Our design calls for an Lp of

Lp = 120.21 * 5.5x10^{-6} / 2.94 = 225 µH

12.5 Auxiliary Turns Ratio

The turns ratio between secondary and auxiliary winding is set to give 12V output plus a 0.6V diode drop to provide power to the chip:

Naux/Nsec = 12.6/Vout

12.6 Vaux Resistors

The output voltage is set by the resistor divider, R1 and R2, across the auxiliary winding voltage (Vauxw). The divided voltage is fed into the Vaux pin. A Schottky diode, D2, is used as a clamping diode in parallel with R2, to minimize negative voltages on the Vaux pin.

Vsec = Vauxw * (Nsec/Naux)

Voltage regulation is controlled by the resistor divider and the iW2202's internal voltage reference, which is fixed at 1.2V. The voltage on the Vaux pin is compared with the reference by the real-time waveform analysis circuitry. If it is above this level,

the next cycle will be a sense cycle. If it is below this level, the next cycle will be a power cycle:

Vauxw = Vref * (R1+R2)/R2

Vsec = 1.2* ((R1+R2)/R2 * (Nsec/Naux))

Example

Continuing our example, we see that Nsec/Naux = 19.7/12.6.

To find R1 and R2, we first note that:

Vauxw = Vref(1 + R1/R2) ,

R1 = (Vauxw –Vref)*R2/Vref

If we arbitrarily set R2 to 1.1 kΩ, we have:

R1 = (12.6 - 1.2)*1100/1.2 = 10.45 kΩ

12.7 PFC Choke and Capacitor

In the BIFRED topology used in this design, there is a definite relationship between the flyback primary inductance (Lp), the boost inductance (L1), and the boost capacitor (C1) voltage:

$L1 = (\eta * Vin\_rms^2 * L2)/Vc1^2$

We would like the bulk capacitor voltage to be no more than the peak input voltage:

$Vc1 = Vin\_rms * \sqrt{2}$

By substituting $Vin\_rms * \sqrt{2}$ for Vc1, we get:

L1 = η *Lp/2

Other implementations of the BIFRED technology operate at elevated capacitor voltages, but this does not occur with a pulseTrain controller.

The size of the bulk capacitor is based on ripple voltage requirements. We have used 2µf per watt of output power as a starting point.

Example

In our design:

L1 = 0.80*225µH/2 = 90 µH

C1 = 2.0*70 = 140 µF

12.8 Vin Resistors

The pin sensing line voltage uses a fixed resistor divider consisting of R7 and R8. R7 = 500 KΩ; R8 = 1 KΩ.

12.9 Conclusion

This example shows the simplicity of designing a power supply with an iWatt pulseTrain controller.

In particular, note the complete absence of loop compensation, eliminating the time and costs associated with loop compensation design.

We have also eliminated optoisolators and their associated feedback circuitry, reducing costs and PC board area.

Finally, PFC features have been added with a minimum of cost and design effort.

13 Physical Dimensions

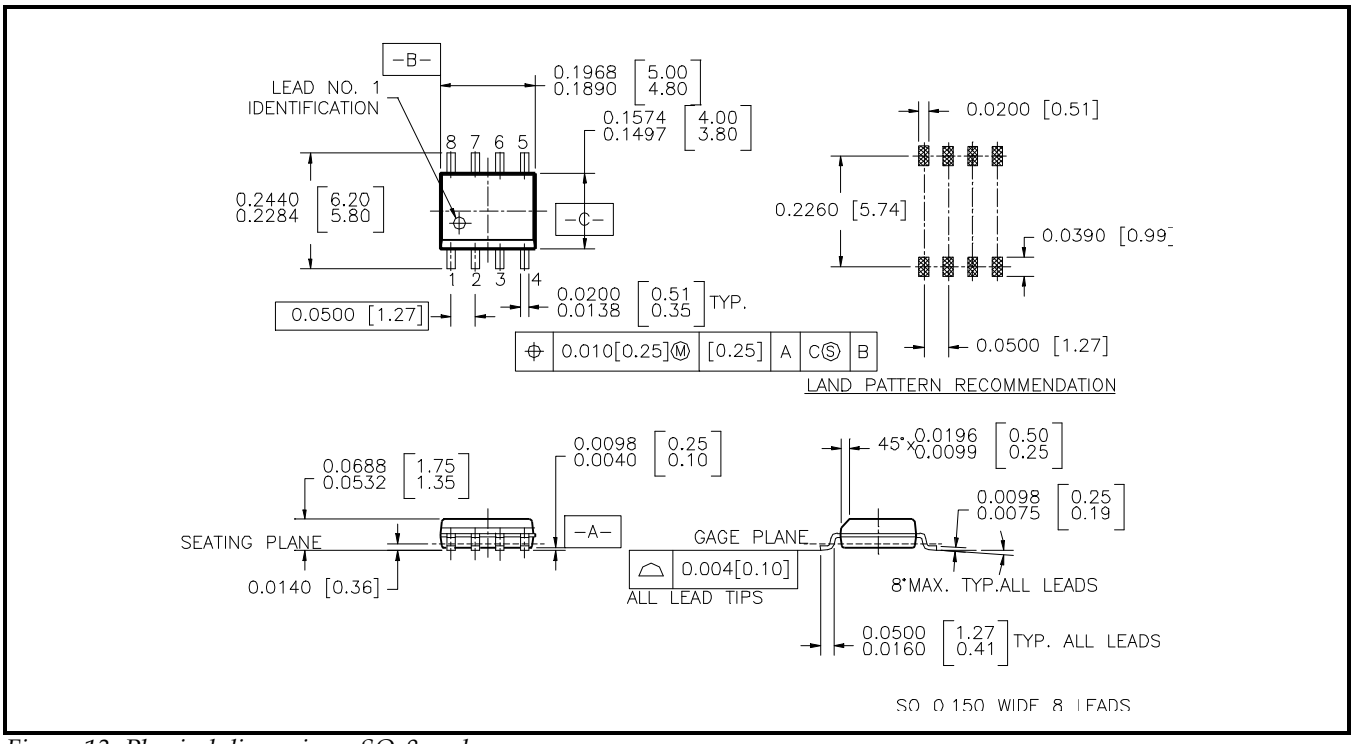


Figure 13. Physical dimensions, SO-8 package

14 About iWatt

iWatt Inc. is a fabless semiconductor company that develops power management ICs for computer, communication, and consumer markets. The company's patented pulseTrain ™ technology, the industry's first truly digital approach to power system regulation, is revolutionizing power supply design.

Trademark Information

iWatt and pulseTrain are trademarks of iWatt, Inc.

Contact Information

Web: http://www.iwatt.com

E-mail: sales@iwatt.com

Phone: 408-374-4200

Fax: 408-341-0455

iWatt Corporation
90 Albright Way
Los Gatos CA 95032

Disclaimer

iWatt reserves the right to make changes to its products and to discontinue products without notice.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

IWATT SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS, OR OTHER CRITICAL APPLICATIONS.

Inclusion of iWatt products in critical applications is understood to be fully at the risk of the customer. Questions concerning potential risk applications should be directed to iWatt through an iWatt sales office.

iWatt semiconductors are typically used in power supplies in which high voltages are present during operation. High-voltage safety precautions should be observed in design and operation to minimize the chance of injury.