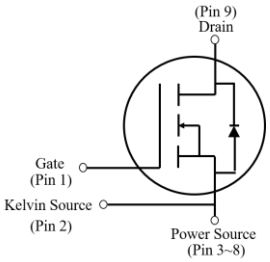
IV2Q06040L1 – 650V 40mΩ Gen2 SiC MOSFET

Features

- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- High operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin source pin easing driver circuit design

Outline:



TOLL

Applications

- Solar inverters
- UPS
- Motor drivers
- High voltage DC/DC converters
- Switch mode power supplies

Marking Diagram:

2Q06040L1
YYWWZ
XXXX

2Q06040L1 = Specific Device Code
YY = Year
WW = Work Week
Z = Assembly Location
XXXX = Lot Traceability

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DS}	Drain-Source voltage	650	V	V_{GS}=0V, I_D=100μA	
V_{GSmax} (DC)	Maximum DC voltage	-5 to 20	V	Static (DC)	
V_{GSmax} (Spike)	Maximum spike voltage	-10 to 23	V	Duty cycle<1%, and pulse width<200ns	
V_{GSon}	Recommended turn-on voltage	18±0.5	V		
V_{GSoff}	Recommended turn-off voltage	-3.5 to -2	V		
I_D	Drain current (continuous)	60	A	V_{GS}=18V, T_C=25°C	Fig. 21
		43	A	V_{GS}=18V, T_C=100°C	
I_{DM}	Drain current (pulsed)	150	A	Pulse width limited by SOA	Fig. 24
P_{TOT}	Total power dissipation	249	W	T_C=25°C	Fig. 22
T_{stg}	Storage temperature range	-55 to 175	°C		
T_J	Operating junction temperature	-55 to 175	°C		
T_L	Solder Temperature	260	°C	wave soldering only allowed at leads, 1.6mm from case for 10 s	

Thermal Data

Symbol	Parameter	Value	Unit	Note
$R_{\theta(J-C)}$	Thermal Resistance from Junction to Case	0.6	°C/W	Fig. 23

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
I_{DSS}	Zero gate voltage drain current		3	100	μA	V_{DS}=650V, V_{GS}=0V	
I_{GSS}	Gate leakage current			±100	nA	V_{DS}=0V, V_{GS}=-5~20V	
V_{TH}	Gate threshold voltage	1.8	2.8	4.5	V	V_{GS}=V_{DS}, I_D=7.5mA	Fig. 8, 9
			2.1			V_{GS}=V_{DS}, I_D=7.5mA @ T_J=175°C	
R_{ON}	Static drain-source on-resistance		40	53	mΩ	V_{GS}=18V, I_D=20A @T_J=25°C	Fig. 4, 5, 6, 7
			60		mΩ	V_{GS}=18V, I_D=20A @T_J=175°C	
C_{iss}	Input capacitance		2000		pF	V_{DS}=600V, V_{GS}=0V, f=1MHz, V_{AC}=25mV	Fig. 16
C_{oss}	Output capacitance		158		pF		
C_{rss}	Reverse transfer capacitance		11.4		pF		
E_{oss}	C_{oss} stored energy		31		μJ		Fig. 17
Q_g	Total gate charge		94.7		nC	V_{DS}=400V, I_D=20A, V_{GS}=-3 to 18V	Fig. 18
Q_{gs}	Gate-source charge		24.5		nC		
Q_{gd}	Gate-drain charge		47.3		nC		
R_g	Gate input resistance		2.9		Ω	f=1MHz	
E_{ON}	Turn-on switching energy		133.4		μJ	V_{DS}=400V, I_D=30A, V_{GS}=-3.5 to 18V, $R_{G(ext)}$=3.3Ω, L=200μH T_J=25°C	Fig. 19, 20
E_{OFF}	Turn-off switching energy		37.6		μJ		
$t_{d(on)}$	Turn-on delay time		7.0		ns		
t_r	Rise time		14.1				
$t_{d(off)}$	Turn-off delay time		17.0				
t_f	Fall time		8.0				

Reverse Diode Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
V_{SD}	Diode forward voltage		4.1		V	I_{SD}=20A, V_{GS}=0V	Fig. 10, 11, 12
			3.8		V	I_{SD}=20A, V_{GS}=0V, T_J=175°C	
t_{rr}	Reverse recovery time		33.3		ns	V_{GS}=-3.5V/+18V, I_{SD}=30A, V_R=400V, $R_{G(ext)}$=15Ω L=200μH di/dt=3000A/μs	
Q_{rr}	Reverse recovery charge		192.1		nC		
I_{RRM}	Peak reverse recovery current		17.5		A		

Typical Performance (curves)

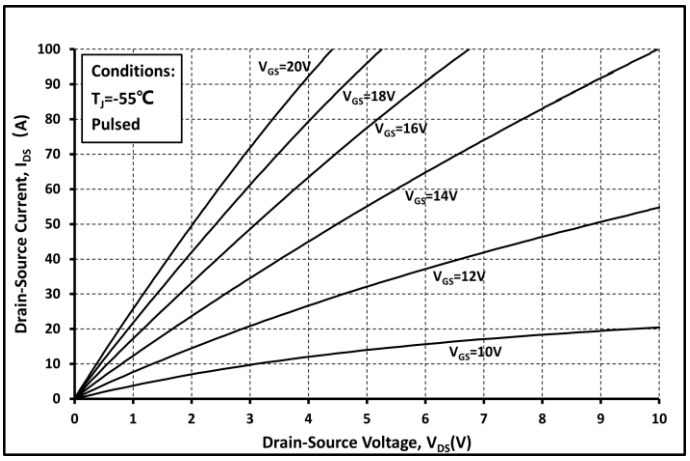


Fig. 1 Output Curve @ T_J=-55℃

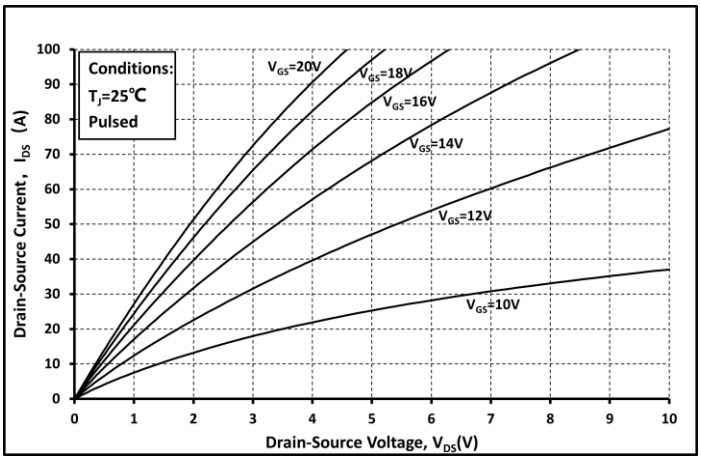


Fig. 2 Output Curve @ T_J=25℃

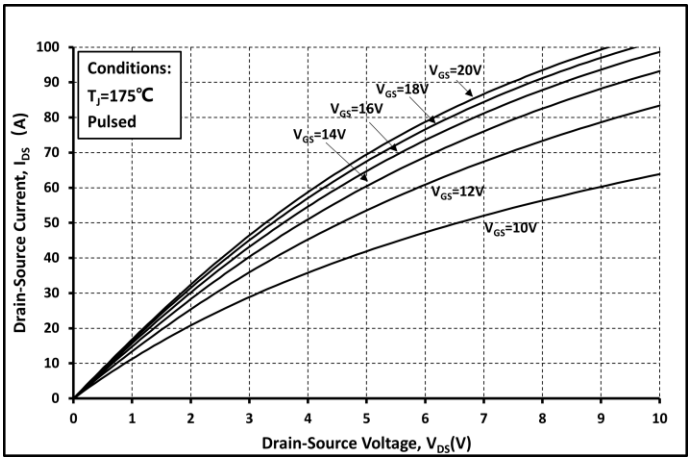


Fig. 3 Output Curve @ T_J=175℃

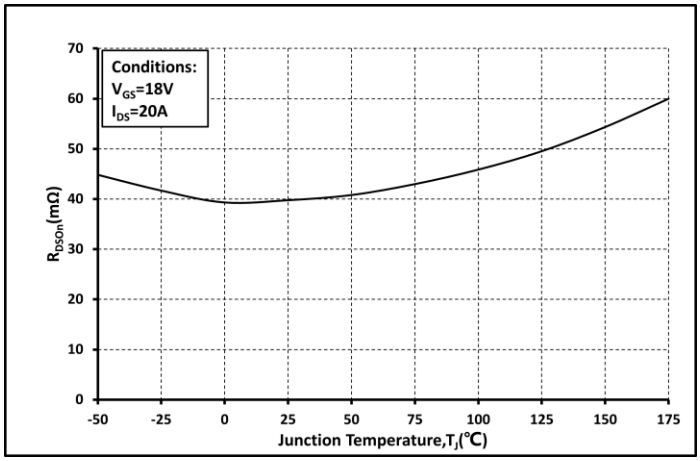


Fig. 4 Ron vs. Temperature

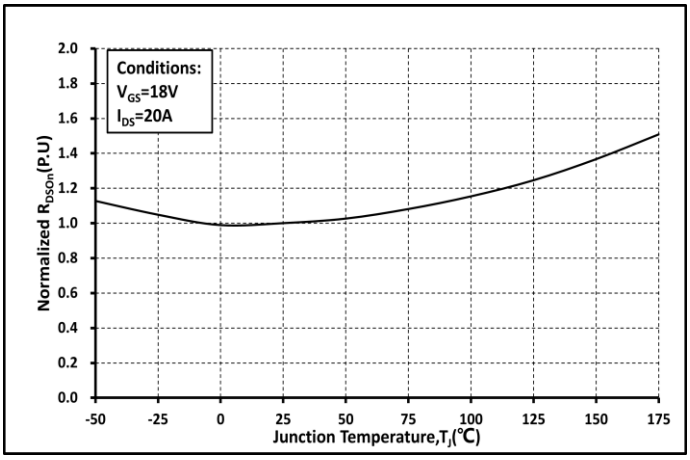


Fig. 5 Normalized Ron vs. Temperature

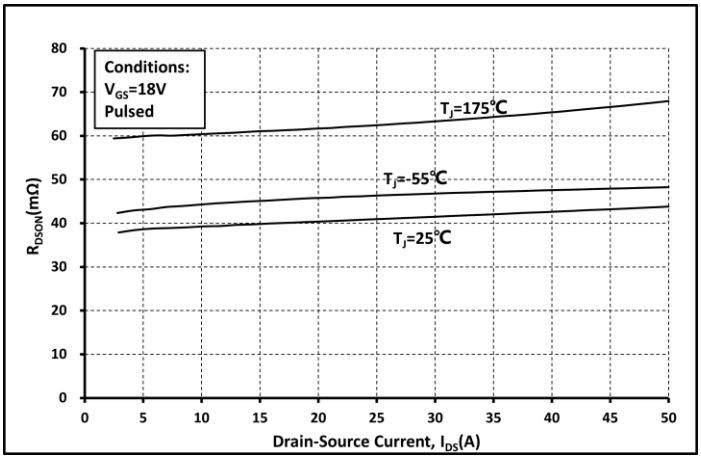


Fig. 6 Ron vs. I_{DS} @ Various Temperature

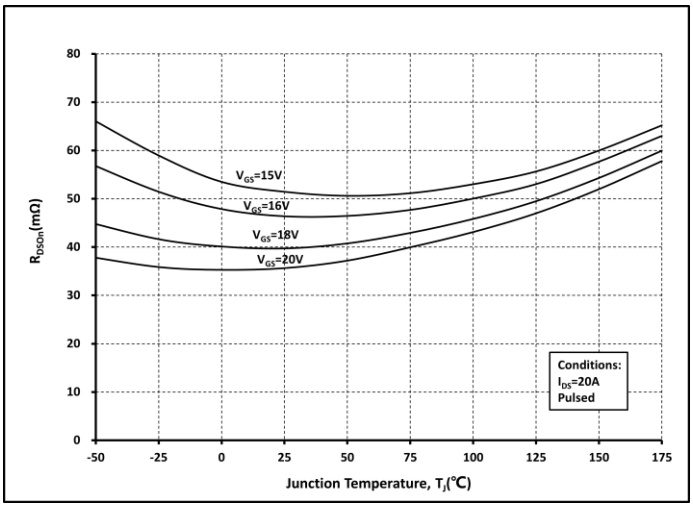


Fig. 7 Ron vs. Temperature @ Various V_{GS}

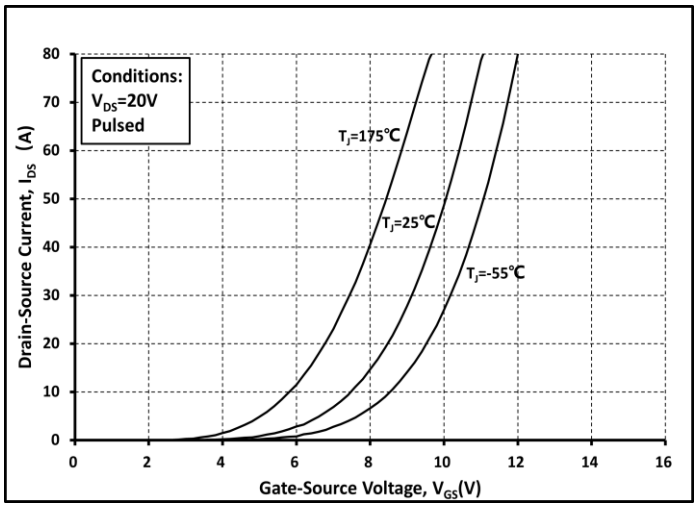


Fig. 8 Transfer Curves @ Various Temperature

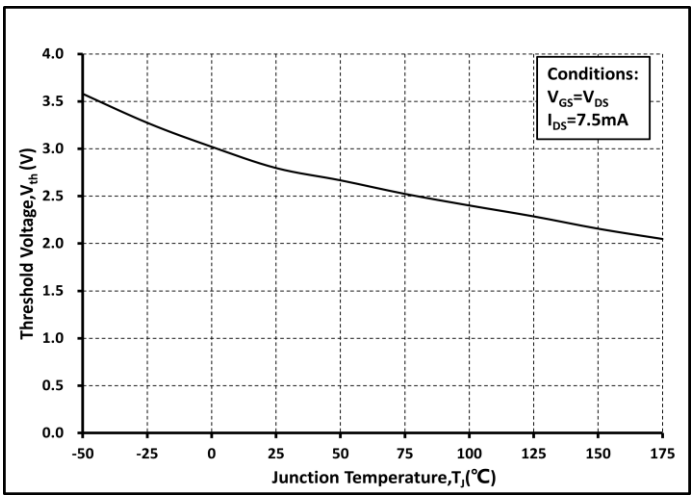


Fig. 9 Threshold Voltage vs. Temperature

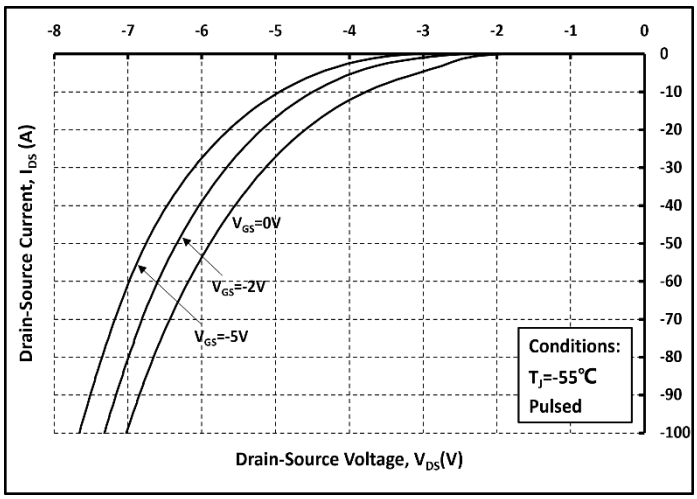


Fig. 10 Body Diode curves @ T_J=-55℃

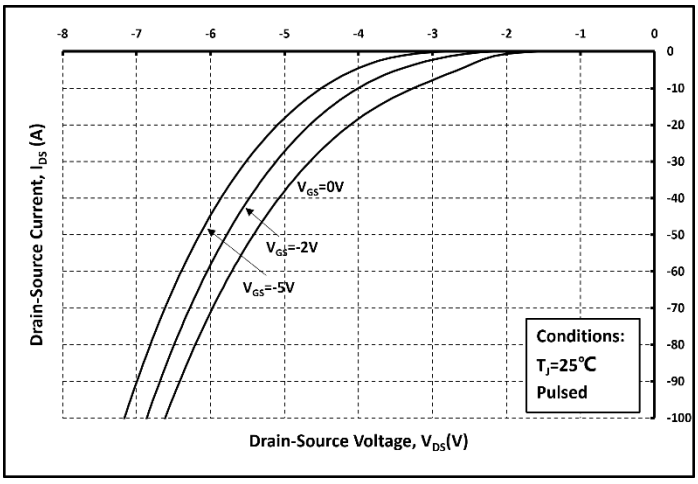


Fig. 11 Body Diode curves @ T_J=25℃

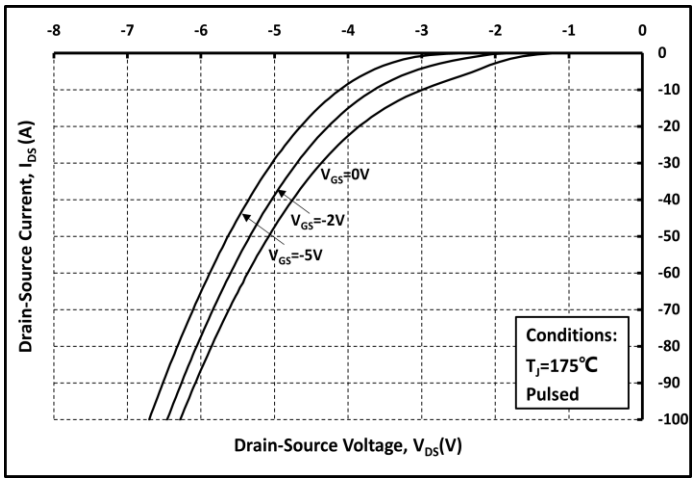


Fig. 12 Body Diode curves @ T_J=175℃

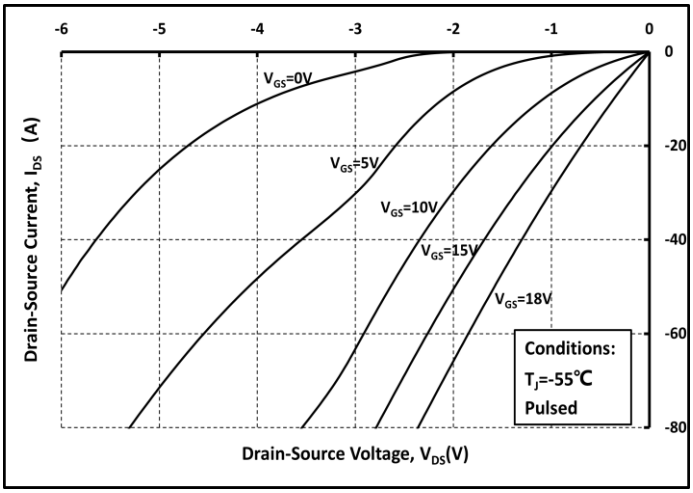


Fig. 13 3rd Quadrant curves @ T_J=-55°C

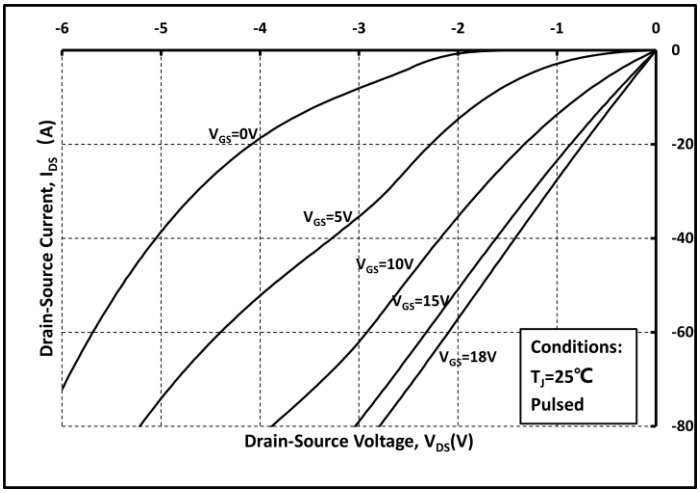


Fig. 14 3rd Quadrant curves @ T_J=25°C

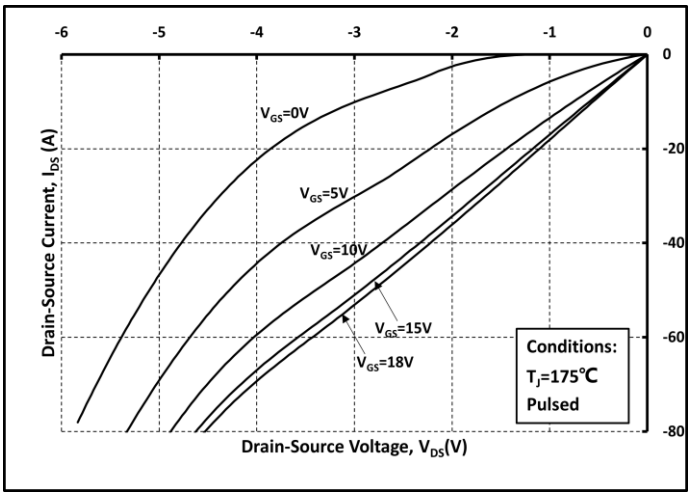


Fig. 15 3rd Quadrant curves @ T_J=175°C

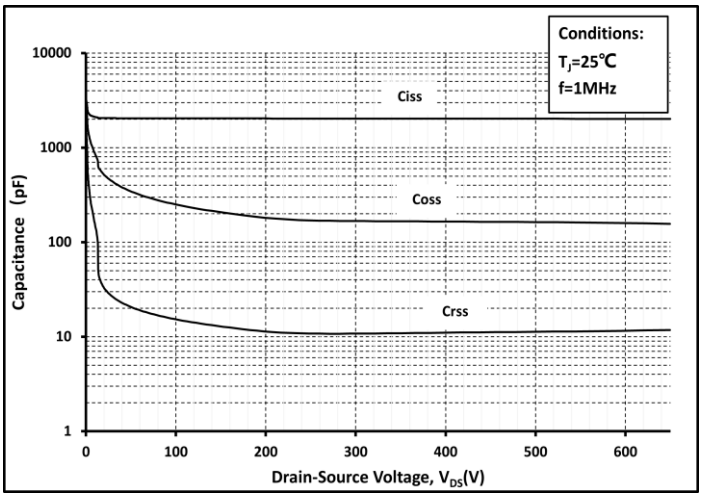


Fig. 16 Capacitance vs. V_{DS}

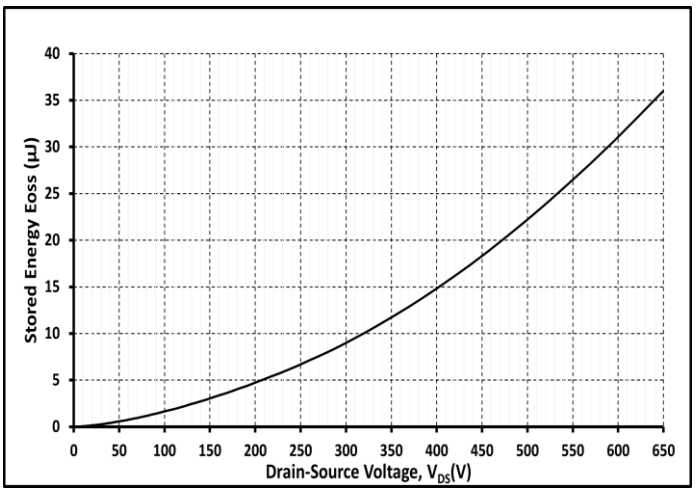


Fig. 17 Output Capacitor Stored Energy

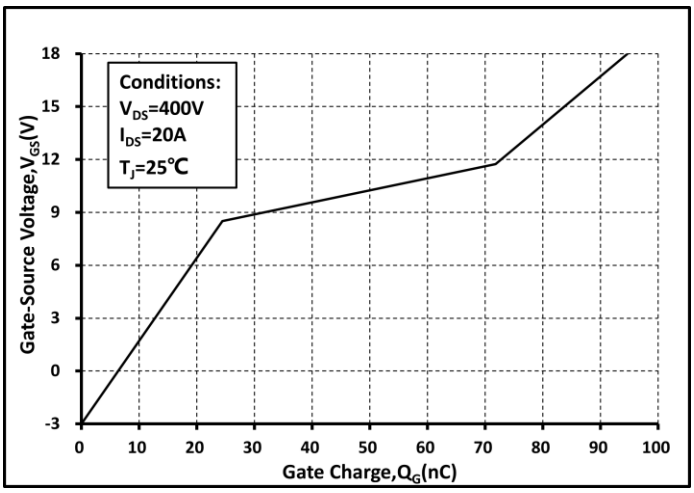


Fig. 18 Gate Charge Characteristics

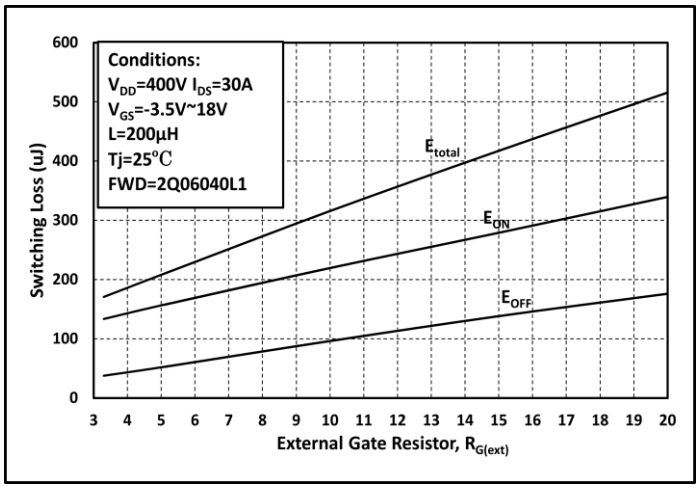


Fig. 19 Switching Energy vs. $R_{G(ext)}$

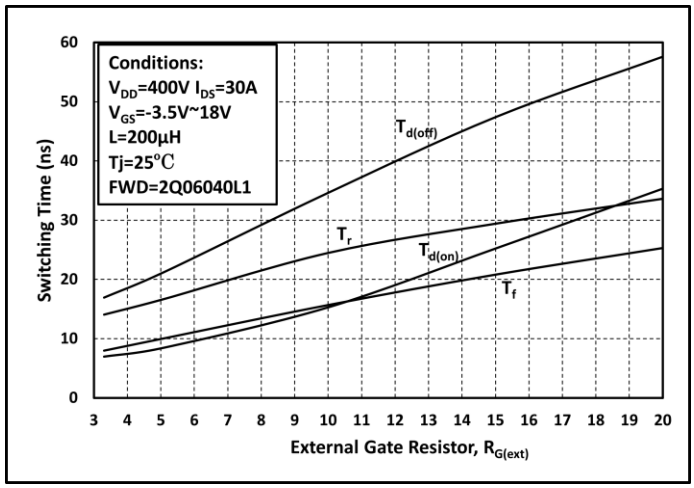


Fig. 20 Switching Times vs. $R_{G(ext)}$

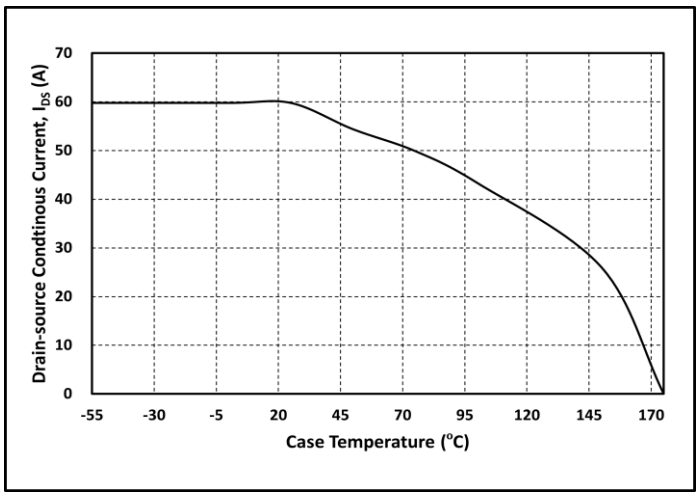


Fig. 21 Continuous Drain Current vs. Case Temperature

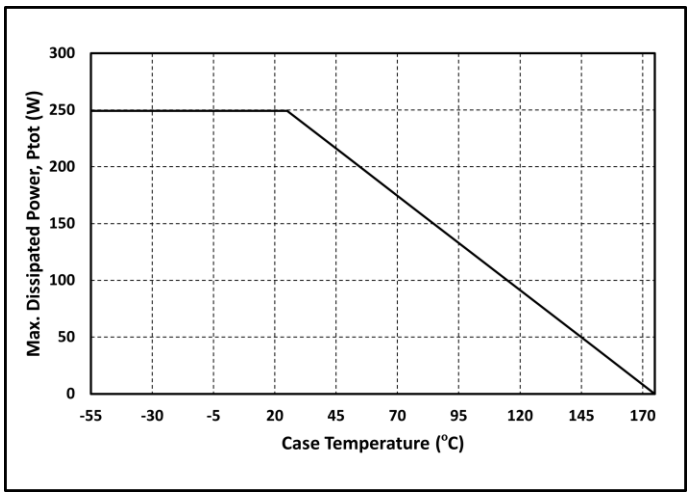


Fig. 22 Max. Power Dissipation Derating vs. Case Temperature

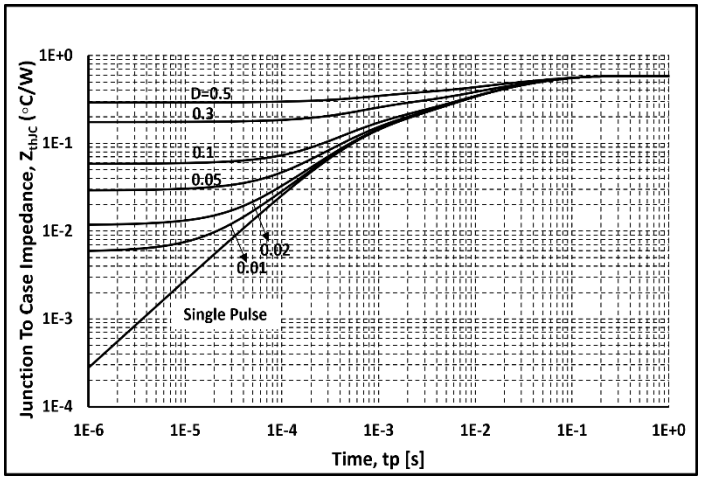


Fig. 23 Thermal impedance

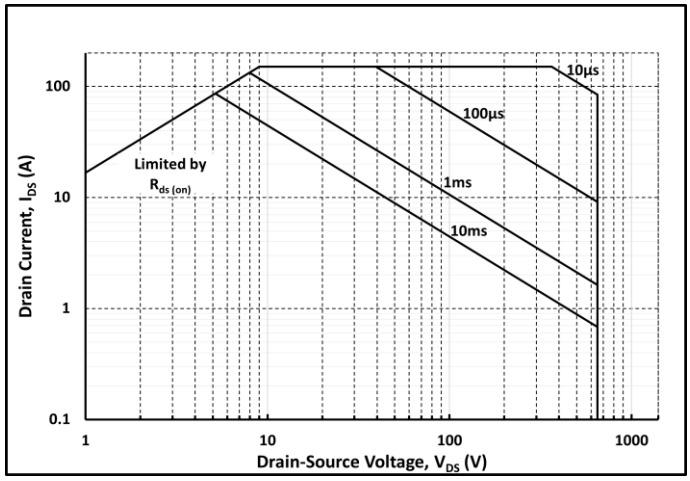
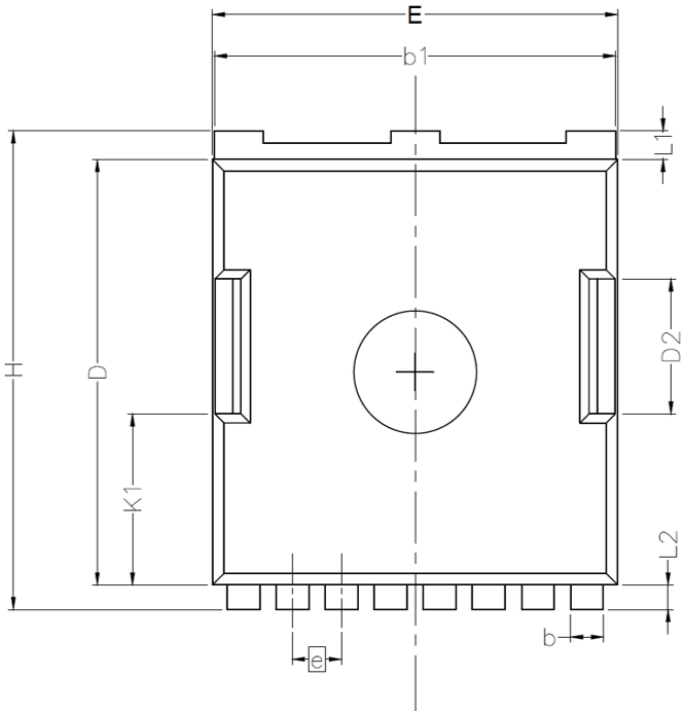
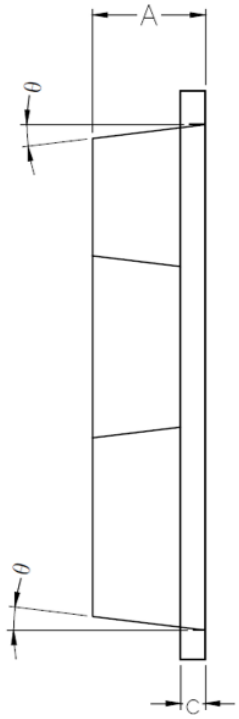


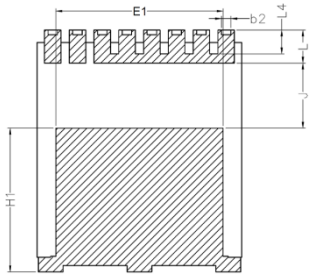
Fig. 24 Safe Operating Area

Package Dimensions



Dimensions In Millimeters		
SYMBOL	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.7	10.10
E1	7.90	8.30
e	1.20 BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°





Note:

1. Package Reference: JEDEC TOLL, Variation AD
2. All Dimensions are in mm
3. Slot Required, Notch May Be Rounded
4. Dimension D&E Do Not Include Mold Flash
5. Subject to Change Without Notice

Notes

For further information please contact IVCT's office.

The Information in this document is subject to change without notice.

Related Links

http://www.inventchip.com.cn