



# ISP1110

## Universal Serial Bus transceiver with UART signaling

Rev. 02 — 19 March 2007

Product data sheet

## 1. General description

---

The ISP1110 is a Universal Serial Bus (USB) transceiver that supports Universal Asynchronous Receiver-Transmitter (UART) signaling mode.

The ISP1110 USB transceiver is fully compliant with *Universal Serial Bus Specification Rev. 2.0*. The ISP1110 can transmit and receive USB data at full-speed (12 Mbit/s).

The ISP1110 transceiver allows USB Application Specific Integrated Circuits (ASICs) with I/O power supply voltage from 1.65 V to 2.85 V to interface to the physical layer of the USB. The transceiver has an integrated 5 V-to-3.3 V voltage regulator for direct powering through USB supply line  $V_{BUS}$  and an integrated voltage detector to detect the presence of the  $V_{BUS}$  voltage on the  $V_{CC(5V0)}$  pin. When  $V_{BUS}$  is present, the transceiver is in USB mode. When  $V_{BUS}$  is not present, the transceiver can be set to UART signaling mode.

The ISP1110 transceiver is available in HBCC16 lead-free and halogen-free package.

## 2. Features

---

- Fully complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports USB data transfer at full-speed (12 Mbit/s)
- Integrated DP pull-up resistor to reduce external components
- Implemented internal DP pull-up resistor as described in *ECN\_27%\_Resistor*
- Integrated 5 V-to-3.3 V voltage regulator to power through USB line  $V_{BUS}$
- $V_{BUS}$  voltage presence is indicated on pin VBUSDET
- Pins VP and VM function in bidirectional mode, allowing pin count saving for ASIC interface
- Used as a USB peripheral transceiver
- Stable RCV output during Single-Ended Zero (SE0) condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports 2.8 V UART signaling mode on the DP and DM lines
- Supports  $V_{CC(I/O)}$  voltage range from 1.65 V to 2.85 V
- Supports  $V_{CC(UART)}$  voltage range from 2.7 V to 4.5 V
- Off-state supply current from  $V_{CC(UART)}$  is less than 3  $\mu$ A
- Static current from  $V_{CC(I/O)}$  is less than 3  $\mu$ A (typical 1  $\mu$ A)
- Available in small HBCC16 (3 mm  $\times$  3 mm) lead-free and halogen-free package

3. Applications

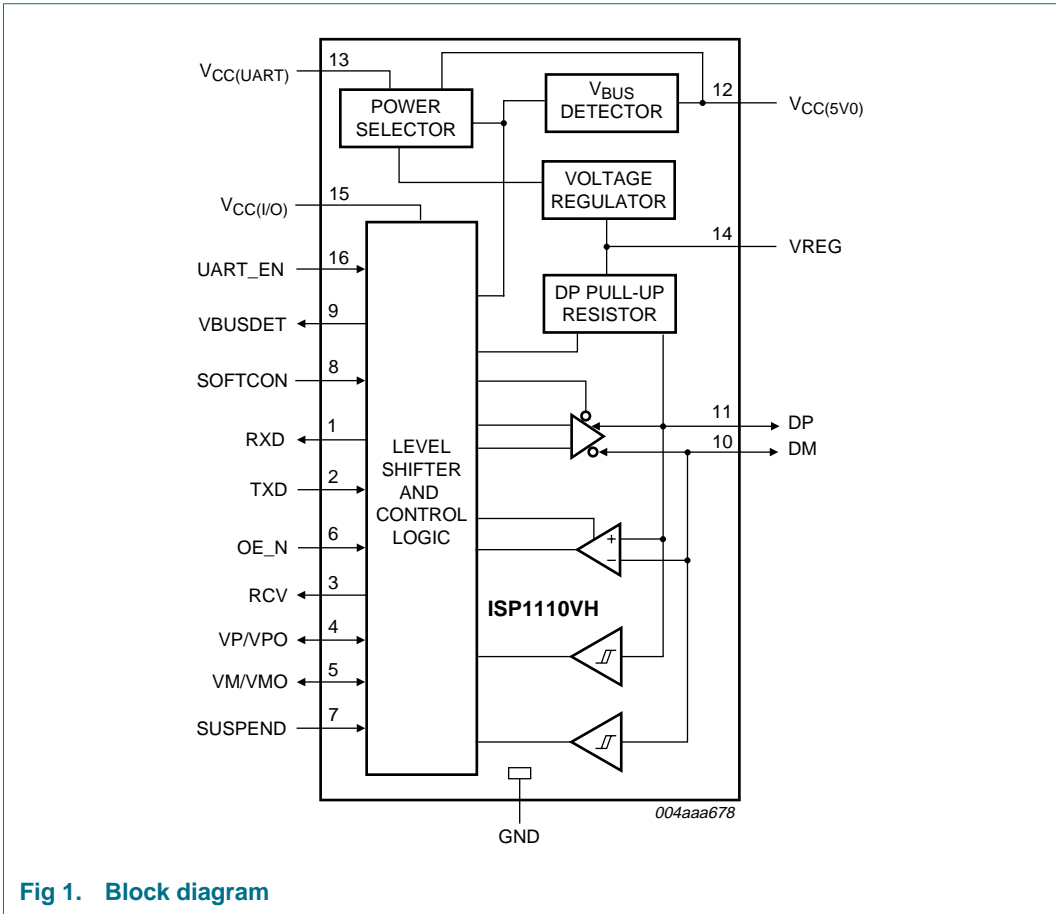
- Mobile phone
- Personal Digital Assistant (PDA)
- Other portable devices

4. Ordering information

Table 1. Ordering information

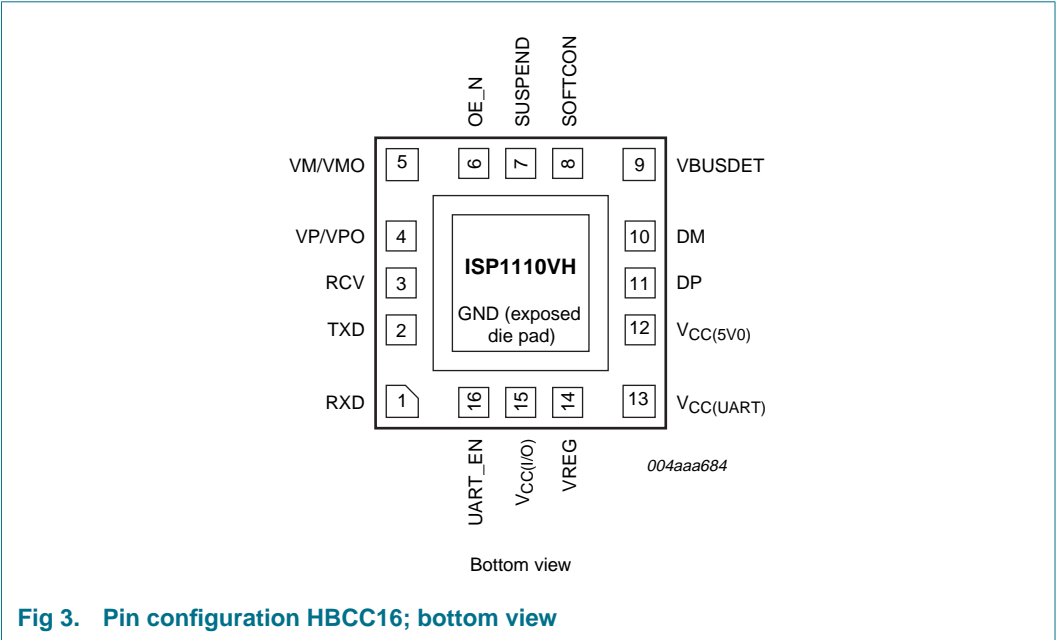
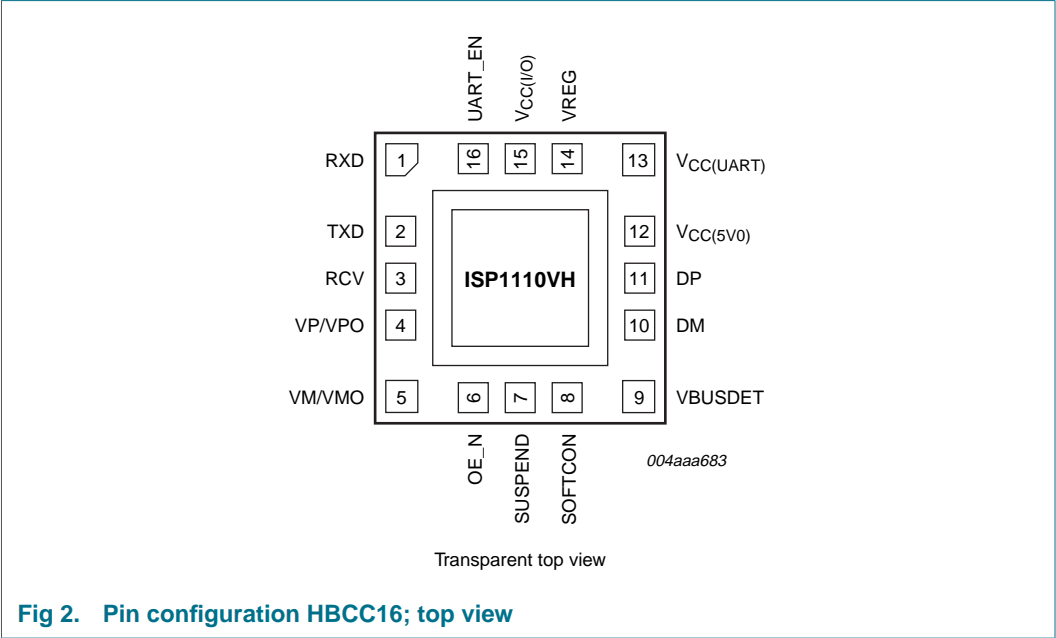
Type number	Package		Version
	Name	Description	
ISP1110VH	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2

5. Block diagram



6. Pinning information

6.1 Pinning



## 6.2 Pin description

Table 2. Pin description

Symbol <sup>[1]</sup>	Pin	Type <sup>[2]</sup>	Description
RXD	1	O	UART RXD output to microcontroller (CMOS level with respect to $V_{CC(I/O)}$ ); driven LOW in USB mode output pad; push pull; 4 mA output drive; CMOS
TXD	2	I	UART TXD input from microcontroller (CMOS level with respect to $V_{CC(I/O)}$ ) input pad; push pull; CMOS
RCV	3	O	differential data receiver output (CMOS level with respect to $V_{CC(I/O)}$ ); driven LOW when input SUSPEND is HIGH; the output state of RCV is preserved and stable during an SE0 condition; driven LOW when in UART mode output pad; push pull; 4 mA output drive; CMOS
VP/VPO	4	I/O	single-ended DP receiver output VP (CMOS level with respect to $V_{CC(I/O)}$ ); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VPO; see <a href="#">Table 5</a> and <a href="#">Table 6</a> bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
VM/VMO	5	I/O	single-ended DM receiver output VM (CMOS level with respect to $V_{CC(I/O)}$ ); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VMO; see <a href="#">Table 5</a> and <a href="#">Table 6</a> bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
OE_N	6	I	USB output enable (CMOS level with respect to $V_{CC(I/O)}$ , active LOW); enables the transceiver to transmit data on the USB bus input pad; push pull; CMOS
SUSPEND	7	I	suspend input (CMOS level with respect to $V_{CC(I/O)}$ ); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level; this pin is ignored when in UART mode input pad; push pull; CMOS
SOFTCON	8	I	software controlled USB connection input; a HIGH level enables the internal DP pull-up resistor when VBUSDET is HIGH; this pin is ignored when in UART mode input pad; push pull; CMOS
VBUSDET	9	O	$V_{BUS}$ indicator output (CMOS level with respect to $V_{CC(I/O)}$ ); when $V_{BUS} > V_{CC(5V0)th}$ , then VBUSDET = HIGH and when $V_{BUS} < V_{CC(5V0)th}$ , then VBUSDET = LOW output pad; push pull; 4 mA output drive; CMOS
DM	10	AI/O	<b>USB mode</b> — Negative USB data bus connection (analog, bidirectional, differential) <b>UART mode</b> — UART TXD line (digital output)
DP	11	AI/O	<b>USB mode</b> — Positive USB data bus connection (analog, bidirectional, differential) <b>UART mode</b> — UART RXD line (digital input)

Table 2. Pin description ...continued

Symbol <sup>[1]</sup>	Pin	Type <sup>[2]</sup>	Description
V <sub>CC(5V0)</sub>	12	-	supply voltage input (4.0 V to 5.5 V); can be directly connected to USB line V <sub>BUS</sub>
V <sub>CC(UART)</sub>	13	-	supply voltage input (2.7 V to 4.5 V) for the UART signaling
VREG	14	-	internal regulator output; a decoupling capacitor of at least 0.1 $\mu$ F is required
V <sub>CC(I/O)</sub>	15	-	supply voltage for digital I/O pins (1.65 V to 2.85 V). When V <sub>CC(I/O)</sub> is not connected, the DP and DM pins are in off-state. This supply pin is totally independent of V <sub>CC(5V0)</sub> and VREG, and must never exceed VREG.
UART_EN	16	I	enable UART signaling mode when V <sub>CC(5V0)</sub> is not present input pad; push-pull; CMOS
GND	exposed die pad	-	ground supply; down bonded to the exposed die pad (heat sink); to be connected to the PCB ground

[1] Symbol names ending with underscore N, for example, \_N, indicate active LOW signals.

[2] I = input; O = output; I/O = digital input/output; AI/O = analog input/output.

## 7. Functional description

### 7.1 Modes of operation

The ISP1110 supports two modes of operation:

- USB mode (3.3 V signaling)
- UART mode (2.8 V signaling)

[Table 3](#) shows the definition of various operating modes.

**Table 3. Operating modes: definition**

$V_{CC(I/O)}$	$V_{CC(UART)}$	$V_{CC(5V0)} = V_{BUS}$	UART_EN	Mode
Off	X	X	X	not defined
On	X	off	LOW	isolate mode
On	on	off	HIGH	UART mode
On	X	on	LOW	USB mode

[Table 4](#) shows the pin status in various operating modes.

**Table 4. Pin status in various modes**

Pin	Isolate mode	UART mode	USB mode
DP	not powered	high-Z	see <a href="#">Table 5</a>
DM	not powered	driven (= TXD)	see <a href="#">Table 5</a>
VP/VPO, VM/VMO	high-Z	LOW when OE_N = HIGH high-Z when OE_N = LOW	see <a href="#">Table 5</a>
RCV	LOW	LOW	see <a href="#">Table 5</a>
VBUSDET	LOW	LOW	HIGH
RXD	LOW	driven (= DP)	LOW
UART_EN, TXD, SUSPEND, SOFTCON, OE_N	high-Z	high-Z	high-Z
VREG	not powered	2.8 V	3.3 V

#### 7.1.1 USB mode

When the ISP1110 is in USB mode, pins DP and DM work as the USB D+ and D– lines, respectively. The DP and DM driver is powered by VREG. The USB function is compatible with the ISP1102 transceiver.

When the ISP1110 is in USB mode, the TXD input pin is ignored and the RXD output pin is driven LOW.

The ISP1110 is in USB mode when  $V_{CC(5V0)} > V_{CC(5V0)th}$  and UART\_EN is LOW.  $V_{CC(I/O)}$  must be on.

A short description of the USB detection sequence is:

1. The phone is connected to the USB port of a powered PC.
2. The ISP1110 detects  $V_{BUS}$  is above  $V_{CC(5V0)th}$ . The ISP1110 enters USB mode and the Analog USB Transceiver (ATX) is powered by VREG.

3. If the phone is switched off ( $V_{CC(I/O)}$  is not present), then the DP and DM pins of the ISP1110 remain at high-impedance and the PC will not detect any device attachment.
4. If the phone is switched on ( $V_{CC(I/O)}$  is present), then the ISP1110 will drive the VBUSDET pin to a HIGH level.
5. The phone processor detects that pin VBUSDET is HIGH. If the phone system software is ready for USB operation, the phone processor will assert pin SOFTCON.
6. The ISP1110 will enable the DP pull-up resistor ( $R_{PU(DP)}$ ).
7. The PC detects DP at the HIGH level and starts the USB full-speed enumeration.
8. The PC loads the driver for the phone, if enumeration is successful.

For the flowchart, see [Section 7.1.3](#).

### 7.1.2 UART mode

When the ISP1110 is in UART mode, the DP and DM driver is powered by 2.8 V. The ISP1110 works as a level shifter between these pairs of pins:

- From TXD ( $V_{CC(I/O)}$  level) to DM (2.8 V level).
- From DP (2.8 V level) to RXD ( $V_{CC(I/O)}$  level).

When the ISP1110 is in UART mode, the USB differential receiver is disabled. The SUSPEND and SOFTCON input pins are ignored. The RCV pin is driven LOW. The VP/VPO and VM/VMO pins are driven LOW, if OE\_N is HIGH. The VP/VPO and VM/VMO pins are 3-state LOW, if OE\_N is LOW.

The ISP1110 is in UART mode when  $V_{CC(5V0)} < V_{CC(5V0)th}$  and pin UART\_EN is HIGH.  $V_{CC(I/O)}$  and  $V_{CC(UART)}$  must be on.

A short description of the UART detection sequence is:

1. The phone is switched on ( $V_{CC(I/O)}$  is present).
2. If  $V_{BUS}$  is off, the ISP1110 will drive VBUSDET to a LOW level. The ATX is powered by 2.8 V.
3. The ISP1110 will enter UART signaling mode, if UART\_EN is HIGH.

For the flowchart, see [Section 7.1.3](#).

### 7.1.3 Mode detection flowchart

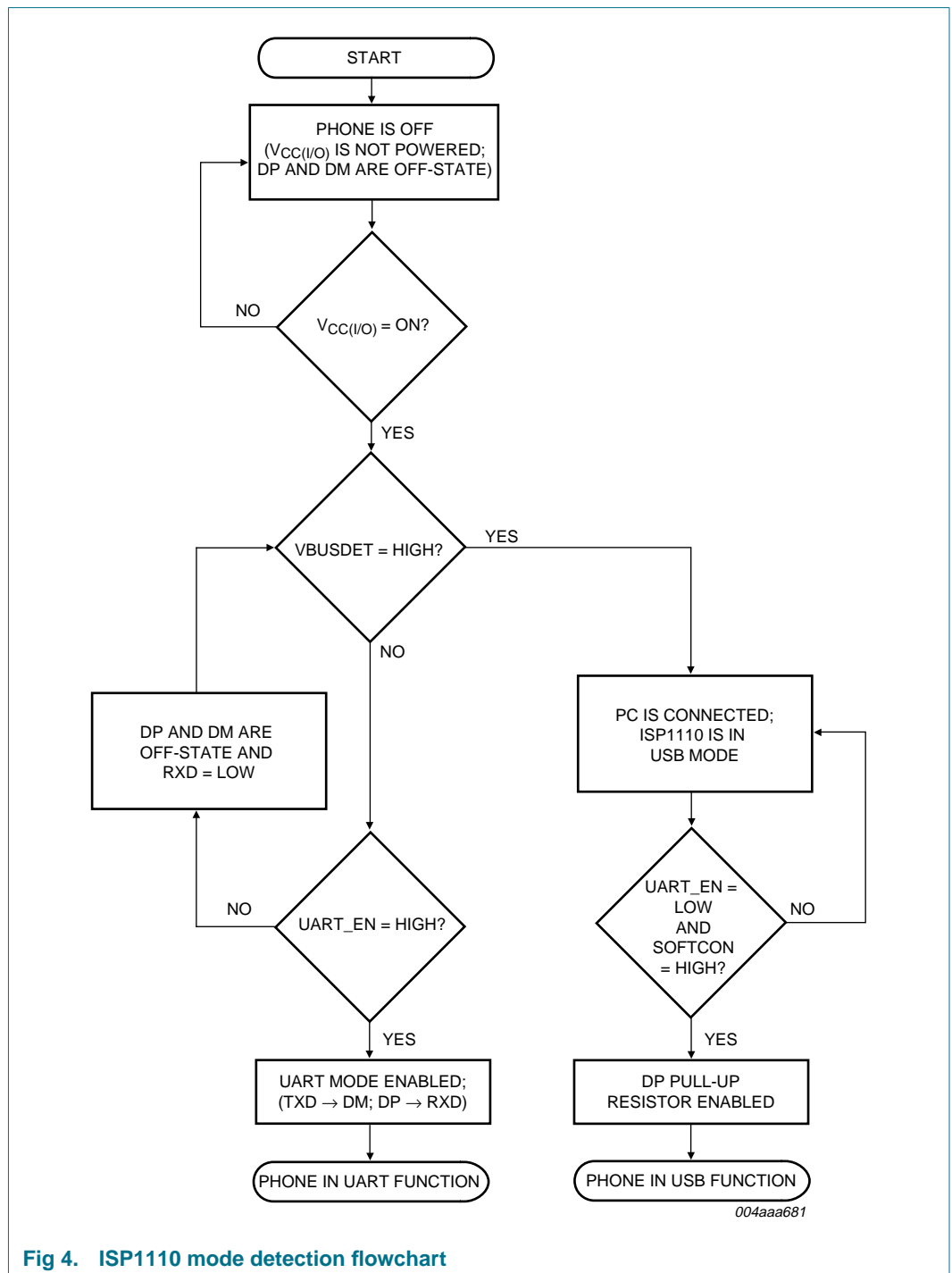


Fig 4. ISP1110 mode detection flowchart

### 7.1.4 Mode switching time

When the USB cable is connected, the ISP1110 is in USB mode. When the USB cable is removed and the UART cable is connected, the ISP1110 may switch to UART mode as long as the VBUSDET output is LOW. On the other hand, if the UART cable is removed and the USB cable is connected, the ISP1110 can switch to USB mode.



UART mode cannot be enabled until the voltage on  $V_{CC(5V0)}$  drops below the VBUSDET threshold (0.8 V to 4.0 V). Therefore, the time required to switch from USB mode to UART mode is determined by the RC discharge time on the  $V_{BUS}$  line. Given that  $V_{CC(5V0)} = 5.0$  V,  $R = 100$  k $\Omega$  and  $C = 1$   $\mu$ F, the discharge time is less than 200 ms (from 5 V to 0.8 V). Assume the detection of the UART cable connect or disconnect is very fast (within 1 ms), the total switching time from the USB cable removal to entering UART mode can be less than 200 ms. The total switching time from the UART cable removal to entering USB mode can be less than 200 ms.

When VBUSDET becomes LOW, it is recommended that you wait for 50 ms before asserting UART\_EN. This is because there is no hysteresis built for the VBUSDET threshold detector.

The time between VBUSDET going HIGH and SOFTCON assertion is 0 ms to 100 ms, according to *Universal Serial Bus Specification Rev. 2.0, Section 7.1.7.3*.

## 7.2 Analog USB Transceiver (ATX)

The ISP1110 ATX supports USB full-speed (12 Mbit/s) signaling. The ATX function is compatible with the ISP1102 transceiver. [Table 5](#) shows the function of the ATX.

**Table 5. USB function**

SUSPEND	OE_N	DP and DM	RCV	VP/VPO	VM/VMO	Function
LOW	LOW	driving/receiving	active	VPO input	VMO input	normal driving (differential receiver active)
LOW	HIGH	receiving <sup>[1]</sup>	active	VP output	VM output	receiving
HIGH	LOW	driving	inactive <sup>[2]</sup>	VPO input	VMO input	driving during suspend (differential receiver inactive)
HIGH	HIGH	high-Z <sup>[1]</sup>	inactive <sup>[2]</sup>	VP output	VM output	low-power state

[1] Signal levels on the DP and DM pins are determined by other USB devices and external pull-up or pull-down resistors.

[2] In suspend mode (SUSPEND = HIGH), the differential receiver is inactive and output RCV is always LOW. The resume signaling is detected through single-ended receivers VP/VPO and VM/VMO.

**Table 6. USB driving function (pin OE\_N = LOW)**

VM/VMO	VP/VPO	Data
LOW	LOW	SE0
LOW	HIGH	differential logic 1
HIGH	LOW	differential logic 0
HIGH	HIGH	illegal state

**Table 7. USB receiving function (pin OE\_N = HIGH)**

DP, DM	RCV	VP/VPO	VM/VMO
Differential logic 0	LOW	LOW	HIGH
Differential logic 1	HIGH	HIGH	LOW
SE0	RCV* <sup>[1]</sup>	LOW	LOW

[1] RCV\* denotes the signal level on output RCV just before the SE0 state occurs. This level is stable during the SE0 period.

### 7.3 V<sub>BUS</sub> detector

The V<sub>BUS</sub> detector provides voltage level detection on V<sub>BUS</sub>, if V<sub>BUS</sub> is connected to V<sub>CC(5V0)</sub>. If V<sub>BUS</sub> is greater than V<sub>BUS</sub> valid threshold V<sub>CC(5V0)th</sub>, pin VBUSDET will output a HIGH level. Otherwise, pin VBUSDET will output a LOW level.

The V<sub>BUS</sub> detector is powered by V<sub>CC(I/O)</sub>.

### 7.4 DP pull-up resistor

The internal DP pull-up resistor is connected between the VREG and DP pins, if pin SOFTCON is a HIGH level.

The pull-up resistor is context variable, as described in document *ECN\_27%\_Resistor*. The variable pull-up resistor hardware is implemented here to meet the *ECN\_27%\_Resistor* specification.

### 7.5 DC-DC regulator

In USB mode, when V<sub>CC(5V0)</sub> = 4.0 V to 5.5 V, the regulator will output 3.0 V to 3.6 V. In UART mode, when V<sub>CC(UART)</sub> = 2.7 V to 4.5 V, the regulator will output 2.35 V to 2.85 V.

A 0.1 μF capacitor is required to connect to the VREG pin.

### 7.6 Power selector

When VBUSDET = HIGH, the regulator will be powered by V<sub>CC(5V0)</sub>. When VBUSDET = LOW and UART\_EN = HIGH, the regulator will be powered by V<sub>CC(UART)</sub>.

When V<sub>CC(I/O)</sub> is not connected, the DP and DM output will be in off-state.

For proper operation, the V<sub>CC(I/O)</sub> voltage must not exceed VREG.

## 8. Limiting values

**Table 8. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		-0.5	+6.0	V
$V_{CC(UART)}$	supply voltage (UART)		-0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage		-0.5	+4.6	V
$V_I$	input voltage		-0.5	$V_{CC(I/O)} + 0.5$ V	V
$I_{lu}$	latch-up current	$V_I = -1.8$ V to +5.4 V	-	100	mA
$V_{ESD}$	electrostatic discharge voltage	all pins; $I_{LI} < 1$ $\mu$ A	[1] -2000	+2000	V
		pins DP, DM, $V_{CC(5V0)}$ , GND; $I_{LI} < 3$ $\mu$ A; 1 $\mu$ F capacitor on $V_{CC(5V0)}$	[1] -3000	+3000	V
$T_{stg}$	storage temperature		-40	+125	°C

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  resistor (Human Body Model).

## 9. Recommended operating conditions

**Table 9. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		4.0	5.0	5.5	V
$V_{CC(UART)}$	supply voltage (UART)		2.7	-	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		1.65	1.8	2.85	V
$V_I$	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{IA(I/O)}$	input voltage on analog I/O pins	pins DP and DM	0	-	3.6	V
$T_{amb}$	ambient temperature		-40	-	+85	°C
$T_j$	junction temperature		-40	-	+125	°C

## 10. Static characteristics

**Table 10. Static characteristics: supply pins**

$V_{CC(5V0)} = 4.0$  V to 5.5 V;  $V_{CC(UART)} = 2.7$  V to 4.5 V;  $V_{CC(I/O)} = 1.65$  V to 2.85 V;  $T_{amb} = -40$  °C to +85 °C.

Typical values are at  $V_{CC(5V0)} = 5.0$  V;  $V_{CC(UART)} = 2.8$  V;  $V_{CC(I/O)} = 1.8$  V;  $T_{amb} = +25$  °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(VREG)}$	output voltage on pin VREG	USB mode	[1] 3.0	3.3	3.6	V
		UART mode	2.35	2.6	2.85	V
$I_{CC(5V0)}$	supply current (5.0 V)	USB mode; transmitting and receiving at 12 Mbit/s; $C_L = 50$ pF on pins DP and DM	[2] -	4	8	mA
$I_{CC(UART)}$	supply current (UART)	UART mode; 921.6 kbit/s	-	-	4	mA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	transmitting and receiving at 12 Mbit/s	[2] -	1	2	mA

**Table 10. Static characteristics: supply pins ...continued**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$ ;  $V_{CC(UART)} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }2.85\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ .

Typical values are at  $V_{CC(5V0)} = 5.0\text{ V}$ ;  $V_{CC(UART)} = 2.8\text{ V}$ ;  $V_{CC(I/O)} = 1.8\text{ V}$ ;  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(5V0)(idle)}$	idle and SE0 supply current (5.0 V)	USB mode; idle: $V_{DP} > 2.7\text{ V}$ , $V_{DM} < 0.3\text{ V}$ ; SE0: $V_{DP} < 0.3\text{ V}$ , $V_{DM} < 0.3\text{ V}$	[3] -	-	300	$\mu\text{A}$
$I_{CC(I/O)(static)}$	static supply current on pin $V_{CC(I/O)}$		-	-	3	$\mu\text{A}$
$I_{CC(5V0)(susp)}$	suspend mode supply current (5.0 V)	USB mode SUSPEND = HIGH	[3] -	-	35	$\mu\text{A}$
$I_{CC(UART)(off)}$	off-state supply current (UART)	USB mode or UART_EN = LOW	-	-	3	$\mu\text{A}$
$V_{CC(5V0)th}$	supply voltage detection threshold (5.0 V)	$1.65\text{ V} \leq V_{CC(I/O)} \leq 2.85\text{ V}$	0.8	-	4.0	V
$V_{CC(I/O)th}$	supply voltage detection threshold (I/O)		0.5	-	1.4	V

[1] The minimum voltage is 2.7 V in suspend mode.

[2] Maximum value characterized only, not tested in production.

[3] Excluding any load current and source current to the DP/DM pull-up and pull-down resistors (200  $\mu\text{A}$  typical).

**Table 11. Static characteristics: digital pins**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$ ;  $V_{CC(UART)} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }2.85\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ .

Typical values are at  $V_{CC(5V0)} = 5.0\text{ V}$ ;  $V_{CC(UART)} = 2.8\text{ V}$ ;  $V_{CC(I/O)} = 1.8\text{ V}$ ;  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC(I/O)</sub> = 1.65 V to 2.85 V						
Input levels						
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3V <sub>CC(I/O)</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>CC(I/O)</sub>	-	-	V
Output levels						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-	-	0.15	V
		I <sub>OL</sub> = 2 mA	-	-	0.4	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = 100 μA	V <sub>CC(I/O)</sub> – 0.15 V	-	-	V
		I <sub>OH</sub> = 2 mA	V <sub>CC(I/O)</sub> – 0.4 V	-	-	V
Leakage current						
I <sub>LI</sub>	input leakage current		[1] –1	-	+1	μA
Capacitance						
C <sub>in</sub>	input capacitance	pin to GND	-	-	10	pF
Example 1: V <sub>CC(I/O)</sub> = 1.8 V ± 0.15 V						
Input levels						
V <sub>IL</sub>	LOW-level input voltage		-	-	0.5	V
V <sub>IH</sub>	HIGH-level input voltage		1.2	-	-	V
Output levels						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-	-	0.15	V
		I <sub>OL</sub> = 2 mA	-	-	0.4	V

**Table 11. Static characteristics: digital pins ...continued**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$ ;  $V_{CC(UART)} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }2.85\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ .  
 Typical values are at  $V_{CC(5V0)} = 5.0\text{ V}$ ;  $V_{CC(UART)} = 2.8\text{ V}$ ;  $V_{CC(I/O)} = 1.8\text{ V}$ ;  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = 100 μA	1.5	-	-	V
		I <sub>OH</sub> = 2 mA	1.25	-	-	V
Example 2: V <sub>CC(I/O)</sub> = 2.775 V ± 0.075 V						
Input levels						
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
V <sub>IH</sub>	HIGH-level input voltage		3.0	-	-	V
Output levels						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-	-	0.15	V
		I <sub>OL</sub> = 2 mA	-	-	0.4	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = 100 μA	2.55	-	-	V
		I <sub>OH</sub> = 2 mA	2.3	-	-	V

[1] If  $V_{CC(I/O)} \geq V_{CC(UART)}$ , then the leakage current will be higher than the specified value when in UART mode.

**Table 12. Static characteristics: analog I/O pins DP and DM**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$ ;  $V_{CC(UART)} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }2.85\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ .  
 Typical values are at  $V_{CC(5V0)} = 5.0\text{ V}$ ;  $V_{CC(UART)} = 2.8\text{ V}$ ;  $V_{CC(I/O)} = 1.8\text{ V}$ ;  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input levels (USB mode)</b>						
<b>Differential receiver</b>						
$V_{DI}$	differential input sensitivity	$ V_{DP} - V_{DM} $	0.2	-	-	V
$V_{CM}$	differential common mode voltage range	includes $V_{DI}$ range	0.8	-	2.5	V
<b>Single-ended receiver</b>						
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{hys}$	hysteresis voltage		0.4	-	0.7	V
<b>Input levels (UART mode)</b>						
$V_{IL}$	LOW-level input voltage		-0.3	-	+0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	3.0	V
$V_{hys}$	hysteresis voltage		0.4	-	0.7	V
<b>Output levels (USB mode)</b>						
$V_{OL}$	LOW-level output voltage	$R_L = 1.5\text{ k}\Omega\text{ to }3.6\text{ V}$	-	-	0.3	V
$V_{OH}$	HIGH-level output voltage	$R_L = 15\text{ k}\Omega\text{ to GND}$	[1] 2.8	-	3.6	V
<b>Output levels (UART mode)</b>						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 4\text{ mA}$	-0.1	-	+0.37	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 4\text{ mA}$	2.16	-	2.85	V
<b>Leakage current</b>						
$I_{LZ}$	off-state leakage current		-1	-	+1	$\mu\text{A}$
<b>Capacitance</b>						
$C_{in}$	input capacitance	pin to GND	-	-	10	pF

**Table 12. Static characteristics: analog I/O pins DP and DM ...continued**

$V_{CC(SV0)} = 4.0\text{ V to }5.5\text{ V}$ ;  $V_{CC(UART)} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }2.85\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ .

Typical values are at  $V_{CC(SV0)} = 5.0\text{ V}$ ;  $V_{CC(UART)} = 2.8\text{ V}$ ;  $V_{CC(I/O)} = 1.8\text{ V}$ ;  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Resistance						
Z <sub>DRV</sub>	driver output impedance	steady-state drive	[2] 34	39	44	Ω
Z <sub>INP</sub>	input impedance		10	-	-	MΩ
R <sub>PU(DP)</sub>	pull-up resistance on pin DP	bus idle	900	-	1575	Ω
		bus active	1425	-	3090	Ω
Termination						
V <sub>TERM</sub>	termination voltage	for upstream port pull-up (R <sub>PU(DP)</sub> )	[3][4] 3.0	-	3.6	V

[1]  $V_{OH(min)} = V_{REG} - 0.2\text{ V}$ .

[2] Includes external resistors of  $33\text{ }\Omega \pm 1\%$  on pins DP and DM.

[3] This voltage is available at pin VREG.

[4] The minimum voltage is 2.7 V in suspend mode.

## 11. Dynamic characteristics

**Table 13. Dynamic characteristics: analog I/O pins DP and DM**

$V_{CC(SV0)} = 4.0\text{ V to }5.5\text{ V}$ ;  $V_{CC(UART)} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }2.85\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ .

Typical values are at  $V_{CC(SV0)} = 5.0\text{ V}$ ;  $V_{CC(UART)} = 2.8\text{ V}$ ;  $V_{CC(I/O)} = 1.8\text{ V}$ ;  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Driver characteristics (UART mode)</b>						
$t_{LR}$	transition time: rise time	$C_L < 250\text{ pF}$ ; 10 % to 90 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 5</a>	[1] 50	-	200	ns
$t_{LF}$	transition time: fall time	$C_L < 250\text{ pF}$ ; 90 % to 10 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 5</a>	[1] 50	-	200	ns
<b>Driver characteristics (USB mode)</b>						
$t_{FR}$	rise time	$C_L = 50\text{ pF to }125\text{ pF}$ ; 10 % to 90 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 5</a>	4	-	20	ns
$t_{FF}$	fall time	$C_L = 50\text{ pF to }125\text{ pF}$ ; 90 % to 10 % of $ V_{OH} - V_{OL} $ ; see <a href="#">Figure 5</a>	4	-	20	ns
FRFM	differential rise time/fall time matching	excluding the first transition from Idle state	[2] 90	-	111.1	%
$V_{CRS}$	output signal crossover voltage	excluding the first transition from Idle state; see <a href="#">Figure 6</a>	[3] 1.3	-	2.0	V
<b>Driver timing</b>						
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	VPO, VMO to DP, DM; see <a href="#">Figure 6</a> and <a href="#">Figure 9</a>	-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	VPO, VMO to DP, DM; see <a href="#">Figure 6</a> and <a href="#">Figure 9</a>	-	-	18	ns
$t_{PHZ}$	driver disable delay from HIGH level	OE_N to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a>	-	-	15	ns
$t_{PLZ}$	driver disable delay from LOW level	OE_N to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a>	-	-	15	ns

**Table 13. Dynamic characteristics: analog I/O pins DP and DM ...continued**

$V_{CC(5V0)} = 4.0\text{ V to }5.5\text{ V}$ ;  $V_{CC(UART)} = 2.7\text{ V to }4.5\text{ V}$ ;  $V_{CC(I/O)} = 1.65\text{ V to }2.85\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ .

Typical values are at  $V_{CC(5V0)} = 5.0\text{ V}$ ;  $V_{CC(UART)} = 2.8\text{ V}$ ;  $V_{CC(I/O)} = 1.8\text{ V}$ ;  $T_{amb} = +25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PZH}$	driver enable delay to HIGH level	OE_N to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a>	-	-	15	ns
$t_{PZL}$	driver enable delay to LOW level	OE_N to DP, DM; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a>	-	-	15	ns

### Receiver timings

#### Differential receiver

$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RCV; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>	-	-	15	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RCV; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>	-	-	15	ns

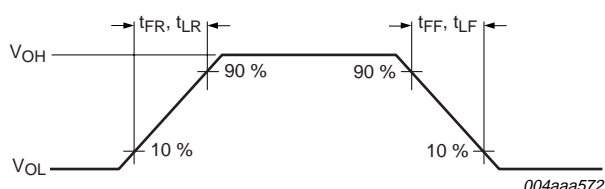
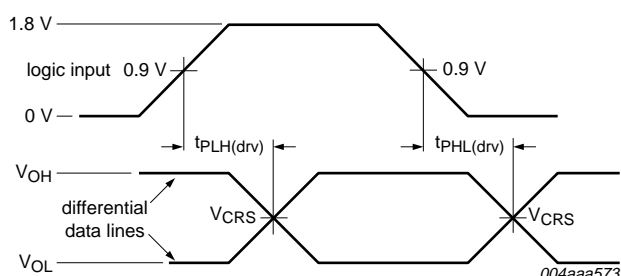
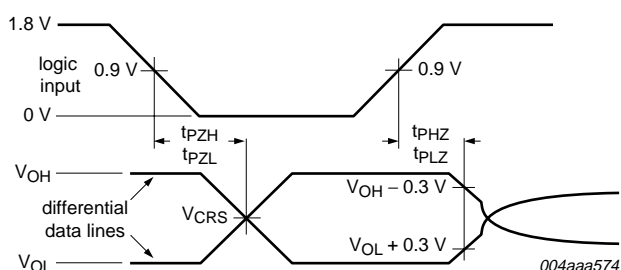
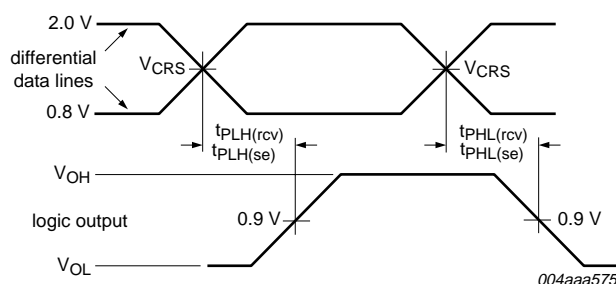
#### Single-ended receiver

$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to VP/VPO, VM/VMO; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>	-	-	18	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to VP/VPO, VM/VMO; see <a href="#">Figure 8</a> and <a href="#">Figure 11</a>	-	-	18	ns

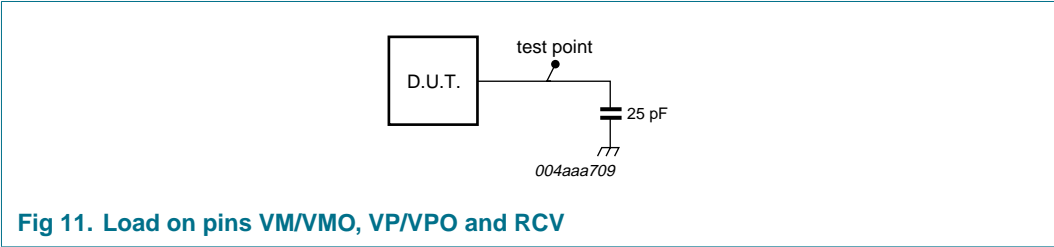
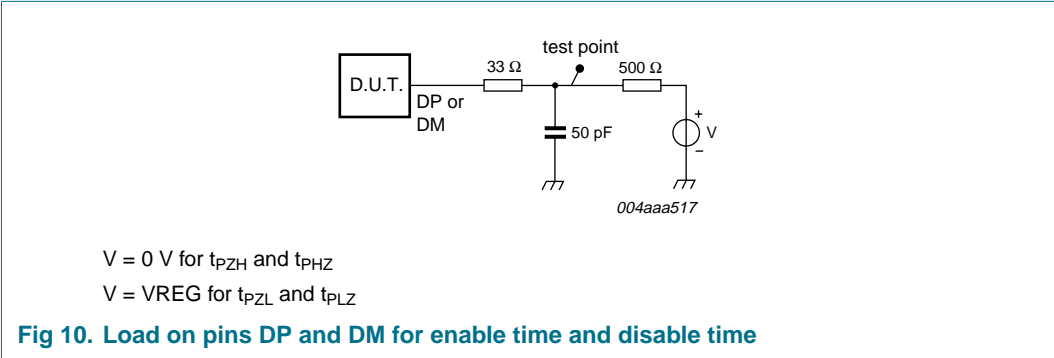
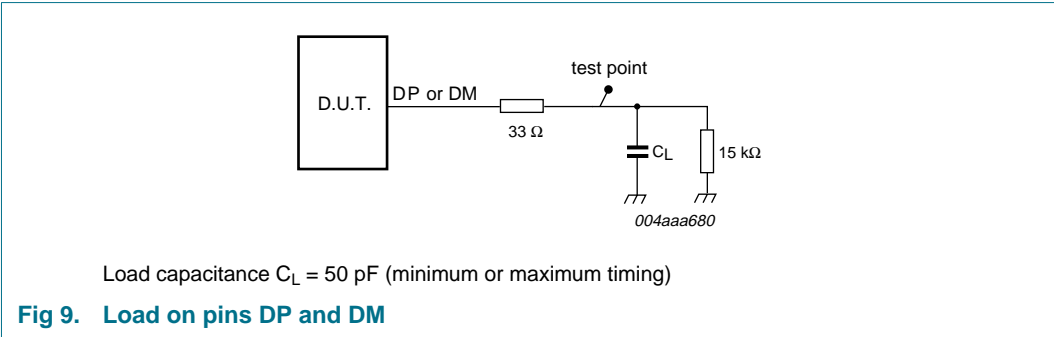
[1] For UART TXD on pin DM.

[2]  $t_{FR}$  /  $t_{FF}$ .

[3] Characterized only, not tested. Limits guaranteed by design.

**Fig 5. Rise time and fall time****Fig 6. Timing of VPO and VMO to DP and DM****Fig 7. Timing of OE\_N to DP and DM****Fig 8. Timing of DP and DM to RCV, VP/VPO and VM/VMO**

12. Test information





13. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mmSOT639-2

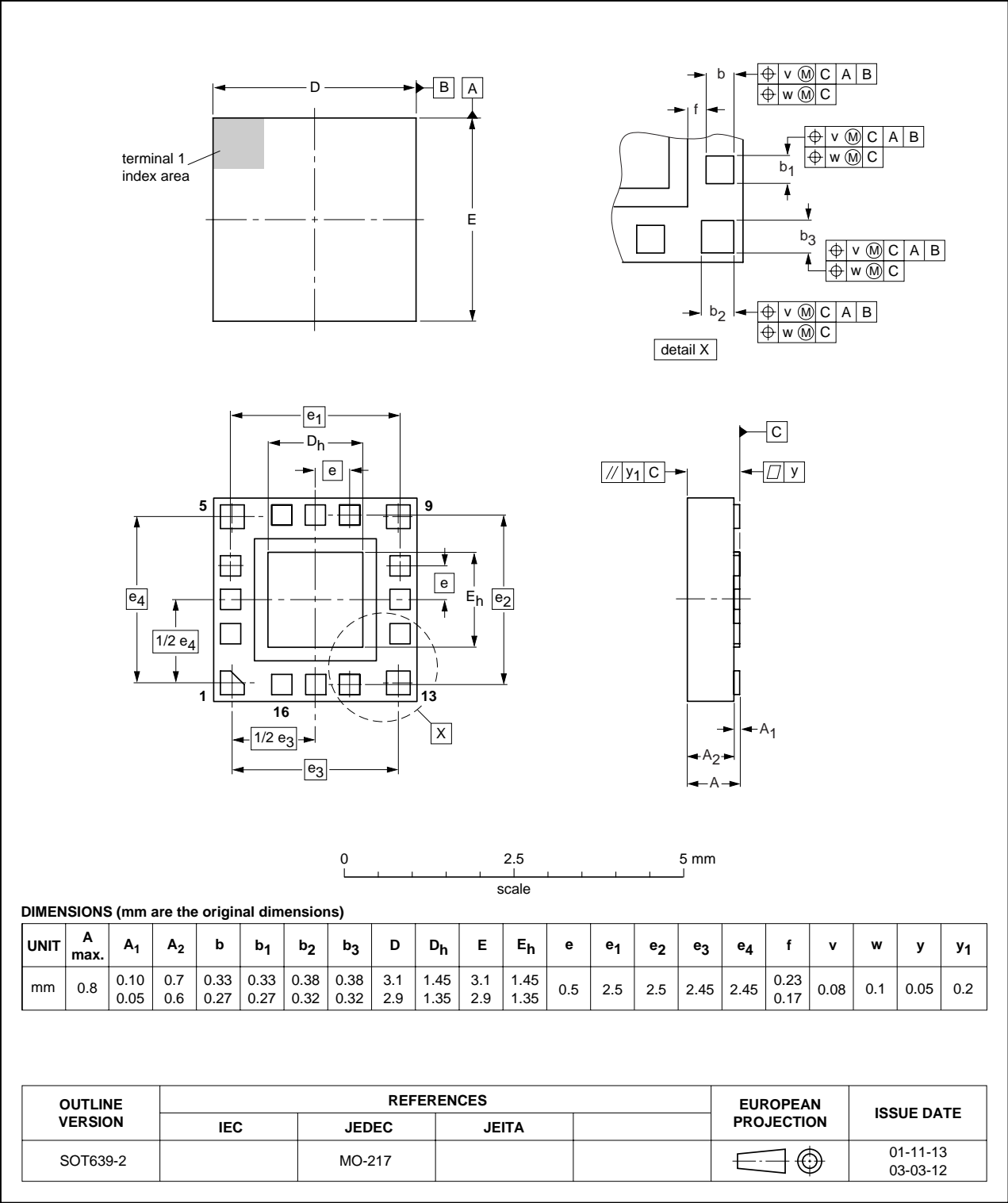


Fig 12. Package outline SOT639-2 (HBCC16)

## 14. Packing information

The ISP1110VH (HBCC16 package) is delivered on a Type A carrier tape, see [Figure 13](#). The tape dimensions are given in [Table 14](#).

The reel diameter is 330 mm. The reel is made of polystyrene and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is  $\pm 0.02$  mm. The camber must not exceed 1 mm in 100 mm.

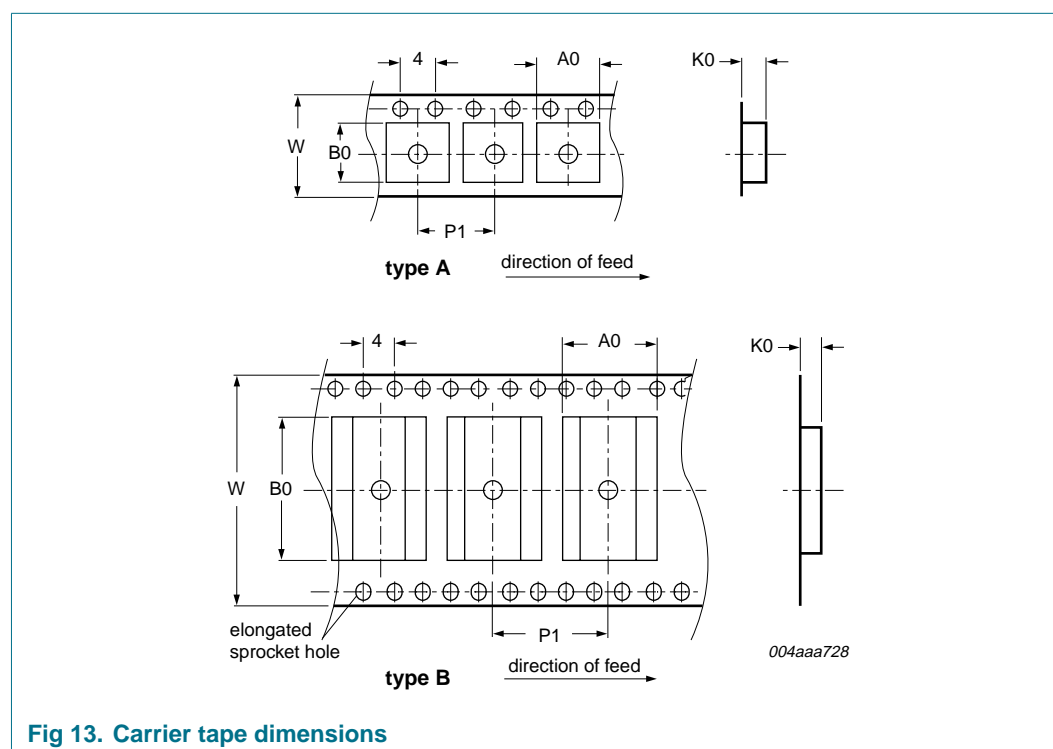


Fig 13. Carrier tape dimensions

Table 14. Type A carrier tape dimensions for the ISP1110VH

Dimension	Value	Unit
A0	3.3	mm
B0	3.3	mm
K0	1.1	mm
P1	8.0	mm
W	12.0 $\pm$ 0.3	mm

## 15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

## 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 14](#)) than a PbSn process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 15](#) and [16](#)

Table 15. SnPb eutectic process (from J-STD-020C)

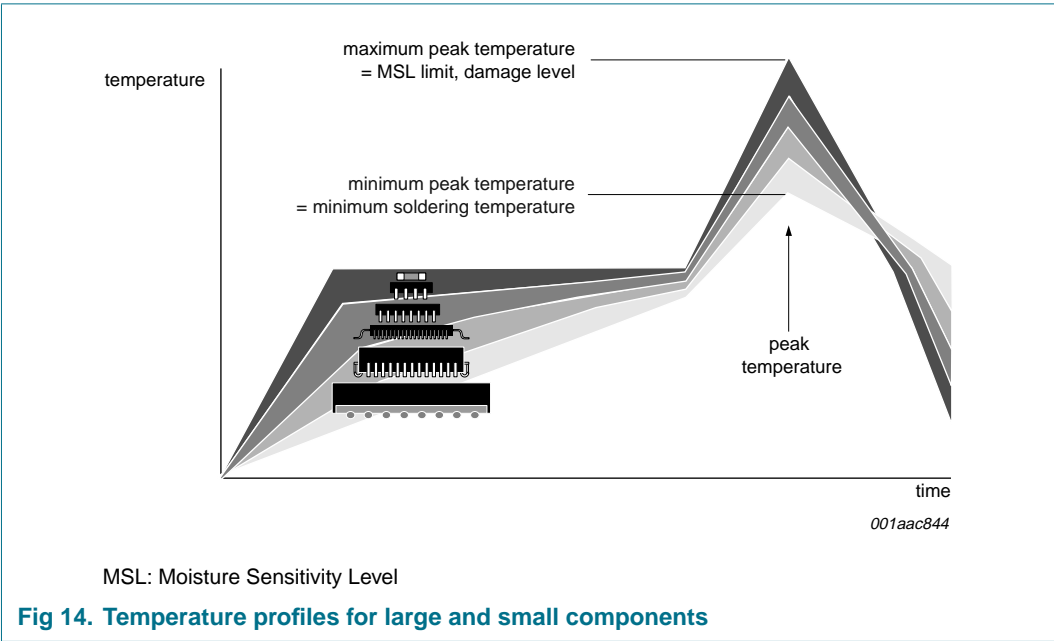
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 14](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

## 16. Abbreviations

Table 17. Abbreviations

Acronym	Description
ASIC	Application Specific Integrated Circuits
ATX	Analog USB Transceiver
CMOS	Complementary Metal-Oxide Semiconductor
HBM	Human Body Model
PDA	Personal Digital Assistant
RXD	Receive Data
SE0	Single-Ended Zero
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

## 17. References

- [1] Universal Serial Bus Specification Rev. 2.0
- [2] ECN\_27%\_Resistor (Pull-up/pull-down Resistors ECN)

## 18. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1110_2	20070319	Product data sheet	-	ISP1110_1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• <a href="#">Table 2 “Pin description”</a>: updated description for pin 6.</li><li>• <a href="#">Section 7.1 “Modes of operation”</a>: updated <a href="#">Table 3</a> and added <a href="#">Table 4</a>.</li><li>• <a href="#">Section 7.1.1 “USB mode”</a>: updated third paragraph.</li><li>• <a href="#">Section 7.1.2 “UART mode”</a>: updated fourth paragraph.</li><li>• <a href="#">Table 9 “Recommended operating conditions”</a>: added T<sub>j</sub>.</li></ul>			
ISP1110_1	20060323	Product data sheet	-	-

## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 19.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 19.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 20. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 21. Tables

Table 1.	Ordering information	2
Table 2.	Pin description	4
Table 3.	Operating modes: definition	6
Table 4.	Pin status in various modes	6
Table 5.	USB function	9
Table 6.	USB driving function (pin OE_N = LOW)	9
Table 7.	USB receiving function (pin OE_N = HIGH)	9
Table 8.	Limiting values	11
Table 9.	Recommended operating conditions	11
Table 10.	Static characteristics: supply pins	11
Table 11.	Static characteristics: digital pins	12
Table 12.	Static characteristics: analog I/O pins DP and DM	13
Table 13.	Dynamic characteristics: analog I/O pins DP and DM	14
Table 14.	Type A carrier tape dimensions for the ISP1110VH	18
Table 15.	SnPb eutectic process (from J-STD-020C)	20
Table 16.	Lead-free process (from J-STD-020C)	20
Table 17.	Abbreviations	21
Table 18.	Revision history	21

continued >>

## 22. Figures

Fig 1.	Block diagram	2
Fig 2.	Pin configuration HBCC16; top view	3
Fig 3.	Pin configuration HBCC16; bottom view	3
Fig 4.	ISP1110 mode detection flowchart	8
Fig 5.	Rise time and fall time	15
Fig 6.	Timing of VPO and VMO to DP and DM	15
Fig 7.	Timing of OE_N to DP and DM	15
Fig 8.	Timing of DP and DM to RCV, VP/VPO and VM/VMO	15
Fig 9.	Load on pins DP and DM	16
Fig 10.	Load on pins DP and DM for enable time and disable time	16
Fig 11.	Load on pins VM/VMO, VP/VPO and RCV	16
Fig 12.	Package outline SOT639-2 (HBCC16)	17
Fig 13.	Carrier tape dimensions	18
Fig 14.	Temperature profiles for large and small components	20

continued >>



## 23. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>2</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Block diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>3</b>
6.1	Pinning .....	3
6.2	Pin description .....	4
<b>7</b>	<b>Functional description</b> .....	<b>6</b>
7.1	Modes of operation .....	6
7.1.1	USB mode .....	6
7.1.2	UART mode .....	7
7.1.3	Mode detection flowchart .....	8
7.1.4	Mode switching time .....	8
7.2	Analog USB Transceiver (ATX) .....	9
7.3	V <sub>BUS</sub> detector .....	10
7.4	DP pull-up resistor .....	10
7.5	DC-DC regulator .....	10
7.6	Power selector .....	10
<b>8</b>	<b>Limiting values</b> .....	<b>11</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>11</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>11</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>14</b>
<b>12</b>	<b>Test information</b> .....	<b>16</b>
<b>13</b>	<b>Package outline</b> .....	<b>17</b>
<b>14</b>	<b>Packing information</b> .....	<b>18</b>
<b>15</b>	<b>Soldering</b> .....	<b>18</b>
15.1	Introduction to soldering .....	19
15.2	Wave and reflow soldering .....	19
15.3	Wave soldering .....	19
15.4	Reflow soldering .....	19
<b>16</b>	<b>Abbreviations</b> .....	<b>21</b>
<b>17</b>	<b>References</b> .....	<b>21</b>
<b>18</b>	<b>Revision history</b> .....	<b>21</b>
<b>19</b>	<b>Legal information</b> .....	<b>22</b>
19.1	Data sheet status .....	22
19.2	Definitions .....	22
19.3	Disclaimers .....	22
19.4	Trademarks .....	22
<b>20</b>	<b>Contact information</b> .....	<b>22</b>
<b>21</b>	<b>Tables</b> .....	<b>23</b>
<b>22</b>	<b>Figures</b> .....	<b>24</b>
<b>23</b>	<b>Contents</b> .....	<b>25</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by

**PHILIPS**

© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 19 March 2007

Document identifier: ISP1110\_2