ISP1107

Advanced Universal Serial Bus transceiver

Rev. 01 — 23 February 2000 Objective specification

1. General description

The ISP1107 is a Universal Serial Bus (USB) transceiver that is fully compliant with the *Universal Serial Bus Specification Rev. 1.1*. It is ideal for portable electronics devices such as mobile phones, digital still cameras and personal digital assistants. It allows 1.8 V, 2.5 V and 3.3 V USB Application Specific ICs (ASICs) and Programmable Logic Devices (PLDs) to interface with the physical layer of the Universal Serial Bus. It has an integrated 5 V to 3.3 V voltage regulator allowing direct powering from the USB supply V_{BUS}.

The ISP1107 can be used as a USB device transceiver or a USB host transceiver. It can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates. The ISP1107 is compatible with the industry-standard Philips Semiconductors USB transceiver PDIUSBP11A.

2. Features

- Complies with *Universal Serial Bus Specification Rev. 1.1*
- Integrated 5 V to 3.3 V voltage regulator allowing direct powering from USB V_{BUS}
- Used as a USB device transceiver or a USB host transceiver
- Supports full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) serial data rates
- Slew-rate controlled differential data driver
- Differential input receiver with wide common-mode range and very high input sensitivity
- Stable RCV output during SE0 condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Three I/O voltage levels: 1.8 V, 2.5 V and 3.3 V
- Backward compatible with PDIUSBP11A
- Higher than 8 kV ESD protection
- Full industrial operating temperature range –40 to +85 °C
- Available in small TSSOP16 and BCC16 packages.

3. Applications

- Portable electronic devices, such as
  - mobile phones
  - digital still cameras
  - personal digital assistants (PDA)
  - Internet appliances (IA).

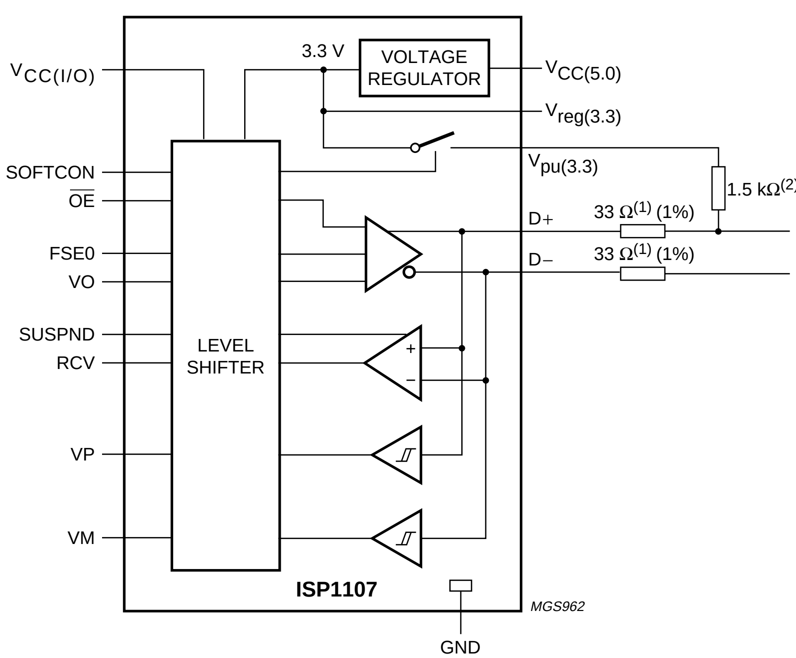
4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1107xx	BCC16 [1]	plastic bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm	SOTxxx
ISP1107DH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] In development.

5. Functional diagram



(1) Use a 39 Ω resistor (1%) for a USB v2.0 compliant output impedance range.

(2) Connect to D– for low-speed operation.

Fig 1. Functional diagram.

6. Pinning information

6.1 Pinning

Fig 2. Pinning diagram BCC16 (to be added).

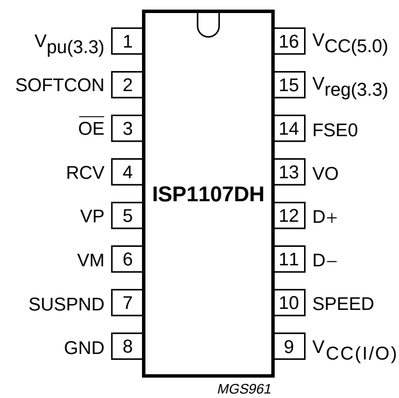


Fig 3. Pinning diagram TSSOP16.

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
$V_{pu(3.3)}$	1	-	pull-up supply voltage (3.3 V ± 10%); used to connect an external 1.5 kΩ resistor on D+ (full-speed) or D– (low-speed); pin function is controlled by input SOFTCON: **SOFTCON = LOW —** $V_{pu(3.3)}$ floating (high impedance) **SOFTCON = HIGH —** $V_{pu(3.3)}$ = 3.3 V
SOFTCON	2	I	software controlled USB connection input; a HIGH level applies 3.3 V to pin $V_{pu(3.3)}$, which is connected to an external 1.5 kΩ pull-up resistor; this allows USB connect/disconnect signalling to be controlled by software
$\overline{OE}$	3	I	output enable input (CMOS level re. $V_{CC(I/O)}$, active LOW); enables the transceiver to transmit data on the USB bus
RCV	4	O	differential data receiver output (CMOS level re. $V_{CC(I/O)}$); driven LOW when input SUSPND is HIGH; the output state of RCV is preserved and stable during an SE0 condition
VP	5	O	single-ended D+ receiver output (CMOS level re. $V_{CC(I/O)}$); used for external detection of single-ended zero (SE0), error conditions, speed of connected device; driven HIGH when $V_{CC(5.0)}$/$V_{reg(3.3)}$ are not connected to any voltage supply
VM	6	O	single-ended D– receiver output (CMOS level re. $V_{CC(I/O)}$); used for external detection of single-ended zero (SE0), error conditions, speed of connected device; driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ or $V_{reg(3.3)}$
SUSPND	7	I	suspend input (CMOS level re. $V_{CC(I/O)}$); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level

Table 2: Pin description*...continued*

Symbol	Pin	Type	Description
GND	8	-	ground supply
$V_{CC(I/O)}$	9	-	supply voltage for digital I/O pins (1.65 to 3.6 V). Three voltage levels are supported: 1.8 V ± 0.15 V, 2.5 V ± 0.2 V and 3.3 V ± 0.3V; when $V_{CC(I/O)}$ is not connected, the D+/D– pins are in three-state
SPEED	10	I	speed selection input (CMOS level re. $V_{CC(I/O)}$); adjusts the slew rate of differential data outputs D+ and D– according to the transmission speed: **LOW:** low-speed (1.5 Mbit/s) **HIGH:** full-speed (12 Mbit/s)
D–	11	AI/O	negative USB data bus connection (analog, differential); for low-speed mode connect to pin $V_{pu(3.3)}$ via a 1.5 kΩ resistor
D+	12	AI/O	positive USB data bus connection (analog, differential); for full-speed mode connect to pin $V_{pu(3.3)}$ via a 1.5 kΩ resistor
VO	13	I	differential driver data input (CMOS level re. $V_{CC(I/O)}$, Schmitt trigger); see Table 4
FSE0	14	I	differential driver data input (CMOS level re. $V_{CC(I/O)}$, Schmitt trigger); see Table 4
$V_{reg(3.3)}$	15	-	regulated supply voltage output (3.0 to 3.6 V) during 5 V operation; used as supply voltage input for 3.3 V operation (3.3 V ± 10%)
$V_{CC(5.0)}$	16	-	supply voltage for 5 V operation (4.0 to 5.5 V); can be connected directly to USB supply V_{BUS}; connect this pin to $V_{reg(3.3)}$ during 3.3 V operation

7. Functional description

7.1 Function selection

Table 3: Function table

SUSPND	$\overline{OE}$	D+/D–	RCV	VP/VM	Function
L	L	driving & receiving	active	active	normal driving (differential receiver active)
L	H	receiving [1]	active	active	receiving
H	L	driving	inactive [2]	active	driving during ‘suspend’ [3] (differential receiver inactive)
H	H	high-Z [1]	inactive [2]	active	low-power state

[1] Signal levels on D+/D– are determined by other USB devices and external pull-up/down resistors.

[2] In ‘suspend’ mode (SUSPND = HIGH) the differential receiver is inactive and output RCV is always LOW. Out-of-suspend (‘K’) signalling is detected via the single-ended receivers VP and VM.

[3] During suspend, the slew-rate control circuit of low-speed operation is disabled. The D+/D– are still driven to their intended states, without slew-rate control. This is permitted because driving during suspend is used to signal remote wakeup by driving a ‘K’ signal (one transition from idle to ‘K’ state) for a period of 1 to 15 ms.

7.2 Operating functions

Table 4: Driving function ($\overline{OE}$ = L)

FSE0	VO	Data
L	L	differential logic 0
L	H	differential logic 1
H	L	SE0
H	H	SE0

Table 5: Receiving function ($\overline{OE}$ = H)

D+/D–	RCV	VP	VM
differential logic 0	L	L	H
differential logic 1	H	H	L
SE0	RCV* [1]	L	L

[1] RCV* denotes the signal level on output RCV just before SE0 state occurs. This level is kept stable during the SE0 period.

7.3 Power supply configurations

The ISP1107 can be used with different power supply configurations, which can be changed dynamically. An overview is given in Table 6.

Normal mode — Both $V_{CC(I/O)}$ and $V_{CC(5.0)}/V_{reg(3.3)}$ are connected. For 5 V operation, $V_{CC(5.0)}$ is connected to a 5 V source (4.0 to 5.5 V). The internal voltage regulator then produces 3.3 V for the USB connections. For 3.3 V operation, both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected to a 3.3 V source (3.0 - 3.6 V). $V_{CC(I/O)}$ is independently connected to a 1.8 V, 2.5 V or 3.3 V source, depending on the supply voltage of the external circuit.

Disable mode — $V_{CC(I/O)}$ is not connected, $V_{CC(5.0)}/V_{reg(3.3)}$ are connected. In this mode, the ISP1107's internal circuits ensure that the D+/D– pins are in three-state and the power consumption drops to the low-power (suspended) state level.

Sharing mode — $V_{CC(I/O)}$ is connected, $V_{CC(5.0)}/V_{reg(3.3)}$ are not connected. In this mode, the D+/D– pins are made three-state and the ISP1107 allows external signals of up to 3.6 V to share the D+/D– lines. The ISP1107's internal circuits ensure that virtually no current is drawn via the D+/D– lines. The power consumption through pin $V_{CC(I/O)}$ drops to the low-power (suspended) state level. Both the VP and VM pins are driven HIGH to indicate this mode.

Table 6: Power supply configuration overview

$V_{CC(5.0)}/V_{reg(3.3)}$	$V_{CC(I/O)}$	Configuration	Special characteristics
connected	connected	Normal mode	-
connected	not connected	Disable mode	D+/D– high impedance
not connected	connected	Sharing mode	D+/D– are high impedance; VP/VM are driven HIGH

8. Limiting values

Table 7: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5.0)}$	supply voltage		–0.5	+6.0	V
$V_{CC(I/O)}$	I/O supply voltage		–0.5	+4.6	V
$V_{reg(3.3)}$	regulated supply voltage		–0.5	+4.6	V
V_I	DC input voltage		–0.5	$V_{CC(I/O)}$ + 0.5	V
$I_{latchup}$	latchup current	V_I = –1.8 to 5.4 V	-	100	mA
V_{esd}	electrostatic discharge voltage [1]	I_{LI} < 1 μA			
		pins D+, D–	-	±8000	V
		other pins	-	±2000	V
T_{stg}	storage temperature		–40	+125	°C

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model).

Table 8: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5.0)}$	supply voltage	5 V operation	4.0	5.0	5.5	V
$V_{CC(I/O)}$	I/O supply voltage		1.65	-	3.6	V
$V_{reg(3.3)}$	regulated supply voltage	3.3 V operation	3.0	3.3	3.6	V
V_I	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{I(AI/O)}$	input voltage on analog I/O pins (D+/D–)		0	-	3.6	V
T_{amb}	operating ambient temperature		–40	-	+85	°C

9. Static characteristics

Table 9: Static characteristics: supply pins

V_{CC} = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{reg(3.3)}$	regulated supply voltage	unloaded		3.0 [1]	3.3	3.6	V
I_{CC}	operating supply current	full-speed transmitting and receiving at 12 Mbit/s; C_L = 50 pF on D+/D−		-	6	10 [2]	mA
$I_{CC(idle)}$	supply current during full-speed idle and SE0	full-speed idle: D+ > 2.7 V, D− < 0.3 V; SE0: D+ < 0.3 V, D− < 0.3 V	[3]	-	-	500	µA
$I_{CC(susp)}$	suspend supply current	SUSPND = HIGH	[3]	-	-	20	µA
$I_{CC(dis)}$	disable mode supply current	$V_{CC(I/O)}$ not connected	[3]	-	-	20	µA
ICC(I/O)	operating I/O supply current	full-speed transmitting and receiving at 12 Mbit/s		-	0.3	1 [2]	mA
$I_{CC(I/O)(static)}$	static I/O supply current	full-speed idle, SE0 or suspend		-	-	10	µA
$I_{CC(I/O)(sharing)}$	sharing mode I/O supply current	$V_{CC(5.0)}$/$V_{reg(3.3)}$ not connected	[3]	-	-	10	µA
$I_{Dx(sharing)}$	sharing mode load current on pins D+ and D−	$V_{CC(5.0)}$/$V_{reg(3.3)}$ not connected; SOFTCON = LOW; V_{Dx} = 3.6 V	[3]	-	-	5	µA

[1] In ‘suspend’ mode, the minimum voltage is 2.7 V.

[2] Characterized only, not tested in production.

[3] Excluding $V_{pu(3.3)}$ source current to 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typ.).

Table 10: Static characteristics: digital pins

V_{CC} = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 to 3.6 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.6V_{CC(I/O)}$	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 4 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	$V_{CC(I/O)} - 0.15$	-	-	V
		I_{OH} = 4 mA	$V_{CC(I/O)} - 0.4$	-	-	V
Leakage current						
I_{LI}	input leakage current		-	-	±1	µA
$V_{CC(I/O)}$ = 1.8 V ± 0.15 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.5	V
V_{IH}	HIGH-level input voltage		1.2	-	-	V

Table 10: Static characteristics: digital pins *...continued*

V_{CC} = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 4 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	1.5	-	-	V
		I_{OH} = 4 mA	1.25	-	-	V
$V_{CC(I/O)}$ = 2.5 V ± 0.2 V)						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.7	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 4 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.15	-	-	V
		I_{OH} = 4 mA	1.9	-	-	V
$V_{CC(I/O)}$ = 3.3 V ± 0.3 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.9	V
V_{IH}	HIGH-level input voltage		2.15	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.2	V
		I_{OL} = 4 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.85	-	-	V
		I_{OH} = 4 mA	2.6	-	-	V

Table 11: Static characteristics: analog I/O pins (D+, D−)

V_{CC} = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
Differential receiver						
V_{DI}	differential input sensitivity	$\lvert V_{I(D+)} - V_{I(D-)} \rvert$	0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range	0.8	-	2.5	V
Single-ended receiver						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
Output levels						
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to + 3.6 V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	2.8	-	3.6	V
Leakage current						
I_{LZ}	OFF-state leakage current		-	-	±1	µA

Table 11: Static characteristics: analog I/O pins (D+, D–)...*continued*

V_{CC} = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Capacitance							
C_{IN}	transceiver capacitance	pin to GND		-	-	20	pF
Resistance							
Z_{DRV}	driver output impedance	steady-state drive	[1]	34	39	44	Ω
Z_{DRV2}	driver output impedance for USB 2.0	steady-state drive	[2]	41	45	49	Ω
Z_{INP}	input impedance			10	-	-	MΩ
R_{SW}	internal switch resistance at pin $V_{pu(3.3)}$			-	-	10	Ω
Termination							
V_{TERM} [3]	termination voltage for upstream port pull-up (R_{PU})			3.0 [4]	-	3.6	V

[1] Includes external resistors of 33 Ω ±1% on both D+ and D–.

[2] Includes external resistors of 39 Ω ±1% on both D+ and D–. This range complies with *Universal Serial Bus Specification Rev. 2.0*.

[3] This voltage is available at pins $V_{reg(3.3)}$ and $V_{pu(3.3)}$.

[4] In ‘suspend’ mode the minimum voltage is 2.7 V.

10. Dynamic characteristics

Table 12: Dynamic characteristics: analog I/O pins (D+, D–) [1]

V_{CC} = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
Full-speed mode							
t_{FR}	rise time	C_L = 50 to 125 pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$; see Figure 4		4	-	20	ns
t_{FF}	fall time	C_L = 50 to 125 pF; 90 to 10% of $\lvert V_{OH} - V_{OL}\rvert$; see Figure 4		4	-	20	ns
FRFM	differential rise/fall time matching (t_{FR}/t_{FF})	excluding the first transition from Idle state		90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state; see Figure 7	[2]	1.3	-	2.0	V
Low-speed mode							
t_{LR}	rise time	C_L = 200 to 600 pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$; see Figure 4		75	-	300	ns
t_{LF}	fall time	C_L = 200 to 600 pF; 90 to 10% of $\lvert V_{OH} - V_{OL}\rvert$; see Figure 4		75	-	300	ns
LRFM	differential rise/fall time matching (t_{LR}/t_{LF})	excluding the first transition from Idle state		80	-	125	%

Table 12: Dynamic characteristics: analog I/O pins (D+, D–) [1] *…continued*

V_{CC} = 4.0 to 5.5 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CRS}	output signal crossover voltage	excluding the first transition from idle state; see Figure 7	[2]	1.3	-	2.0	V
Driver timing							
Full-speed mode							
$t_{PLH(drv)}$	driver propagation delay (VO, FSE0 to D+,D–)	LOW-to-HIGH; see Figure 7		-	-	15	ns
$t_{PHL(drv)}$		HIGH-to-LOW; see Figure 7		-	-	15	ns
t_{PHZ}	driver disable delay ($\overline{OE}$ to D+,D–)	HIGH-to-OFF; see Figure 5		-	-	10	ns
t_{PLZ}		LOW-to-OFF; see Figure 5		-	-	10	ns
t_{PZH}	driver enable delay ($\overline{OE}$ to D+,D–)	OFF-to-HIGH; see Figure 5		-	-	15	ns
t_{PZL}		OFF-to-LOW; see Figure 5		-	-	15	ns
Low-speed mode							
Not specified: low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF}.							
Receiver timings (full-speed and low-speed mode)							
Differential receiver							
$t_{PLH(rcv)}$	propagation delay (D+,D– to RCV)	LOW-to-HIGH; see Figure 6		-	-	15	ns
$t_{PHL(rcv)}$		HIGH-to-LOW; see Figure 6		-	-	15	ns
Single-ended receiver							
$t_{PLH(se)}$	propagation delay (D+,D– to VP, VM)	LOW-to-HIGH; see Figure 6		-	-	15	ns
$t_{PHL(se)}$		HIGH-to-LOW; see Figure 6		-	-	15	ns

[1] Test circuit: see Figure 10.

[2] Characterized only, not tested. Limits guaranteed by design.

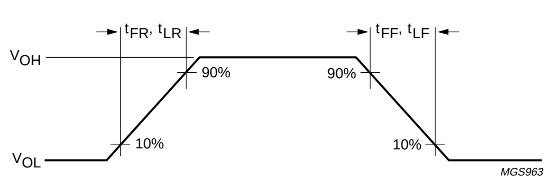


Fig 4. Rise and fall times.

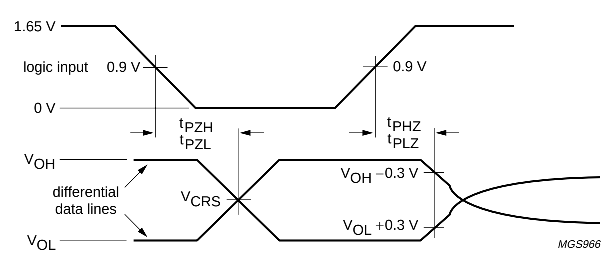


Fig 5. Timing of $\overline{OE}$ to D+, D–.

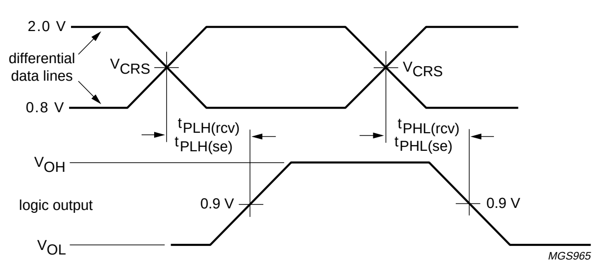


Fig 6. Timing of D+, D– to RCV, VP, VM.

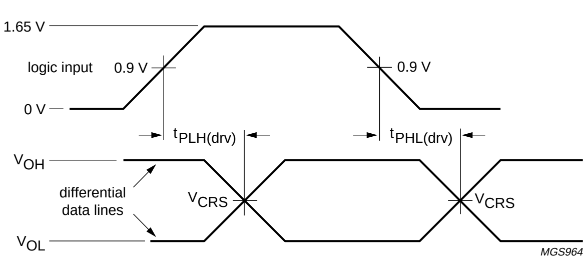
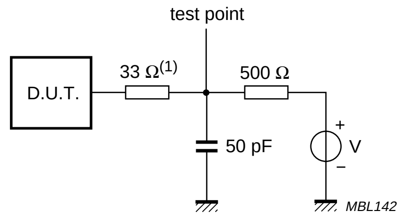


Fig 7. Timing of VO, FSE0 to D+, D–.

11. Test information



V = 0 V for t_{PZH}, t_{PHZ}

V = $V_{reg(/3.3)}$ for t_{PZL}, t_{PLZ}

(1) Complies with USB 1.1. For USB 2.0 a resistor of 39 Ω must be used.

Fig 8. Load for enable and disable times.

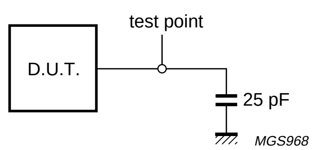
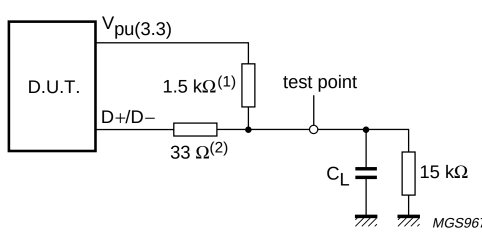


Fig 9. Load for VM, VP and RCV.



Load capacitance:

C_L = 50 pF or 125 pF (full-speed mode, minimum or maximum timing)

C_L = 200 pF or 600 pF (low-speed mode, minimum or maximum timing)

(1) Full-speed mode: connected to D+, low-speed mode: connected to D–.

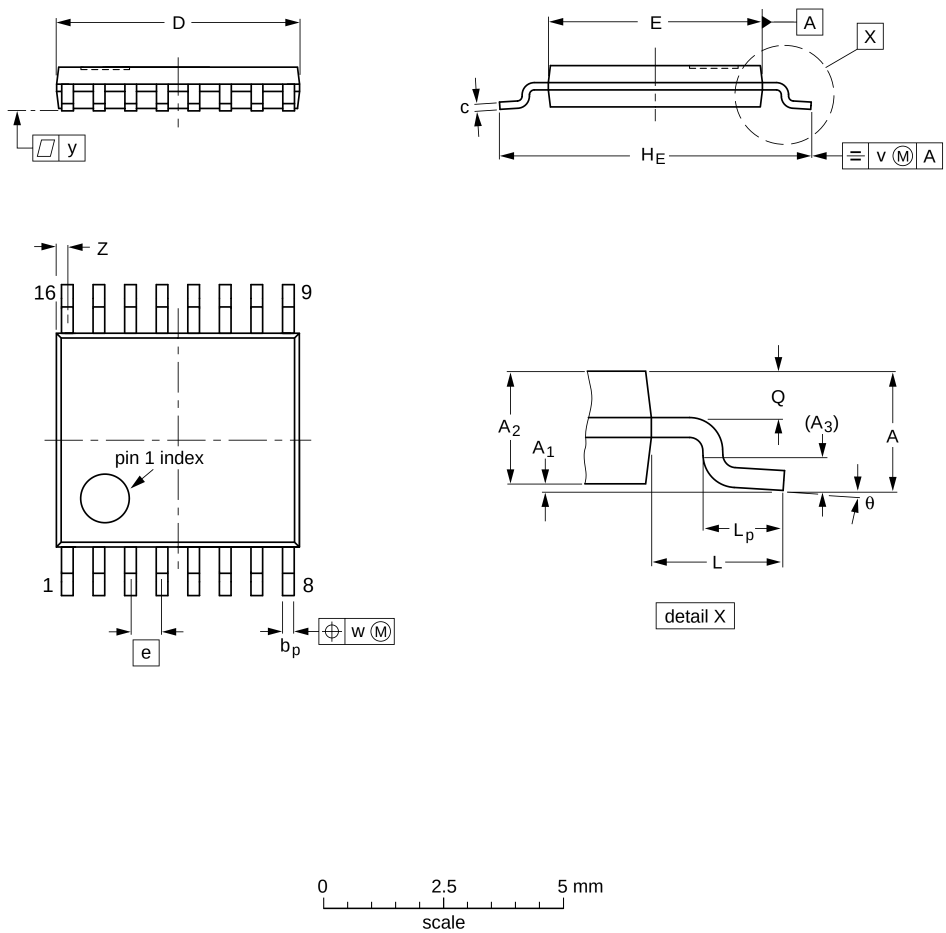
(2) Complies with USB 1.1. For USB 2.0 a resistor of 39 Ω must be used.

Fig 10. Load for D+, D–.

12. Package outline

Fig 11. BCC16 package outline (to be added).

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

Fig 12. TSSOP16 package outline.

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 13: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow [1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable [2]	suitable
PLCC [3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14. Revision history

Table 14: Revision history

Rev	Date	CPCN	Description
01	20000223		Objective specification; initial version.

15. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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