OBSOLETE PRODUCT
RECOMMENDED REPLACEMENT PART
ISL97649AR5566

ISL98665

TFT-LCD Supplies + DVR + V_{COM} Amplifier

FN8564
Rev 0.00
June 27, 2013

The ISL98665 is an integrated power management IC (PMIC) for TFT-LCDs used in notebooks, tablet PCs, and monitors. The device integrates a boost converter for generating AVDD, an LDO for V_{LOGIC}, and a second boost converter for V_{GH}. VGL is generated by a charge pump driven by the switch node of the AVDD boost. The ISL98665 also includes a high performance V_{COM} amplifier and a V_{COM} calibrator, with integrated EEPROM.

The AVDD boost converter features a 2.5A FET with adjustable switching frequency ranging from 310kHz to 1.2MHz. The soft-start time and compensation are adjustable by external components.

V_{GH} boost converter features a 1.2A FET and temperature compensation.

The LDO is able to deliver 360mA for driving the voltage rail required by external digital circuitry.

The ISL98665 provides a 7-bit resolution, current sink V_{COM} calibrator with I^2C interface, and a V_{COM} amplifier. The output of the V_{COM} is powered up with the voltage at the last programmed EEPROM setting.

Features

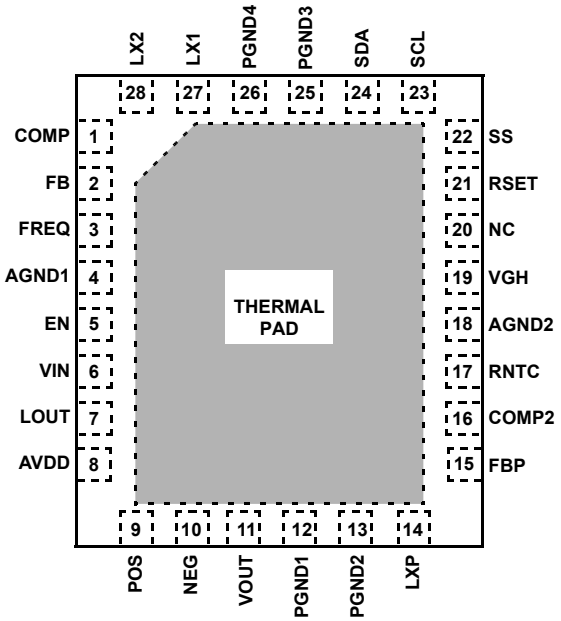
- 2.2V to 5.5V input
- 2.5A, 0.15Ω integrated AVDD boost FET
- 1.2A integrated boost for up to 37.5V V_{GH} with temperature compensation
- LDO able to deliver 360mA
- Adjustable boost switching frequency from 310kHz to 1.2MHz
- Integrated high output current V_{COM} amplifier
- DVR (digital variable resistor)
  - Wiper position stored in 7-bit nonvolatile memory and recalled on power-up
  - Endurance, 1,000 data changes per bit
- UVLO, OVP, OCP, and OTP protection
- 28 Ld, 4x5mm TQFN package
- Pb-Free (RoHS compliant)

Applications

- LCD Notebook, Tablet, and Monitor

Pin Configuration

ISL98665
(28 LD 4x5 TQFN)
TOP VIEW



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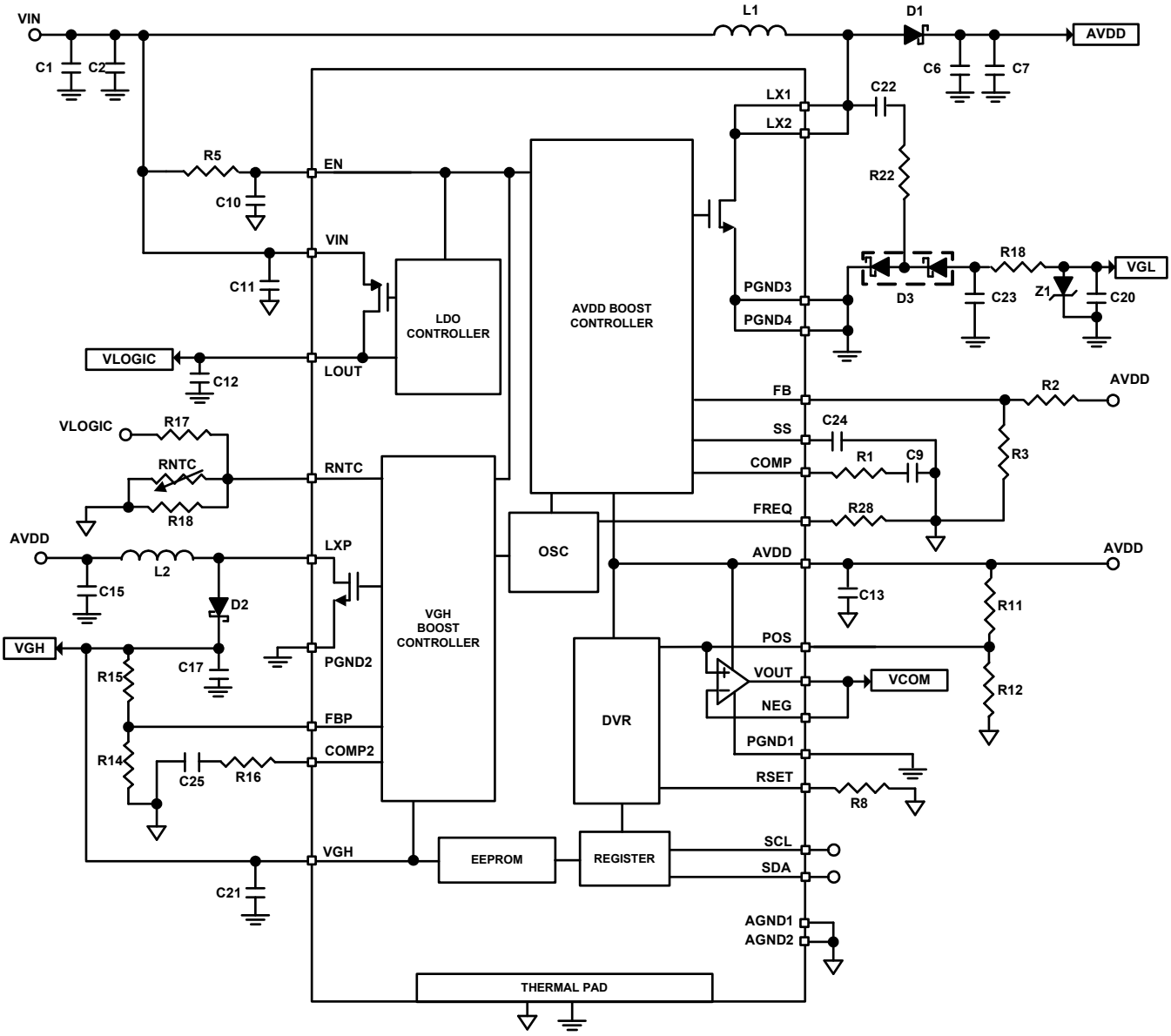
Application/Block Diagram



NOTE: Component designators in this Application Diagram match with the evaluation board schematic.

Pin Descriptions

PIN#	SYMBOL	DESCRIPTION
1	COMP	AVDD boost converter compensation pin. Connect a series resistor and capacitor between this pin and AGND to optimize transient response and stability. For more information refer to “Compensation” on page 12.
2	FB	AVDD boost converter feedback. Connect to the center of a voltage divider between AVDD and AGND to set the AVDD voltage. For more information refer to “AVDD Boost Operation” on page 10.
3	FREQ	Boost Converter frequency adjustment pin. Connect this pin with a resistor to AGND set the boost frequency. Refer to “Switching Frequency Selection” on page 10 for more information.
4	AGND1	Analog ground 1.
5	EN	IC enable pin. Enables all the ISL98665 outputs.
6	VIN	IC input supply and LDO input. Need to connect decoupling capacitor close to VIN pin.
7	LOUT	LDO output. Connect at least one 1µF capacitor to GND for stable operation.
8	AVDD	DVR and V_{COM} amplifier voltage analog supply. Place a 0.47µF capacitor close to the AVDD pin.
9	POS	V_{COM} Amplifier Non-inverting input.
10	NEG	V_{COM} Amplifier Inverting input.
11	VOUT	V_{COM} Amplifier output.
12	PGND1	V_{COM} Amplifier ground.
13	PGND2	VGH power ground.
14	LXP	VGH boost converter switching node.
15	FBP	VGH boost converter feedback. Connect to the center of a voltage divider between VGH and AGND to set the VGH voltage. Refer to “V_{GH} Boost Operation” on page 10 for more information.
16	COMP2	VGH boost converter compensation pin. Connect a series resistor and capacitor between this pin and AGND to optimize transient response and stability. Refer to “Compensation” on page 12 for more information.
17	RNTC	Temperature Compensation pin. Refer to “V_{GH} Temperature Compensation” on page 11 for the connection of this pin.
18	AGND2	Analog ground 2.
19	VGH	Power supply for EEPROM programming; VGH OVP sensing pin.
20	NC	Not connected.
21	RSET	DVR sink current adjustment pin; connect a resistor between this pin and AGND to set the resolution of the DVR output voltage.
22	SS	AVDD Boost Converter Soft-Start. Connect a capacitor between this pin and GND to set the soft-start time. Refer to “Soft-Start” on page 10 for more information.
23	SCL	I^2C clock high impedance input.
24	SDA	I^2C bidirectional data high impedance input/open-drain output.
25, 26	PGND3, PGND4	AVDD boost power ground.
27, 28	LX1, LX2	AVDD boost converter switching node 1 and 2.
	Thermal PAD	Connect to ground plane on PCB to maximize thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL98665IRTZ	98665 IRTZ	-40 to +105	28 Ld 4x5 TQFN	L28.4x5C
ISL98665IRT-EVZ	ISL98665 Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL98665 For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VGH and LXP to AGND . . . . . -0.3V to +45V
LX1, LX2, AVDD, POS, NEG, and VOUT to AGND . . . . . -0.3 to +18V
Voltage Between AGND and PGND. . . . . ±0.5V
All Other Pins to GND . . . . . -0.3 to +6.0V
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2kV
Machine Model (Tested per JESD22-A115-A). 200V
Charged Device Model (Tested per JESD22-C101). 1kV
Latch Up (Tested per JESD78; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld 4x5 TQFN Package (Notes 4, 5). . . .	39	9

Maximum Junction Temperature . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature During Soldering . . . . . +260°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Operating Temperature . . . . . -40°C to +105°C
Supply Voltage
V_{IN} . . . . . 2.2V to 5.5V
AVDD . . . . . Up to 16V
V_{GH} . . . . . Up to 37.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN}= EN = 3.3V, AVDD = 8V, V_{LDO} = 1.89V, V_{GH} = 21V. T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
GENERAL						
V_{IN}	V_{IN} Supply Voltage Range		**2.2**	3.3	**5.5**	V
I_{S_DIS}	V_{IN} Supply Currents when Disabled	V_{IN} < UVLO		390	**500**	µA
I_S	V_{IN} Supply Currents	EN = 3.3V, overdrive AVDD and V_{GH}		1.3	**1.6**	mA
I_{EN}	Enable Pin Current	EN = 3.3V		3		µA
LOGIC INPUT CHARACTERISTICS						
V_{IL}	Low Voltage Threshold	EN, SCL, SDA			**0.60**	V
V_{IH}	High Voltage Threshold	EN, SCL, SDA	**1.2**			V
R_{IL}	Pull-Down Resistor	EN	**0.75**	1.15	**1.55**	MΩ
INTERNAL OSCILLATOR						
F_{OSC}	Switching Frequency	FREQ resistor = 10kΩ	**1.1**	1.2	**1.3**	MHz
		FREQ resistor = 20kΩ	**550**	600	**650**	kHz
AVDD BOOST REGULATOR						
AVDD_RNG	AVDD Output Voltage Range		**1.1*V_{IN}**		**16**	V
DAVDD/ DIOUT	AVDD Load Regulation	10mA < I_{LOAD} < 250mA, T_A = +25°C		0.2		%
DAVDD/ DV_{IN}	AVDD Line Regulation	I_{LOAD} = 150mA, 2.2V < V_{IN} < 5.5V, T_A = +25°C		0.2		%
V_{FB}	AVDD Feedback Voltage	I_{LOAD} = 100mA	**1.188**	1.200	**1.212**	V
I_{FB}	Input Bias Current	FB pin			**200**	nA
$r_{DS(ON)\_AVDD}$	Switch ON-resistance			150	**190**	mΩ
I_{LIM_AVDD}	Switch Current Limit		**2.0**	2.5	**3.0**	A

Electrical Specifications V_{IN}= EN = 3.3V, AVDD = 8V, V_{LDO} = 1.89V, V_{GH} = 21V. T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
$AVDD\_D_{MAX}$	Max Duty Cycle	FREQ = 600kHz	**88**	93		%
V_{GH} BOOST REGULATOR						
V_{GH} _RNG	V_{GH} Output Voltage Range		**1.1* AVDD**		**37.5**	V
I_{LIM_VGH}	V_{GH} Switch Current Limit		**0.8**	1.2	**1.6**	A
DV_{GH}/DI_{OUT}	Load Regulation	2mA < I_{LOAD} < 50mA, T_A = +25°C		0.2		%
DV_{GH}/DV_{IN}	Line Regulation	2.2V < V_{IN} < 5.5V, I_{LOAD} = 5mA, T_A = +25°C		0.2		%
$r_{DS(ON)\_VGH}$	V_{GH} Boost Switch ON Resistance			0.6	**0.8**	Ω
$V_{GH}\_D_{MAX}$	Maximum Duty Cycle	FREQ = 600kHz	**90**	94		%
I_{FBP}	Input Bias Current	FBP Pin			**200**	nA
V_{FBP}	V_{GH} Feedback Voltage	VRNTC < 0.608V, V_{GH} < 37.5V	**0.592**	0.608	**0.622**	V
		VRNTC > 1.215V, V_{GH}< 37.5V	**1.188**	1.215	**1.239**	V
		0.608V < VRNTC < 1.215V, V_{GH}< 37.5V		VRNTC		V
Hys_TCOMP	Temperature Compensation Hysteresis			20		mV
I_{RNTC}	RNTC Current				**200**	nA
LDO REGULATOR						
DV_{LDO}/DV_{IN}	Line Regulation	I_{LOAD} = 1mA, 2.2V < V_{IN} < 5.5V, T_A = +25°C		0.3		%
DV_{LDO}/DI_{OUT}	Load Regulation	1mA < I_{LOAD} < 300mA, T_A = +25°C		0.3		%
V_{DO}	Dropout Voltage	V_{IN} = 2.2V, I_{LOAD} = 250mA		200	**300**	mV
I_{LIM_LDO}	Current Limit	Output drops by 5%	**250**	360		mA
V_{LDO}	LDO Output Voltage	I_{LOAD} = 50mA, T_A = +25°C		1.89		V
V_{COM} AMPLIFIER						
I_{S_com}	V_{COM} Block Supply Current	AVDD = 8V		0.7	**1.35**	mA
V_{OS}	Offset Voltage	V_{POS} = V_{NEG} = 0.5*AVDD			**±15**	mV
I_L	Input Leakage Current	V_{POS} = V_{NEG} = 0.5*AVDD		0	**±1**	µA
CMIR	Common Mode Input Voltage Range		**0**		**AVDD**	V
CMRR	Common-Mode Rejection Ratio	V_{POS} = V_{NEG} from 2V to 6V	**60**	75		dB
PSRR	Power Supply Rejection Ratio	8V < AVDD < 12V V_{POS} = V_{NEG} = 0.5*AVDD	**70**	85		dB
V_{OH}	Output Voltage Swing High	I_{OUT} (source) = 0.1mA	**AVDD - 0.015**	AVDD - 0.005		V
		I_{OUT} (source) = 75mA	**AVDD - 1.74**	AVDD - 1.28		V
V_{OL}	Output Voltage Swing Low	I_{OUT} (sink) = 0.1mA		GND + 0.001	**GND + 0.006**	V
		I_{OUT} (sink) = 75mA		GND + 0.94	**GND + 1.4**	V

Electrical Specifications V_{IN}= EN = 3.3V, AVDD = 8V, V_{LDO} = 1.89V, V_{GH} = 21V. T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
I_{SC}	Output Short Circuit Current	V_{OUT} = AVDD, V_{OUT} shorted to GND (Sourcing)	**135**	180		mA
		V_{OUT} = GND, V_{OUT} shorted to AVDD (Sinking)	**170**	220		mA
SR	Slew Rate	Rising, 0.5V ≤ V_{OUT} ≤ +5.5V, R_L = 10kΩ || C_L = 10pF to AGND		35		V/µs
		Falling, +5.5V ≥ V_{OUT} ≥ 0.5V, R_L = 10kΩ || C_L = 10pF to AGND		35		
BW	Bandwidth (-3dB)	A_V ± 1, R_L = 10kΩ || C_L = 10pF to AGND		20		MHz
V_{COM} CALIBRATOR (DVR)						
$RSET_{VR}$	RSET Voltage Resolution	(Note 7)		7		Bits
$RSET_{DNL}$	RSET Differential Nonlinearity	T_A = +25°C, (Note 8)			±1	LSB
$RSET_{ZSE}$	RSET Zero-Scale Error	T_A = +25°C, (Note 8)			±2	LSB
$RSET_{FSE}$	RSET Full-Scale Error	T_A = +25°C, (Note 8)			±8	LSB
I_{RSET}	RSET Current Capability		**105**			µA
AVDD to RSET	AVDD to RSET Voltage Attenuation			1.20		V/V
FAULT DETECTION THRESHOLD						
V_{UVLO}	Undervoltage Lock out Threshold	V_{IN} rising	**1.85**	2.0	**2.15**	V
		Hysteresis		0.2		V
OVP_{AVDD}	AVDD Boost Overvoltage Protection	AVDD rising (Note 9)	**15.4**	15.9	**16.4**	V
		Hysteresis		1.3		V
OVP_{VGH}	V_{GH} Boost Overvoltage Protection	V_{GH} rising	**38**	39	**40**	V
T_{OFF}	Thermal Shutdown all Channels	Temperature rising		150		°C
		Hysteresis		40		°C
POWER SEQUENCE						
$t_{ss}V_{LOGIC}$	V_{LOGIC} Soft-start Time			0.45		ms
I_{ss}	AVDD Boost Soft-start Current at Start-Up			4		µA
V_{ss}	Soft-Start Voltage	End of soft-start ramp		1		V
$t_{delay}V_{GH}$	Delay from AVDD start-up finish to V_{GH} Start	V_{GH} = 37.5V		2.5		ms
$t_{ss}V_{GH}$	V_{GH} Soft-Start Time	V_{GH} = 37.5V		33		ms
EEPROM						
	EEPROM Endurance	T_A = +25°C,		1		kCyc
	EEPROM Retention	T_A = +25°C,		88		kHrs

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Established by design. Not a parametric spec.
8. Compliance to limits is assured by characterization and design.
9. Boost will stop switching as soon as boost output reaches OVP threshold.

Typical Performance Curves

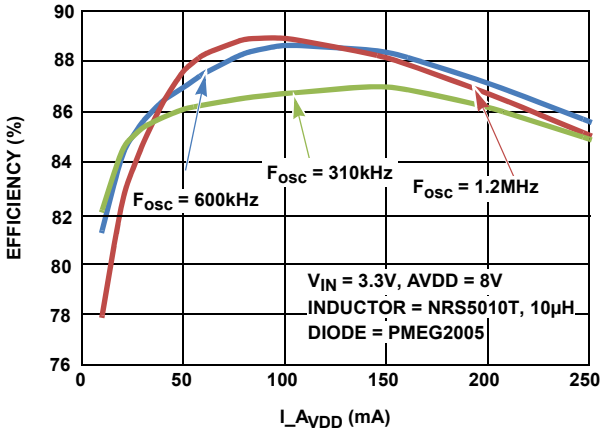


FIGURE 1. AVDD EFFICIENCY vs I_A_{VDD}

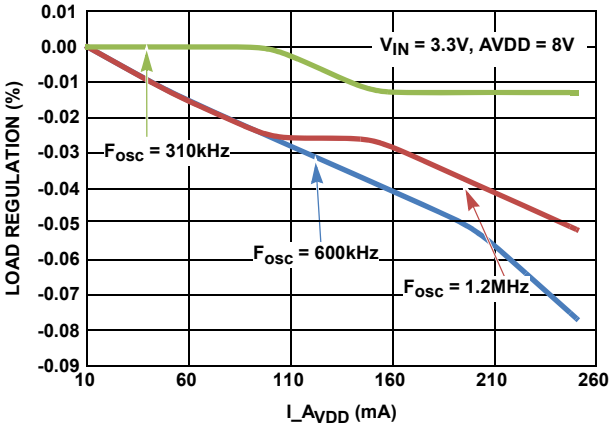


FIGURE 2. AVDD LOAD REGULATION

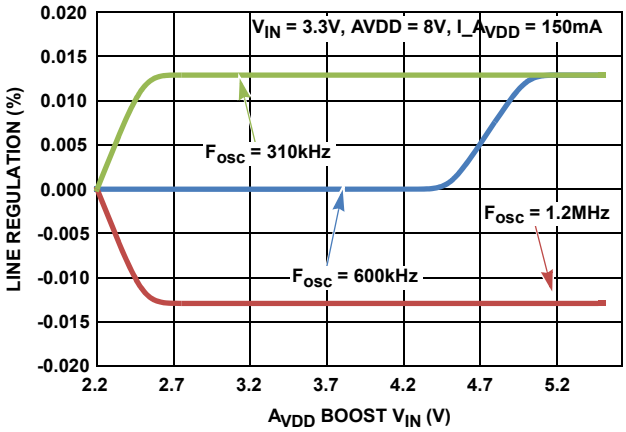


FIGURE 3. AVDD LINE REGULATION

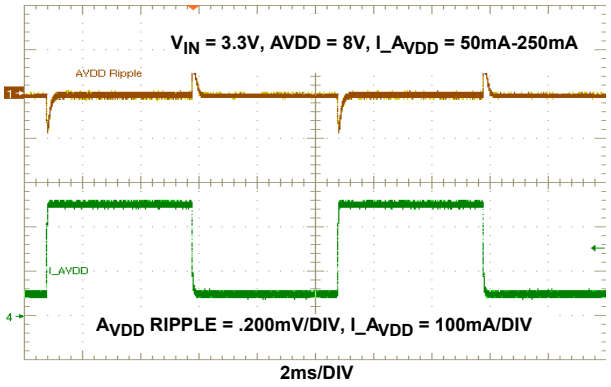


FIGURE 4. AVDD TRANSIENT RESPONSE

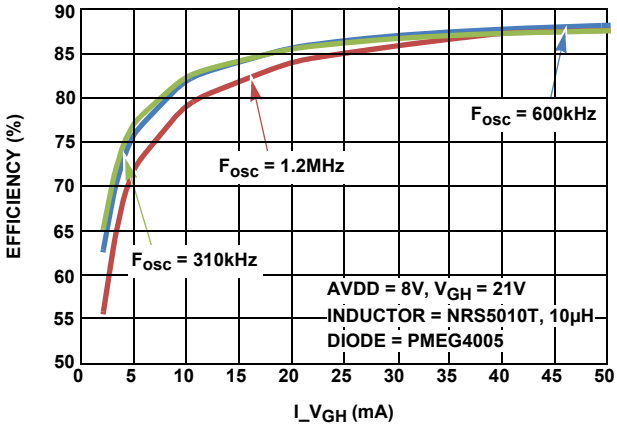


FIGURE 5. V_{GH} EFFICIENCY vs I_V_{GH}

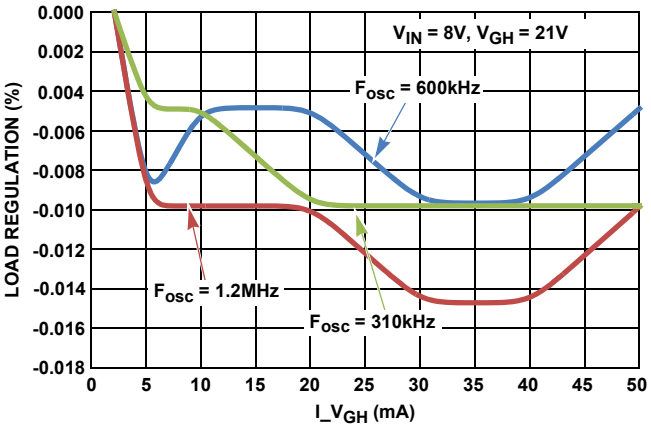


FIGURE 6. V_{GH} LOAD REGULATION

Typical Performance Curves (Continued)

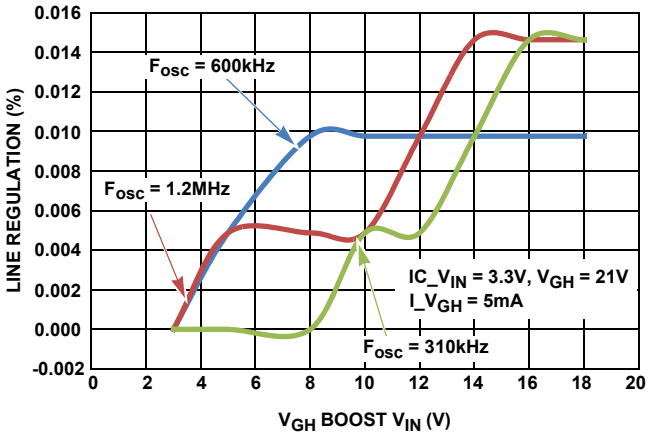


FIGURE 7. V_{GH} LINE REGULATION

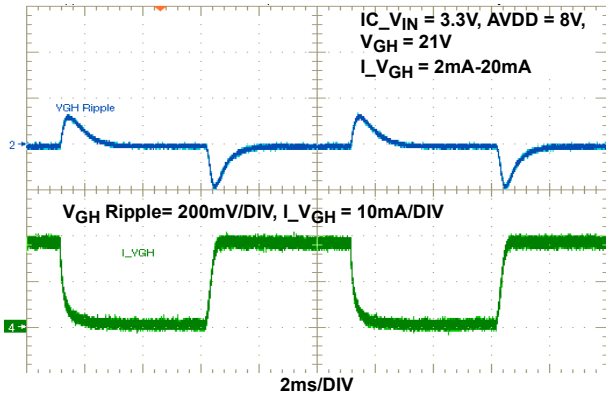


FIGURE 8. V_{GH} TRANSIENT RESPONSE

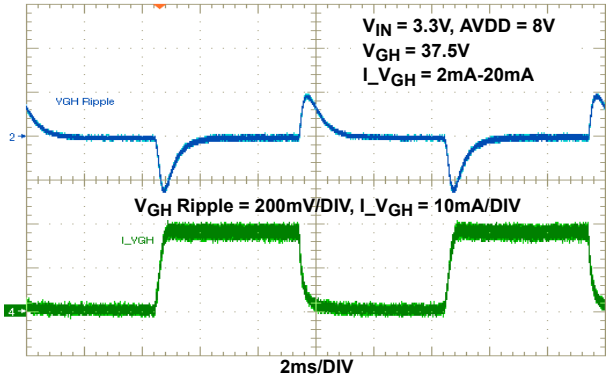


FIGURE 9. V_{GH} TRANSIENT RESPONSE

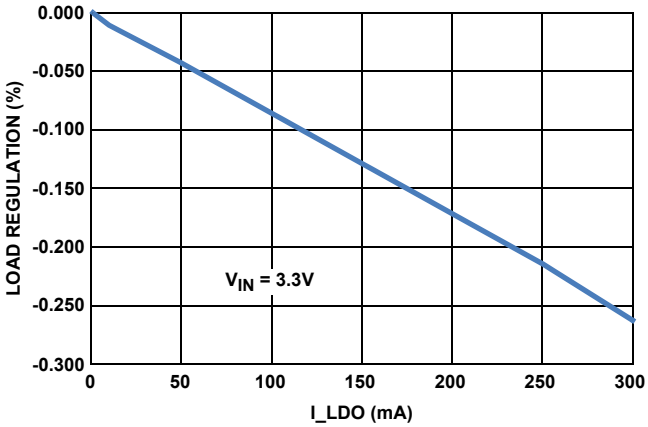


FIGURE 10. L_{DO} LOAD REGULATION

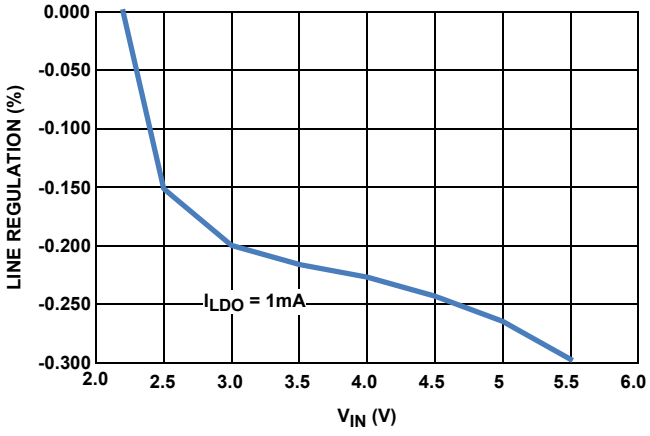


FIGURE 11. L_{DO} LINE REGULATION

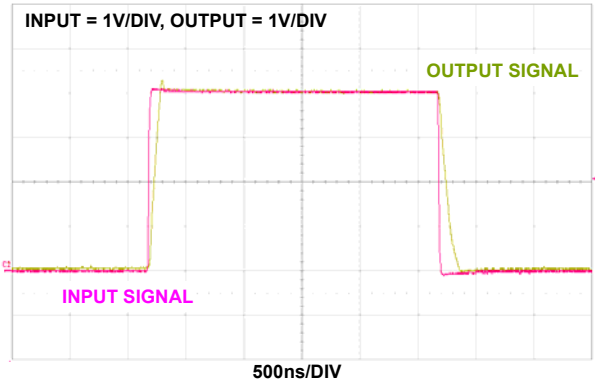


FIGURE 12. V_{COM} LARGE SIGNAL TRANSIENT RESPONSE

Applications Information

Enable Control

The ISL98665 is enabled when the EN pin voltage is high and V_{IN} is above rising UVLO. All output channels in ISL98665 are shut down when the enable pin is pulled down.

Switching Frequency Selection

The ISL98665 switching frequency can be adjusted from 310kHz to 1.2MHz by connecting a resistor between FREQ pin and AGND. A lower switching frequency reduces power dissipation at very light load conditions but more easily allows discontinuous conduction mode. Higher switching frequency allows for smaller external components - inductor and output capacitors. Higher switching frequency will get higher efficiency for a given V_{IN} and loading range, depending on V_{IN}, V_{OUT} and external components, as shown in Figure 1.

The calculation of the switching frequency is shown in Equation 1

$$f_{SW} = \frac{(1.14 \times 10^{10})}{R_{FSW}} \quad \text{(EQ. 1)}$$

f_{SW} is the desired boost switching frequency, and R_{FSW} is the setting resistor (see R_8 in Application Diagram on page 3).

Figure 13 shows the relationship between the switching frequency and the frequency setting resistance.

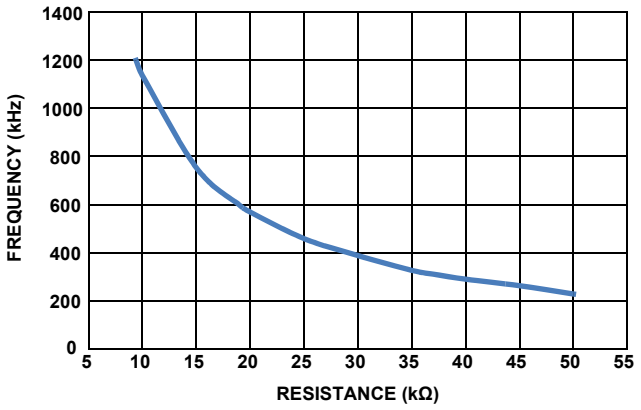


FIGURE 13. A_{VDD} SWITCHING FREQUENCY vs RESISTANCE

AVDD Boost Operation

The AVDD boost converter is a current mode PWM converter operating at frequency ranging from 310kHz or 1.2MHz. It can operate in both discontinuous conduction mode (DCM) at light load and continuous conduction mode (CCM). In continuous conduction mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 2:

$$\frac{V_{AVDD}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 2)}$$

D is the duty cycle of the switching MOSFET.

The boost regulator uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle-by-cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by Equation 3:

$$V_{AVDD} = \frac{R_2 + R_3}{R_3} \times V_{FB} \quad \text{(EQ. 3)}$$

R_2 and R_3 are the feedback resistor values as shown in the "Application/Block Diagram" on page 3.

The current through the MOSFET is limited to 2.5A peak.

This restricts the maximum output current (average) based on Equation 4:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \text{xEff} \quad \text{(EQ. 4)}$$

Eff is the efficiency of the AVDD boost converter, ΔI_L is the peak-to-peak inductor ripple current, and is set by Equation 5:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_{SW}} \quad \text{(EQ. 5)}$$

where f_{SW} is the switching frequency.

SOFT-START

The soft-start is provided by an internal current source of 4µA to charge the external soft-start capacitor. The ISL98665 ramps up the current limit from 0A up to the full value, as the voltage at the SS pin ramps from 0V to 1V. Hence, the soft-start time shown in Figure 24 on page 21 is 5.5ms when the soft-start capacitor is 22nF, and 11.8ms for 47nF.

V_{GH} Boost Operation

The VGH boost converter is a current mode PWM converter operating at frequency ranging from 310kHz or 1.2MHz, which is the same with AVDD boost switching frequency. It can operate in both discontinuous conduction mode (DCM) at light load and continuous conduction mode (CCM) at heavy load.

The VGH boost regulator uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle-by-cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for

noise being coupled into the feedback pin. The boost converter output voltage is determined by Equation 6:

$$V_{GH} = \frac{R_{14} + R_{15}}{R_{14}} \times V_{FBP} \quad \text{(EQ. 6)}$$

Where R_{14} and R_{15} are feedback resistors as shown in the "Application/Block Diagram" on page 3

The current through the MOSFET is limited to 1.2A peak.

In continuous conduction mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 7:

$$\frac{V_{GH}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 7)}$$

where D is the duty cycle of the switching MOSFET, V_{IN} is the input voltage of V_{GH} boost. In most applications, V_{IN} of the V_{GH} boost converter is connected to the AVDD.

For most of the applications, the V_{GH} boost converter operates in discontinuous conduction mode. The operation of boost converter in DCM is much more complicated than in CCM. The voltage conversion ratio is now a function not only of the duty cycle D, but also of the boost inductance, the switching frequency and the loading. In DCM, the voltage conversion ratio is given by Equation 8.

$$\frac{V_{GH}}{V_{IN}} = 1 + \frac{V_{IN} \times D^2}{I_{OUT} \times 2 \times L \times f_s} \quad \text{(EQ. 8)}$$

where f_S is the switching frequency, V_{IN} is the input voltage of V_{GH} boost, I_{OUT} is the loading of V_{GH} boost converter.

V_{GH} TEMPERATURE COMPENSATION

Temperature compensation is integrated in ISL98665 to adjust V_{GH} output voltage in order to compensate the amorphous silicon (a-Si) shift register driving capability over temperature.

A voltage divider with a NTC thermistor between AVDD and ground should be used to determine the RNTC voltage, as shown in Figure 14. R_{17} and R_{18} can be adjusted to select the temperature range, based on the selection of the NTC thermistor.

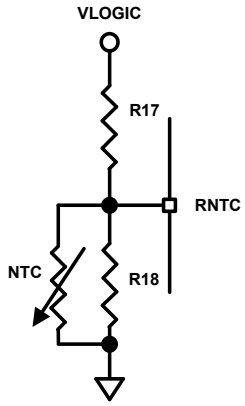


FIGURE 14. RNTC CIRCUIT

The V_{GH} feedback voltage (thus V_{GH} output voltage) is adjusted by the RNTC voltage, which is varied by the NTC thermistor resistance at different temperature, as shown in Figure 15. When the V_{GH} voltage is below the OVP threshold, if RNTC voltage is below 0.608V at higher temperature, the V_{GH} feedback voltage is fixed at 0.608V. If RNTC voltage is above 1.215V at lower temperature, the V_{GH} feedback voltage is fixed at 1.215V. If RNTC voltage is between 0.608V and 1.215V, the V_{GH} feedback voltage follows RNTC voltage. Once V_{GH} output voltage is above OVP threshold, the V_{GH} output voltage will be regulated at 37.5V no matter what RNTC voltage is.

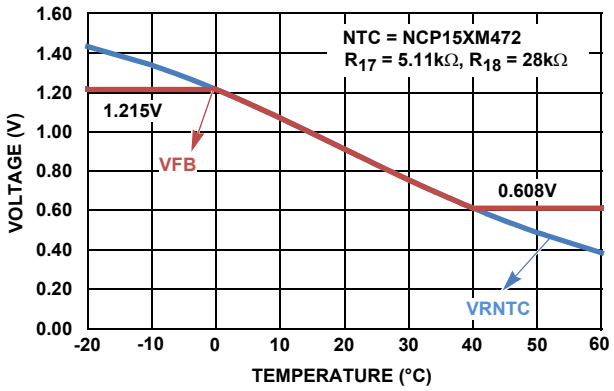


FIGURE 15. VFBP/VRNTC vs TEMPERATURE

NOTES:

10. Above FBP vs Temperature curve is only true when V_{GH} = VFBP*(RU+RL) / RL < OVP where RU is the upper resistance (R_{15} in "Application/Block Diagram" on page 3) and RL is the lower resistance (R_{14} in Application Diagram on page 3) in the FBP resistor ladder from V_{GH} to AGND.
11. When V_{GH} reach OVP, V_{GH} boost regulates at 37.5V, regardless RNTC voltage.

Boost Component Selection

INPUT CAPACITOR

An input capacitor is used to suppress the voltage ripple injected into the boost converter. A ceramic capacitor is recommended. The voltage rating of the input capacitor should be larger than the maximum input voltage. Some input capacitors are recommended in Table 1.

TABLE 1. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
10µF/10V	0603	TDK	C1608X5R1A106M
10µF/16V	0805	TDK	C2012X5R1C106k/0.85

INDUCTOR

The boost inductor is a critical part that influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are used to match the internal slope compensation. If boost converter operates in CCM, the inductor must be able to handle the following average and peak currents shown in Equations 9 and 10:

$$I_{LAVG} = \frac{I_{OUT}}{Eff} x \frac{VOUT}{V_{IN}} \quad \text{(EQ. 9)}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 10)}$$

Where ΔI_L can be calculated using Equation 5.

If boost converter operates in DCM, the inductor must be able to handle the following average and peak currents shown in Equations 11 and 12:

$$I_{LAVG} = \frac{I_{OUT}}{Eff} x \frac{VGH}{V_{IN}} \quad \text{(EQ. 11)}$$

$$I_{LPK} = \frac{V_{IN}}{L} \times \frac{D}{f_s} \quad \text{(EQ. 12)}$$

Some inductors are recommended in Table 2 for different design considerations.

RECTIFIER DIODE

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements. Table 3 shows some recommendations for boost converter diode.

TABLE 2. BOOST CONVERTER INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	MFG	PART NUMBER	NOTE
10µH/ 4Apeak	8.3x8.3x4.5	Sumida	CDRH8D43-100NC	Efficiency Optimization
6.8µH/ 1.8Apeak	5.0x5.0x2.0	TDK	PLF5020T-6R8M1R8	
10µH/ 0.9A	5.0x5.0x1.0	Taiyo Yuden	NRS5010T100MMGF	PCB space/profile optimization

TABLE 3. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	MFG
AVDD			
PMEG2010ER	20V/1A	SOD123W	NXP
MSS1P2U	20V/1A	MicroSMP	VISHAY
V_{GH}			
BAS52-02V	45V/0.75A	SOD523F	INFINEON
DB2J501	50V/0.2A	SOD323	PANASONIC

OUTPUT CAPACITOR

The output capacitor supplies current to the load during transient conditions directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components:

1. The voltage drop due to the inductor ripple current flowing through the ESR of the output capacitor.
2. Charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_s} \quad \text{(EQ. 13)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in Equation 13 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

It is recommended to use one or two 10µF X5R 25V or equivalent ceramic output capacitors for AVDD boost output and 4.7µF X5R 50V or equivalent ceramic output capacitors for V_{GH} boost output.

Table 4 shows some selections of output capacitors.

TABLE 4. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
AVDD			
4.7µF/25V	0805	TDK	C2012X5R1E475K
10µF/25V	0805	Murata	GRM21BR61E106KA73L
V_{GH}			
4.7µF/50V	0805	TDK	C2012X5R1H475M
1µF/50V	0603	TDK	CGA3E3X5R1H105K

COMPENSATION

The boost converters of the ISL98665 can be compensated by an RC network connected from the COMP pins to ground. For AVDD, 15nF and 5.5k RC network is used in the demo board. For V_{GH}, 15nF and 28k RC network is used in the demo board. The larger value resistor and lower value capacitor can lower the transient overshoot, however, at the expense of the stability of the loop.

Linear Regulator (LDO)

The ISL98665 includes an LDO with fixed output voltage of 1.89V. It can supply current up to 350mA.

The efficiency of the LDO depends on the difference between input voltage and output voltage (Equation 14) by assuming LDO quiescent current is much lower than LDO output current:

$$\eta(\%) = \left(\frac{V_{LDO\_IN}}{V_{LDO\_OUT}}\right) \times 100\% \quad \text{(EQ. 14)}$$

The less difference between input and output voltage, the higher efficiency it is.

Ceramic capacitors are recommended for the LDO input and output capacitors. An output capacitor within the 1µF to 4.7µF range is recommended. Larger capacitors help to reduce noise and deviation during transient load change. Some capacitors are recommended in Table 5.

TABLE 5. LDO OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
1µF/10V	0603	TDK	C1608X7R1A105K
1µF/6.3V	0603	MURATA	GRM188R70J105K
2.2µF/6.3V	0603	TDK	C1608X7R0J225K

V_{COM} Amplifier

The V_{COM} amplifier is designed to control the voltage on the back plane of an LCD display. This plane is capacitively coupled to the pixel drive voltage, which alternately cycles positive and negative at the line rate for the display. Thus, the amplifier must be capable of sourcing and sinking pulses of current, which can occasionally be quite large (in the range of 100mA for typical applications).

The ISL98665 V_{COM} amplifier is capable of rail-to-rail output swings and can drive wide range of capacitive loads. As load capacitance increases, the -3dB bandwidth of the device will decrease and the peaking will increase. When driving large capacitive loads, an isolation resistor (typically between 1Ω and 10Ω) should be placed in series with the output.

The positive input of the V_{COM} amplifier (POS) is controlled by the DVR DAC. However, if the DVR DAC calibration function is not required, the V_{COM} amplifier can be used as an independent operational amplifier. Leave the RSET pin floating to disable the DVR DAC function.

I^2C Serial Interface

The ISL98665 uses a standard I^2C interface bus for communication. The two-wire interface links a Master(s) and uniquely addressable Slave devices. The DVR of the ISL98665 operates as a slave device in all applications. The Master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line and the serial data (bi-directional) is on the SDA line. The ISL98665 supports clock rates up to 400kHz (Fast-Mode), and is backwards compatible with standard 100kHz clock rates (Standard-mode).

The SDA and SCL lines must be HIGH when the bus is not in use. An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) is required for SDA and SCL.

The ISL98665 meets standard I^2C timing and interface specifications, see Table 6 and Figure 16, which show the standard timing definitions and specifications for I^2C communication.

TABLE 6. I^2C TIMING AND INTERFACE SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
f_{SCL}	SCL Frequency			**400**	kHz
t_{iN}	Pulse Width Suppression Time at SDA and SCL Inputs			**50**	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid			480	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	480			ns
t_{LOW}	Clock LOW Time	480			ns
t_{HIGH}	Clock HIGH Time	400			ns
$t_{SU:STA}$	START Condition Set-up Time	480			ns
$t_{HD:STA}$	START Condition Hold Time	400			ns
$t_{SU:DAT}$	Input Data Set-up Time	40			ns
$t_{HD:DAT}$	Input Data Hold Time	0			ns
$t_{SU:STO}$	STOP Condition Set-up Time	400			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	400			ns
t_{Wp}	Non-Volatile Write Cycle Time		25		ms
C_{SCL}	Capacitive on SCL		5		pF
C_{SDA}	Capacitive on SDA		5		pF

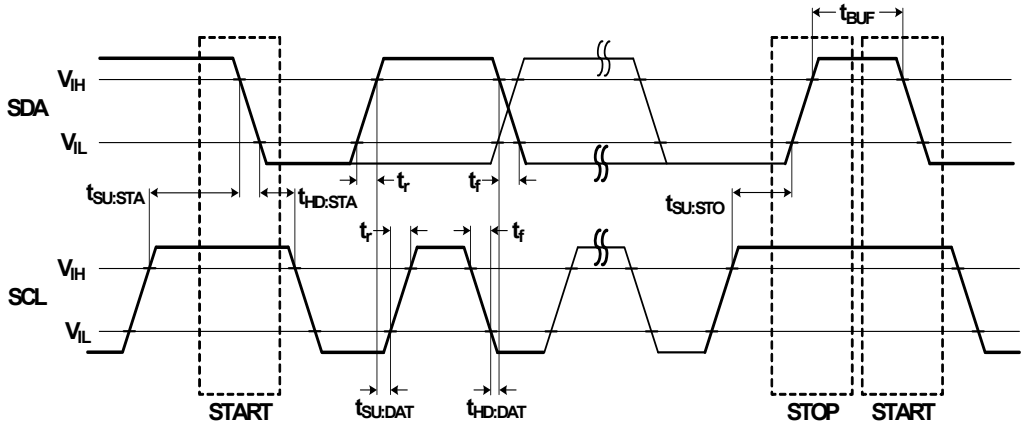


FIGURE 16. I^2C TIMING DEFINITION

PROTOCOL CONVENTIONS

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 16). On power-up of the ISL98665, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of the SDA while SCL is HIGH. The DVR continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 16). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All the I^2C interface must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is high (see Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile write byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 17).

The ISL98665 DVR responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL98665 also respond with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 28h as the seven MSBs. The LSB is in the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation (see Table 7).

TABLE 7. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	R/$\overline{W}$
(MSB)							(LSB)

WRITE OPERATION

A write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition (see Figure 17). After each of the three bytes, the ISL98665 responds with an ACK. When the Write transaction is completed, the Master should generate a STOP condition.

A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers.

During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. The Data Byte is transferred to the WR or to the ACR respectively, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte.

READ OPERATION

A read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/W bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/W bit set to "1". After each of the three bytes, the ISL98665 responds with an ACK; then the ISL98665 transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte.

ISL98665 DVR Memory Description

The ISL98665 contains one non-volatile byte known as the Initial Value Register (IVR). It is accessed by the I^2C interface at Address 00h. The IVR contains the value that is loaded into the Volatile Wiper Register (WR) at power-up.

The volatile WR, and the non-volatile IVR of the DVR are accessed with the same address 00h.

The Access Control Register (ACR) determines which byte at address 00h is accessed (IVR or WR). The volatile ACR must be set as follows:

When the ACR is 00h, which is the default at power-up:

- A read operation to address 00h outputs the value of the non-volatile IVR.
- A write operation to address 00h writes the identical values to the WR and IVR of the DVR.

When the ACR is 80h:

- A read operation to address 00h outputs the value of the volatile WR.
- A write operation to address 00h only writes to the volatile WR.

It is not possible to write to the IVR without writing the same value to the WR.

00h and 80h are the only values that should be written to address 02h. All other values are reserved and must not be written to address 02h.

TABLE 8. REGISTER MAP

ADDRESS (HEX)	NON-VOLATILE	VOLATILE
02	-	ACR
01	Reserved	
00	IVR	WR

NOTE: WR: Wiper Register, IVR: Initial value Register.

Register Description: Access Control

The Access Control Register (ACR) is volatile and is at address 02h. The MSB of ACR decides which byte is accessed at register 00h as shown in the following. All other bits of ACR should be zero (0).

- 00h = Nonvolatile IVR
- 80h = Volatile WR

All other bits of he ACR should be written 0 or 1. Power-up default for this address is 00h.

Register Description: IVR and WR

The output of the DVR is controlled directly by the WR. Writes and reads can be made directly to this register to control and monitor without any non-volatile memory changes. This is done by setting address 02h to data 80h, then writing the data.

The non-volatile IVR stores the power-up value of the DVR output. On power -up, the contents of the IVR are transferred to the WR.

To write to the IVR, first address 02h is set to data 00h, then the data is written. Writing a new value to the IVR register will set a new power- up position for the wiper. Also, writing to this register will load the same value into the WR as the IVR. Therefore, if a new value is loaded into the IVR, not only will the non-volatile IVR change, but the WR will also contain the same value after the write, and the wiper position will change. Reading from the IVR will not change the WR, if its contents are different.

Figure 20 gives examples to show writing to IVR/WR and reading from IVR/WR.

Note: If the Data Byte is to be written only to WR, when the Write transaction is completed, the device enters its standby state. If the Data Byte is to be written also to non-volatile memory (IVR), when the Write transaction is completed, the ISL98665 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL98665 enters its standby state.

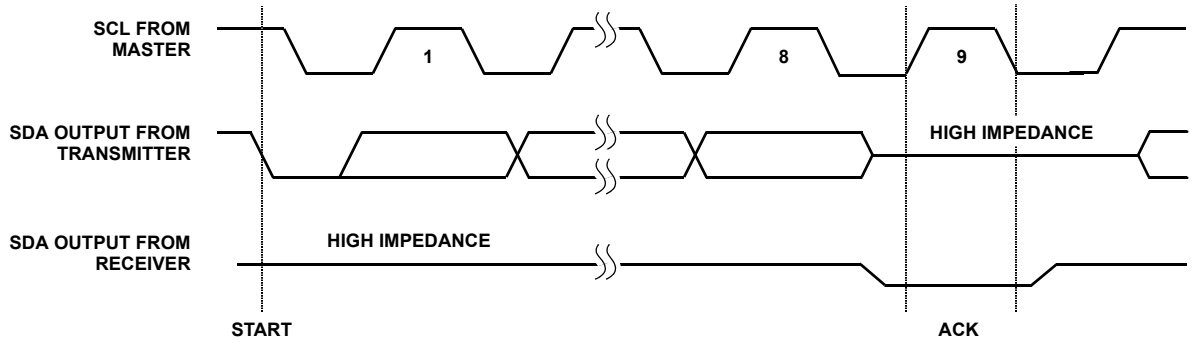


FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER

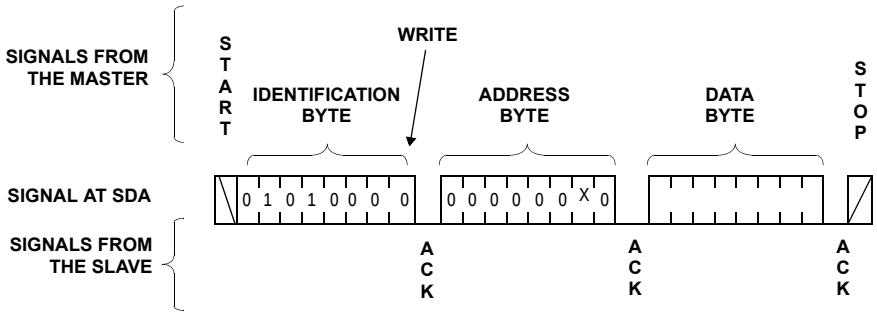


FIGURE 18. BYTE WRITE SEQUENCE

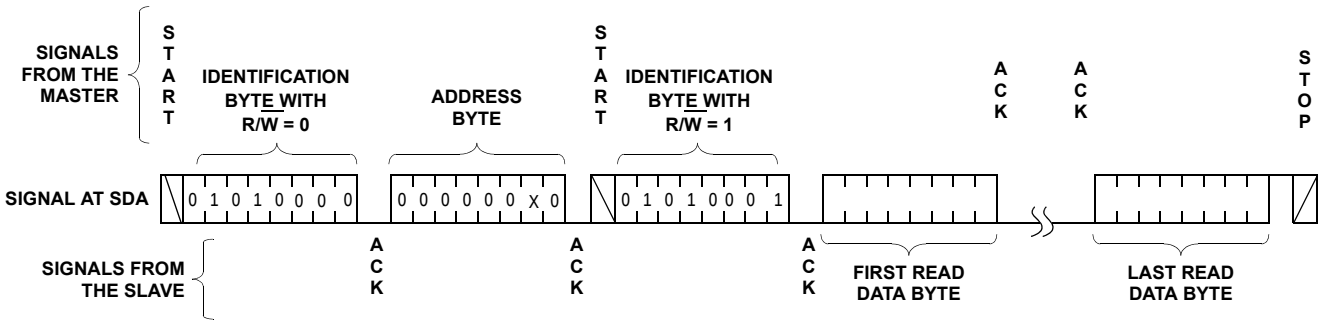


FIGURE 19. READ SEQUENCE

Writing a new value to the IVR
Write to ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A

Then, write to IVR

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	0	D7	D6	D5	D4	D3	D2	D1	A

Note that the WR will also reflect this new value since both registers get writen at the same time
D1:LSB, D7:MSB

Writing a new value to WR only
Write to ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A

Then, write to WR

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	0	D7	D6	D5	D4	D3	D2	D1	A

Note that the IVR value will NOT change
D1:LSB, D7:MSB

Reading from IVR
Write to the ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A

Then set the IVR address

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A

Read from the IVR

	0	1	0	1	0	0	0	1	A	0	D7	D6	D5	D4	D3	D2	D1	

Example 2
Reading from the WR
Write to the ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A

Then set the WR address

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A

Read from the WR

	0	1	0	1	0	0	0	1	A	0	D7	D6	D5	D4	D3	D2	D1	

FIGURE 20. EXAMPLE OF WRITE AND READ SEQUENCE FOR V_{COM} AMPLIFIER

Initial V_{COM} Setting

The ISL98665 provides the ability to reduce the flicker of a TFT-LCD panel during panel production test and alignment. It offers an I^2C programmable adjustment, which can be used to set the panel V_{COM} voltage. The device has a 128-step "digital variable resistor" (DVR) control that adjusts an internal voltage that ultimately controls the sink current (ISET) output of the DVR_OUT node. The DVR_OUT pin is connected to an external voltage divider so that the device will have the capability to scale the voltage by increasing the DVR_OUT sink-current. The resistor on the SET pin (R_{SET}) determines the maximum (full scale) allowable sink-current, which determines the adjustment resolution (step size), as shown in Figure 21.

Note: That R_1 in Figure 21 corresponds to R_{11} in the "Application/Block Diagram" on page 3. The R_2 in Figure 21 corresponds to R_{12} in the "Application/Block Diagram" on page 3.

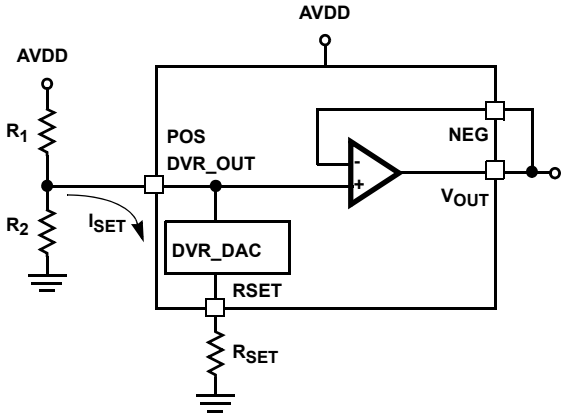


FIGURE 21. DVR_OUTPUT CIRCUIT CONNECTION EXAMPLE

Figure 22, shows the relationship between the 7-bit DVR DAC register value and the DVR's tap position. The taps are generated from a resistor string between AVDD and GND.

Note: That a register value of 0 register value of 0 selects the first step of the resistor string. The output voltage of the internal DVR string is given in Equation 15.

$$V_{DVR} = \left(\frac{127 - RegisterValue}{128}\right)\left(\frac{A_{VDD}}{20}\right) \quad \text{(EQ. 15)}$$

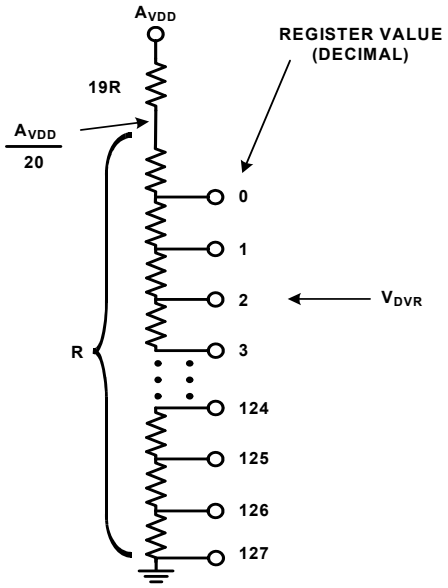


FIGURE 22. DVR DAC - SIMPLIFIED SCHEMATIC

Figure 23, shows the schematic of the DVR_OUT current sink. The combination of amplifier A1, transistor Q1, and resistor R_{SET} forms a voltage-controlled current source, with the voltage determined by the DVR setting.

The initial register value is at 64d by default. The WR value is set back to 64d if any error occurs during I^2C read or write communication. When writing to the EEPROM, V_{GH} needs to be higher than 12V when AVDD is 8V. Outside these conditions, writing operations may not to be successful.

The external R_{SET} resistor sets the full-scale (maximum) sink current that can be pulled from the DVR_OUT node (I_{SET}). The I_{SET} can be up to 105µA maximum (this limit is set by the size of the internal metal interconnects). The relationship between the I_{SET} and the register value is shown in Equation 16.

$$I_{SET} = \frac{V_{DVR}}{R_{SET}} = \left(\frac{127 - RegisterValue}{128}\right)\left(\frac{A_{VDD}}{20}\right)\left(\frac{1}{R_{SET}}\right) \quad \text{(EQ. 16)}$$

The maximum value of I_{SET} can be calculated by substituting the maximum register value of 0 into Equation 16, resulting in Equation 17:

$$I_{SET}(MAX) = \frac{127}{128} \times \frac{A_{VDD}}{20R_{SET}} \quad \text{(EQ. 17)}$$

Equation 15 can also be used to calculate the unit sink current step size per Register Code, resulting in Equation 18:

$$I_{STEP} = \frac{A_{VDD}}{(128)(20)(R_{SET})} \quad \text{(EQ. 18)}$$

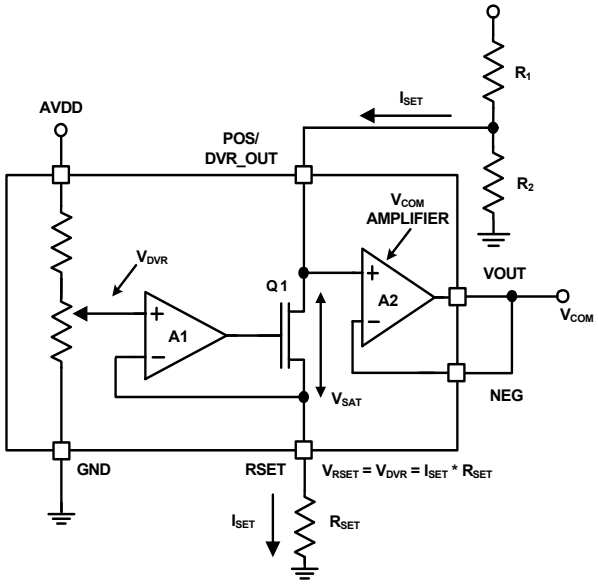


FIGURE 23. DVR CURRENT SINK CIRCUIT

DETERMINATION OF R_{SET}

The ultimate goal for the DVR DAC is to generate an adjustable voltage between two endpoints, V_{COM_MIN} and V_{COM_MAX}, with a fixed power supply voltage, AVDD. This is accomplished by choosing the correct values for R_{SET}, R_1 and R_2. The exact value of R_{SET} is not critical. R_{SET} values range from 3kΩ to more than 100kΩ will work under most conditions. Equation 17 can be used to calculate the minimum value R_{SET}. Larger R_{SET} values reduce quiescent power, since R_1 and R_2 are proportional to R_{SET}.

Equation 19 limits the minimum value for R_{SET}, which is based on the 105µA maximum output current sink.

$$R_{SET} > \frac{AVDD}{(20 \times 105)\mu A} \quad \text{(EQ. 19)}$$

DETERMINATION OF R_1 AND R_2

With AVDD, $V_{COM\ (MIN)}$ and $V_{COM\ (MAX)}$ known and R_{SET} chosen per the above requirements, R_1 and R_2 can be determined using Equations 20 and 21:

$$R_1 = 20.16 \cdot R_{SET}\left(\frac{V_{COM(MAX)} - V_{COM(MIN)}}{V_{COM(MAX)}}\right) \quad \text{(EQ. 20)}$$

$$R_2 = 20.16 \cdot R_{SET}\left(\frac{V_{COM(MAX)} - V_{COM(MIN)}}{A_{VDD} - V_{COM(MAX)}}\right) \quad \text{(EQ. 21)}$$

FINAL TRANSFER FUNCTION FOR DVR

The voltage at POS/DVR_OUT can be calculated from Equation 22:

$$V_{DVROUT} = A_{VDD}\left(\frac{R_2}{R_1+R_2}\right)\left(1-\frac{127-RegisterValue}{128}\left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 22)}$$

With amplifier A2 (V_{COM} Amplifier) in the unity-gain configuration (V_{OUT} tied to NEG as shown in Figure 23), then POS = NEG = V_{OUT}.

Note: There can be a minor variance between POS and V_{OUT} voltages due to the V_{COM} amplifier offset, refer to the V_{COM} amplifier "V_{OS}" specification in the "Electrical Specifications Table" on page 6.

VGL Charge Pump

An external charge pump driven by the AVDD boost switching node can be used to generate VGL, as shown on the "Application/Block Diagram" on page 3.

The number of the charge pump stages can be calculated using Equation 23.

$$VGL_{HEADROOM} = NxAVDD - 2xNxV_d - |VGL| > 0 \quad \text{(EQ. 23)}$$

Where N is the number of the charge pump stages, V_d is the forward voltage drop of one Schottky diode used in the charge pump. V_d is varied with forward current and ambient temperature, so it should be the maximum value in the datasheet of the diode chosen according to max forward current and lowest temperature in the application condition.

Once the number of the charge pump stages is determined, the maximum current that the charge pump can deliver can be calculated using Equation 24:

$$VGL = Nx\left(-AVDD + 2xV_d + \frac{|I_{VGL}|}{(f_{SW}xC_{fly})}\right) \quad \text{(EQ. 24)}$$

Where f_{SW} is the switching frequency of the AVDD boost, C_{fly} is the flying capacitance (C22 in "Application/Block Diagram" on page 3). I_{VGL} is the loading of VGL.

Fault Protection

OVERCURRENT PROTECTION (OCP)

The boost overcurrent protection limits the boost MOSFET current on a cycle-by-cycle basis. When the MOSFET current reaches the current limit threshold, the current PWM switching cycle is terminated and the MOSFET is turned off for the remainder of that cycle. Overcurrent protection does not disable any of the regulators. Once the fault is removed (MOSFET current falls below current limit), the IC will continue with normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

If the input voltage (V_{IN}) falls below the falling UVLO, all the channels will be disabled. All the rails will restart with normal soft-start operation when the V_{IN} input voltage is applied again (V_{IN} > rising UVLO). Refer to the "Electrical Specifications Table" on page 5 for the UVLO specifications.

OVERVOLTAGE PROTECTION (OVP)

The AVDD boost overvoltage protection monitors the AVDD voltage through AVDD pin. When the AVDD pin voltage exceeds the OVP level, the AVDD boost converter stops switching. No other channel faults out when AVDD OVP happens.

The V_{GH} boost overvoltage protection monitors the V_{GH} voltage through the VGH pin. When the VGH pin voltage exceeds the OVP level, the V_{GH} boost converter regulates the output voltage at 37.5V. No other channel faults out when V_{GH} OVP happens.

OVER-TEMPERATURE PROTECTION (OTP)

The ISL98665 has a hysteretic over-temperature protection threshold set at +150°C (typ). If this threshold is reached, all the channels are disabled immediately. When temperature falls by +40°C (typ) then all the regulators automatically re-start.

Power On/OFF Sequence

When V_{IN} rising exceeds rising UVLO and EN is high, V_{LOGIC} starts up with a 0.45ms soft-start time. AVDD boost converter also starts up. The soft-start time of AVDD depends on the capacitance on the SS pin. The 2.5ms after AVDD soft-start is completed, the VGH boost converter starts up. The typical soft-start time of V_{GH} is 33ms. At power off, when V_{IN} reaches falling UVLO, all channels shut down. The detailed power on/off sequence is shown in Figure 24.

Layout Recommendation

The device's performance, including efficiency, output noise, transient response and control loop stability, is affected by the PCB layout. The PCB layout is critical, especially at high switching frequency.

Following are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and thick as possible to minimize parasitic inductance and resistance.
2. The input bypass capacitor should be connected to the VIN pin with the smallest trace possible.
3. Loops with large AC amplitudes and fast slew rate should be made as small as possible.
4. The feedback network should sense the output voltage directly from the point of load. Minimize feedback track lengths to avoid switching noise pick-up.
5. Digital input pins and EN, should be isolated from the high di/dt and dv/dt signals. Otherwise, it may cause a glitch on those inputs.
6. I^2C signals, if not used, should be tied to V_{IN}.
7. Analog ground (AGND) and power ground (PGND) should be separated on PCB. The AGND is a quite ground plane with no large currents flowing through it for all the low-current sensitive analog and digital signals. The compensation and feedback components, soft start capacitors and bias input bypass capacitors need to be connected to AGND. AGND should be on a clearer layer and kept away from the noise. The PGND plane carries high currents, all the power components should be connected to PGND. AGND and PGND should be connected to each other on the PCB at a single point. It is crucial to connect these two grounds at the location very close to the IC.
8. The power ground (PGND) should be connected at the ISL98665 exposed die plate area.
9. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air. A demo board is available to illustrate the proper layout implementation.

Power-ON/OFF Sequence

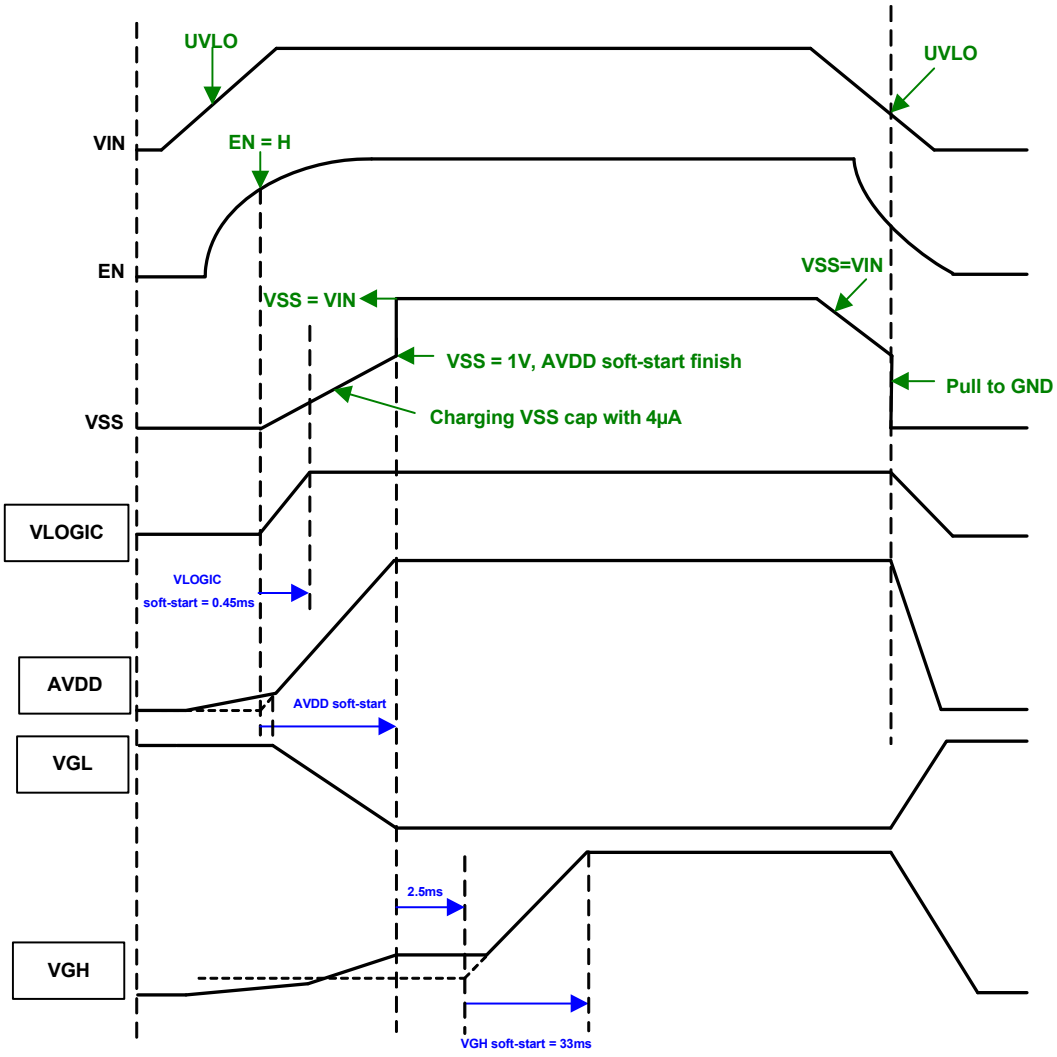


FIGURE 24. POWER-ON/OFF SEQUENCE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 27, 2013	FN8564.0	Initial Release

About Intersil

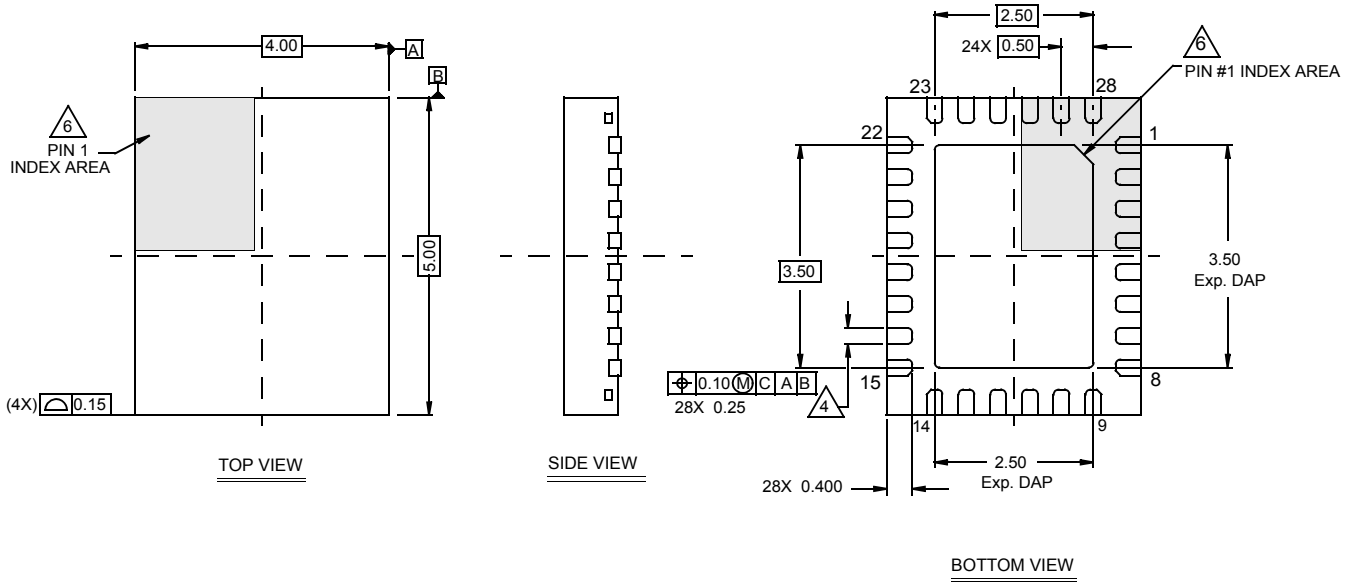
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

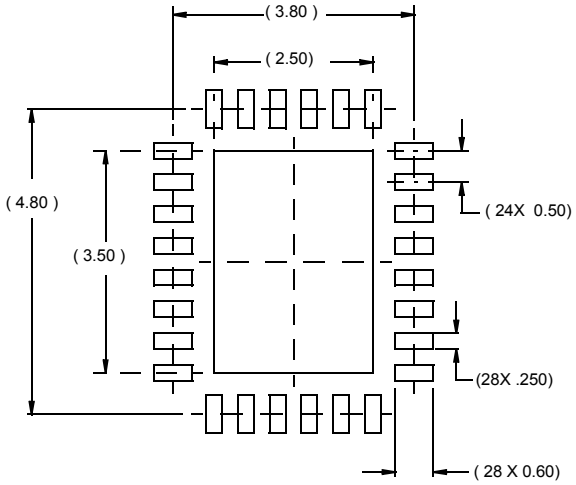
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

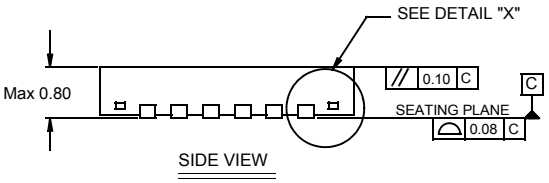
Package Outline Drawing

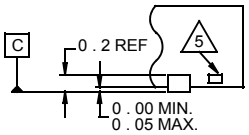
L28.4x5C

28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 9/08









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.