

Multi-Cell Li-ion Battery Pack OCP/Analog Front-End

The ISL94200 is an overcurrent protection device and analog front end for a microcontroller in a multi-cell Li-ion battery pack. The ISL94200 supports battery pack configurations consisting of 4-cells to 7-cells in series and 1 or more cells in parallel. The ISL94200 provides integral overcurrent protection circuitry, short circuit protection, an internal 3.3V voltage regulator, cell voltage monitor level shifters, and drive circuitry for external FET devices for control of pack charge and discharge.

Selectable overcurrent and short circuit thresholds reside in internal RAM registers. An external microcontroller sets the thresholds by setting register values through an I²C serial interface. Internal registers also contain the detection delays for overcurrent and short circuit conditions.

Using an internal analog multiplexer the ISL94200 provides monitoring of each cell voltage plus internal and external temperature by a separate microcontroller with an A/D converter. Software on this microcontroller implements all battery pack control functionality, except for overcurrent and short circuit shutdown.

Applications

- Power Tools
- Battery Backup Systems
- E-Bikes
- Portable Test Equipment
- Medical Systems
- Hybrid Vehicle
- Military Electronics

Ordering Information

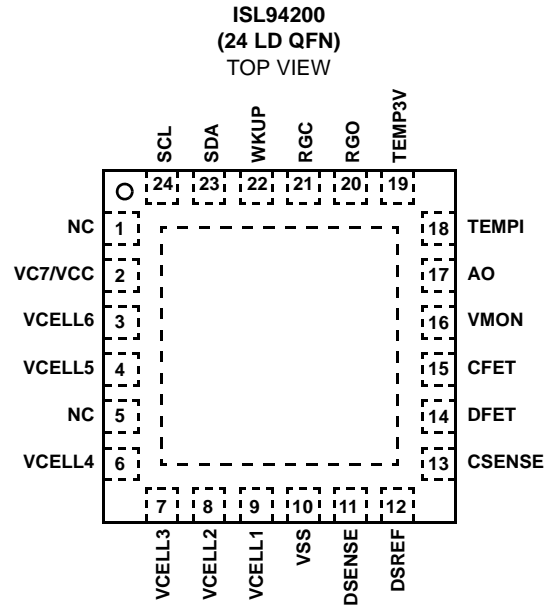
PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL94200IRZ	942 00IRTZ	24 Ld 4x4 QFN	L24.4x4D

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

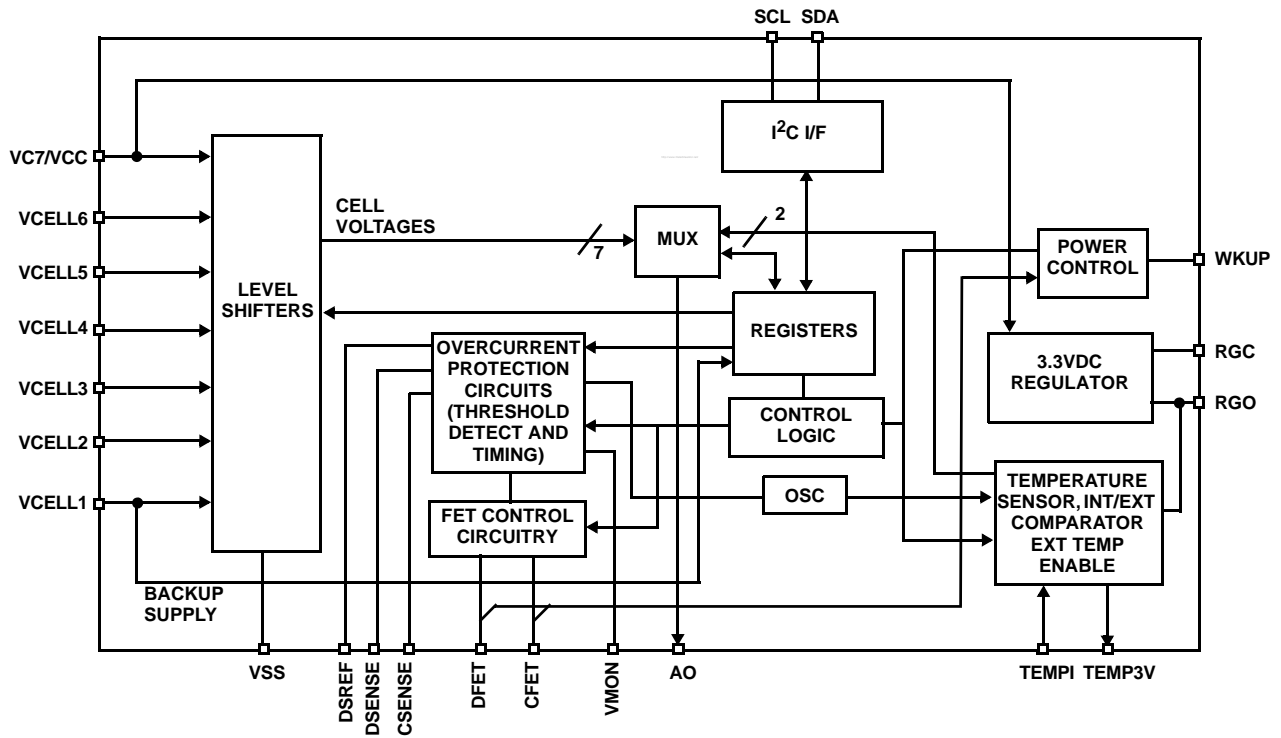
Features

- Software Selectable Overcurrent Protection Levels and Variable Protect Detection Times
 - 4 Discharge Overcurrent Thresholds
 - 4 Short Circuit Thresholds
 - 4 Charge Overcurrent Thresholds
 - 8 Overcurrent Delay Times (Charge)
 - 8 Overcurrent Delay Times (Discharge)
 - 2 Short Circuit Delay Times (Discharge)
- Automatic FET Turn-Off On Reaching External (Battery) or Internal (IC) Temperature Limit
- Fast Short Circuit Pack Shutdown
- Can Use Current Sense Resistor, FET $r_{DS(ON)}$, or Sense FET for Overcurrent Detection
- Four Battery-Backed Software Controlled Flags
- Allows Three Different FET Controls:
 - Back-to-Back N-Channel FETs for Charge and Discharge Control
 - Single N-Channel Discharge FET
 - Single N-Channel FET for Discharge With Separate Optional (Smaller) Back-to-Back N-Channel FETs for Charge
- Integrated Charge/Discharge FET Drive Circuitry With 130 μ A (Typ) Turn-On Current and 180mA (Typ) Discharge FET Turn-Off Current
- 10% Accurate 3.3V Voltage Regulator (Minimum 25mA Out With External NPN Transistor Having Current Gain Of 70)
- Monitored Cell Voltage Output Stable in 100 μ s
- Simple I²C Host Interface
- Sleep Operation With Programmable Negative Edge or Positive Edge Wake-Up
- <10 μ A Sleep Mode
- Pb-Free (RoHS compliant)

Pinout



Functional Diagram



Pin Descriptions

SYMBOL	DESCRIPTION
VC7/VCC	Battery cell 7 voltage input/VCC supply. This pin is used to monitor the voltage of this battery cell externally at pin AO. This pin also provides the operating voltage for the IC circuitry.
VCELLN	Battery cell N voltage input. This pin is used to monitor the voltage of this battery cell externally at pin AO. VCELLN connects to the positive terminal of CELLN and the negative terminal of CELLN + 1.
VSS	Ground. This pin connects to the most negative terminal in the battery string.
DSREF	Discharge current sense reference. This input provides a separate reference point for the charge and discharge current monitoring circuits. With a separate reference connection, it is possible to minimize errors that result from voltage drops on the ground lead when the load is drawing large currents. If a separate reference is not necessary, connect this pin to VSS.
DSENSE	Discharge current sense monitor. This input monitors the discharge current by monitoring a voltage. It can monitor the voltage across a sense resistor, or the voltage across the DFET, or by using a FET with a current sense pin. The voltage on this pin is measured with reference to DSREF.
CSENSE	Charge current sense monitor. This input monitors the charge current by monitoring a voltage. It can monitor the voltage across a sense resistor, or the voltage across the CFET, or by using a FET with a current sense pin. The voltage on this pin is measured with reference to VSS.
DFET	Discharge FET control. The ISL94200 controls the gate of a discharge FET through this pin. The power FET is a N-Channel device. The FET is turned on only by the microcontroller. The FET can be turned off by the microcontroller, but the ISL94200 also turns off the FET in the event of an overcurrent or short circuit condition. If the microcontroller detects an undervoltage condition on any of the battery cells, it can turn off the discharge FET by controlling this output with a control bit.
CFET	Charge FET control. The ISL94200 controls the gate of a charge FET through this pin. The power FET is a N-Channel device. The FET is turned on only by the microcontroller. The FET can be turned off by the microcontroller, but the ISL94200 also turns off the FET in the event of an overcurrent condition. If the microcontroller detects an overvoltage condition on any of the battery cells, it can turn off the FET by controlling this output with a control bit.
VMON	Discharge load monitoring. In the event of an overcurrent or short circuit condition, the microcontroller can enable an internal resistor that connects between the VMON pin and VSS. When the FETs open because of an overcurrent or short circuit condition and the load remains, the voltage at VMON will be near the VCC voltage. When the load is released, the voltage at VMON drops below a threshold indicating that the overcurrent or short circuit condition is resolved. At this point, the LDFAIL flag is cleared and operation can resume.
AO	Analog multiplexer output. The analog output pin is used by an external microcontroller to monitor the cell voltages and temperature sensor voltages. The microcontroller selects the specific voltage being applied to the output by writing to a control register.
TEMP3V	Temperature monitor output control. This pin outputs a voltage to be used in a divider that consists of a fixed resistor and a thermistor. The thermistor is located in close proximity to the cells. The TEMP3V output is connected internally to the RGO voltage through a PMOS switch only during a measurement of the temperature, otherwise the TEMP3V output is off. The TEMP3V output can be turned on continuously with a special control bit. Microcontroller wake up control. The TEMP3V pin is also turned on when any of the DSC, DOC, or COC bits are set. This can be used to wake up a sleeping microcontroller to respond to overcurrent conditions with its own control mechanism.
TEMPI	Temperature monitor input. This pin inputs the voltage across a thermistor to determine the temperature of the cells. When this input drops below TEMP3V/13, an external over-temperature condition exists. The TEMPI voltage is also fed to the AO output pin through an analog multiplexer so the temperature of the cells can be monitored by the microcontroller.
RGO	Regulated output voltage. This pin connects to the emitter of an external NPN transistor and works in conjunction with the RGC pin to provide a regulated 3.3V. The voltage at this pin provides feedback for the regulator and power for many of the ISL94200 internal circuits as well as providing the 3.3V output voltage for the microcontroller and other external circuits.
RGC	Regulated output control. This pin connects to the base of an external NPN transistor and works in conjunction with the RGO pin to provide a regulated 3.3V. The RGC output provides the control signal for the external transistor to provide the 3.3V regulated voltage on the RGO pin.
WKUP	Wake up Voltage. This input wakes up the part when the voltage crosses a turn-on threshold (wake up is edge triggered). The condition of the pin is reflected in the WKUP bit (The WKUP bit is level sensitive.) WKPOL bit = "1": the device wakes up on the rising edge of the WKUP pin. Also, the WKUP bit is HIGH only when the WKUP pin voltage > threshold. WKPOL bit = "0": the device wakes up on the falling edge of the WKUP pin. Also, the WKUP bit is HIGH only when the WKUP pin voltage < threshold.
SDA	Serial Data. This is the bidirectional data line for an I ² C interface.
SCL	Serial Clock. This is the clock input for an I ² C communication link.

Absolute Maximum Ratings

Power Supply Voltage, VCC V_{SS} - 0.5V to V_{SS} + 36.0V
 Cell Voltage, VCELL
 VCELLN - (VCELLN - 1), VCELL1 - VSS -0.5V to 5V
 Terminal Voltage, V_{TERM1}
 (SCL, SDA, CSENSE, DSENSE, TEMPI, RGO, AO, TEMP3V)
 V_{SS} - 0.5 to V_{RGO} + 0.5V
 Terminal Voltage, V_{TERM2} (CFET, VMON) V_{SS} - 22.0V to V_{CC}
 Terminal Voltage, V_{TERM3} (WKUP)
 V_{SS} - 0.5V to V_{CC} (V_{CC} < 27V)
 Terminal Voltage, V_{TERM4} (RGC) V_{SS} - 0.5V to 5V
 Terminal Voltage, V_{TERM5}, (all other pins)
 V_{SS} - 0.5V to V_{CC} + 0.5V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2) θ_{JA} (°C/W) θ_{JC} (°C/W)
 24 Ld QFN 32 2
 Continuous Package Power Dissipation 400mW
 Storage Temperature -55 to +125°C
 Pb-free Reflow Profile see link below
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

Operating Conditions

Temperature Range -40°C to +85°C
 Supply Voltage Range (Typical). 5V to 10V
 Operating Voltage:
 VCC pin 9.2V to 30.1V
 VCELL1 - VSS 2.3V to 4.3V
 VCELLN - (VCELLN - 1) 2.3V to 4.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Operating Specifications Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Operating Voltage	V _{CC}		9.2		30.1	V
Power-Up Condition 1	V _{PORVCC}	V _{CC} voltage (Note 3)		4	9.2	V
Power-Up Condition 2 Threshold	V _{POR123}	V _{CELL1} - V _{SS} and V _{CELL2} - V _{CELL1} and V _{CELL3} - V _{CELL2} (rising) (Note 3)	1.1	1.7	2.3	V
Power-Up Condition 2 Hysteresis	V _{PORhys}	V _{CELL1} - V _{SS} and V _{CELL2} - V _{CELL1} and V _{CELL3} - V _{CELL2} (falling) (Note 3)		70		mV
3.3V Regulated Voltage	V _{RGO}	0 μ A < I _{RGC} < 350 μ A	3.0	3.3	3.6	V
3.3VDC Voltage Regulator Control Current Limit	I _{RGC}	(Control current at output of RGC. Recommend NPN with gain of 70+)	0.35	0.50		mA
V _{CC} Supply Current	I _{VCC1}	Power-up defaults, WKUP pin = 0V.		400	510	μ A
RGO Supply Current	I _{RGO1}	Power-up defaults, WKUP pin = 0V.		300	410	μ A
V _{CC} Supply Current	I _{VCC2}	LDMONEN bit = 1, VMON floating, CFET = 1, DFET=1, WKPOL bit = 1, VWKUP = 10V, [AO3:AO0] bits = 03H.		500	700	μ A
RGO Supply Current	I _{RGO2}	LDMONEN bit = 1, VMON floating, CFET = 1, DFET=1, WKPOL bit = 1, VWKUP = 10V, [AO3:AO0] bits = 03H.		450	650	μ A
V _{CC} Supply Current	I _{VCC3}	Default register settings, except SLEEP bit = 1. WKUP pin = VCELL1			10	μ A
RGO Supply Current	I _{RGO3}	Default register settings, except SLEEP bit = 1. WKUP pin = VCELL1			1	μ A
VCELL Input Current (V _{CELL1})	I _{VCELL1}	AO3:AO0 bits = 0000H			14	μ A
VCELL Input Current (V _{CELLN})	I _{VCELLN}	AO3:AO0 bits = 0000H			10	μ A

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PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
OVERCURRENT/SHORT CIRCUIT PROTECTION SPECIFICATIONS						
Overcurrent Detection Threshold (Discharge) Voltage Relative To DSREF (Default in Boldface)	V _{OCD}	V_{OCD} = 0.10V (OCDV1, OCDV0 = 0, 0)	0.08	0.10	0.12	V
		V _{OCD} = 0.12V (OCDV1, OCDV0 = 0,1)	0.10	0.12	0.14	V
		V _{OCD} = 0.14V (OCDV1, OCDV0 = 1,0)	0.12	0.14	0.16	V
		V _{OCD} = 0.16V (OCDV1, OCDV0 = 1,1)	0.14	0.16	0.18	V
Overcurrent Detection Threshold (Charge) Voltage Relative to DSREF (Default in Boldface)	V _{OCC}	V_{OCC} = 0.10V (OCCV1, OCCV0 = 0, 0)	-0.12	-0.10	-0.07	V
		V _{OCC} = 0.12V (OCCV1, OCCV0 = 0,1)	-0.14	-0.12	-0.09	V
		V _{OCC} = 0.14V (OCCV1, OCCV0 = 1,0)	-0.16	-0.14	-0.11	V
		V _{OCC} = 0.16V (OCCV1, OCCV0 = 1,1)	-0.18	-0.16	-0.13	V
Short Current Detection Threshold Voltage Relative to DSREF (Default in Boldface)	V _{SC}	V_{OC} = 0.20V (SCDV1, SCDV0 = 0, 0)	0.15	0.20	0.25	V
		V _{OC} = 0.35V (SCDV1, SCDV0 = 0,1)	0.30	0.35	0.40	V
		V _{OC} = 0.65V (SCDV1, SCDV0 = 1, 0)	0.60	0.65	0.70	V
		V _{OC} = 1.20V (SCDV1, SCDV0 = 1,1)	1.10	1.20	1.30	V
Load Monitor Input Threshold (Falling Edge)	V _{VMON}	LDMONEN bit = "1"	1.1	1.45	1.8	V
Load Monitor Input Threshold (Hysteresis)	V _{VMONH}	LDMONEN bit = "1"		0.25		mV
Load Monitor Current	I _{VMON}		20	40	60	μA
Short Circuit Time-out	t _{SCD}	Short circuit detection delay (SCLONG bit = '0')	90	190	290	μs
		Short circuit detection delay (SCLONG bit = '1')	5	10	15	ms
Over Discharge Current Time-out (Default In Boldface)	t _{OCD}	t_{OCD} = 160ms (OCDT1, OCDT0 = 0, 0 and DTDIV = 0)	80	160	240	ms
		t _{OCD} = 320ms (OCDT1, OCDT0 = 0, 1 and DTDIV = 0)	160	320	480	ms
		t _{OCD} = 640ms (OCDT1, OCDT0 = 1, 0 and DTDIV = 0)	320	640	960	ms
		t _{OCD} = 1280ms (OCDT1, OCDT0 = 1, 1 and DTDIV = 0)	640	1280	1920	ms
		t _{OCD} = 2.5ms (OCDT1, OCDT0 = 0, 0 and DTDIV = 1)	1.25	2.50	3.75	ms
		t _{OCD} = 5ms (OCDT1, OCDT0 = 0, 1 and DTDIV = 1)	2.5	5	7.5	ms
		t _{OCD} = 10ms (OCDT1, OCDT0 = 1, 0 and DTDIV = 1)	5	10	15	ms
		t _{OCD} = 20ms (OCDT1, OCDT0 = 1, 1 and DTDIV = 1)	10	20	30	ms

Operating Specifications Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Over Charge Current Time-out (Default In Boldface)	t _{OCC}	t _{OCC} = 80ms (OCCT1,OCCT0 = 0, 0 and CTDIV = 0)	40	80	120	ms
		t _{OCC} = 160ms (OCCT1, OCCT0 = 0, 1 and CTDIV = 0)	80	160	240	ms
		t _{OCC} = 320ms (OCCT1, OCCT0 = 1, 0 and CTDIV = 0)	160	320	480	ms
		t _{OCC} = 640ms (OCCT1, OCCT0 = 1, 1 and CTDIV = 0)	320	640	960	ms
		t _{OCC} = 2.5ms (OCCT1, OCCT0 = 0, 0 and CTDIV = 1)	1.25	2.50	3.75	ms
		t _{OCC} = 5ms (OCCT1, OCCT0 = 0, 1 and CTDIV = 1)	2.5	5	7.5	ms
		t _{OCC} = 10ms (OCCT1, OCCT0 = 1, 0 and CTDIV = 1)	5	10	15	ms
		t _{OCC} = 20ms (OCCT1, OCCT0 = 1, 1 and CTDIV = 1)	10	20	30	ms
OVER-TEMPERATURE PROTECTION SPECIFICATIONS						
Internal Temperature Shutdown Threshold	T _{INTSD}			+125		°C
Internal Temperature Hysteresis	T _{HYS}	Temperature drop needed to restore operation after over-temperature shutdown.		+20		°C
Internal Over-temperature Turn On Delay Time	t _{ITD}			128		ms
External Temperature Output Current	I _{XT}	Current output capability at TEMP3V pin	1.2			mA
External Temperature Limit Threshold	T _{XTF}	Voltage at V _{TEMP1} ; Relative to falling edge $\frac{V_{TEMP3V}}{13}$	-20	0	+20	mV
External Temperature Limit Hysteresis	T _{XTH}	Voltage at V _{TEMP1} .	60	110	160	mV
External Temperature Monitor Delay	t _{XTD}	Delay between activating the external sensor and the internal over-temperature detection.		1		ms
External Temperature Autoscan On-Time	t _{XTAON}	TEMP3V is ON (3.3V)		5		ms
External Temperature Autoscan Off-Time	t _{XTAOFF}	TEMP3V output is off.		635		ms
ANALOG OUTPUT SPECIFICATIONS						
Cell Monitor Analog Output Voltage Accuracy	V _{AOC}	[V _{CELLN} - (V _{CELLN-1})]/2 - AO	-15	4	30	mV
Cell Monitor Analog Output External Temperature Accuracy	V _{AOXT}	External temperature monitoring accuracy. Voltage error at AO when monitoring TEMPI voltage (measured with TEMPI = 1V)	-10		10	mV
Internal Temperature Monitor Output Voltage Slope	V _{INTMON}	Internal temperature monitor voltage change		-3.5		mV/°C

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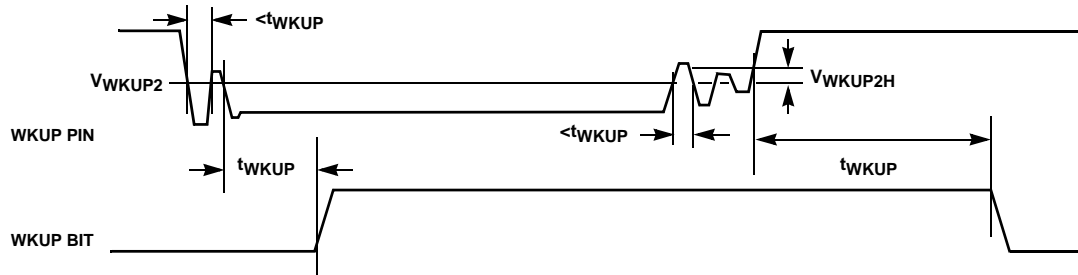
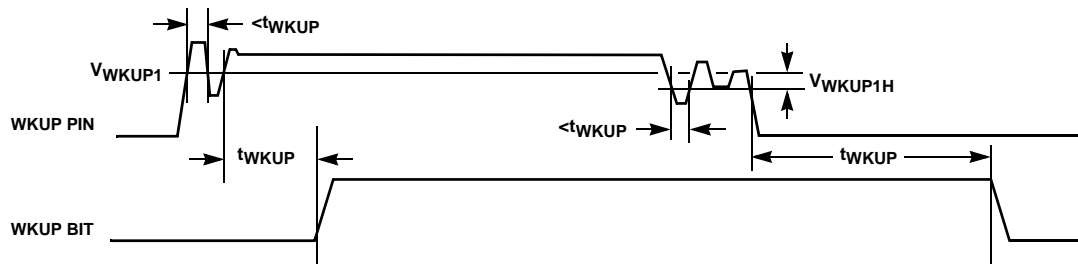
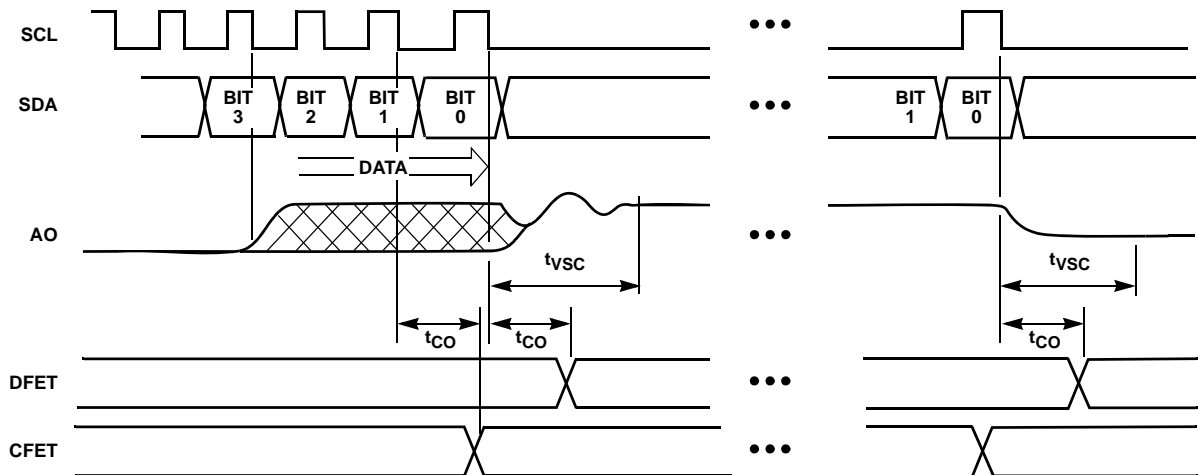
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Internal Temperature Monitor Output	T _{INT25}	Output at +25°C		1.31		V
AO Output Stabilization Time	t _{VSC}	From SCL falling edge at data bit 0 of command to AO output stable within 0.5% of final value. AO voltage steps from 0V to 2V. (C _{AO} = 10pF) (Note 7)			0.1	ms
WAKE UP/SLEEP SPECIFICATIONS						
Device WKUP Pin Voltage Threshold (WKUP Pin Active High - Rising Edge)	V _{WKUP1}	WKUP pin rising edge (WKPOL = 1) Device wakes up and sets WKUP flag HIGH.	3.5	5.0	6.5	V
Device Wkup Pin Hysteresis (WKUP Pin Active High)	V _{WKUP1H}	WKUP pin falling edge hysteresis (WKPOL = 1) sets WKUP flag LOW (does not automatically enter sleep mode)		100		mV
Input Resistance On WKUP	R _{WKUP}	Resistance from WKUP pin to VSS (WKPOL = 1)	130	230	330	kΩ
Device WKUP Pin Active Voltage Threshold (WKUP Pin Active Low - Falling Edge)	V _{WKUP2}	WKUP pin falling edge (WKPOL = 0) Device wakes up and sets WKUP flag HIGH.	V _{CELL1} - 2.6	V _{CELL1} - 2.0	V _{CELL1} - 1.2	V
Device Wkup Pin Hysteresis (WKUP Pin Active Low)	V _{WKUP2H}	WKUP pin rising edge hysteresis (WKPOL = 0) sets WKUP flag LOW (does not automatically enter sleep mode)		200		mV
Device Wake-up Delay	t _{WKUP}	Delay after voltage on WKUP pin crosses the threshold (rising or falling) before activating the WKUP bit.	20	40	60	ms
FET CONTROL SPECIFICATIONS (FOR VCELL1, VCELL2, VCELL3 VOLTAGES FROM 2.8V TO 4.3V)						
Control Outputs Response Time (CFET, DFET)	t _{CO}	Bit 0 to start of control signal (DFET) Bit 1 to start of control signal (CFET)		1.0		μs
CFET Gate Voltage	V _{CFET}	No load on CFET	V _{CELL3} - 0.5		V _{CELL3} + 0.1	V
DFET Gate Voltage	V _{DFET}	No load on DFET	V _{CELL3} - 0.5		V _{CELL3} + 0.1	V
FET Turn On Current (DFET)	I _{DFON}	DFET voltage = 0 to V _{CELL3} - 1.5V	80	130	400	μA
FET Turn On Current (CFET)	I _{CF(ON)}	CFET voltage = 0 to V _{CELL3} - 1.5V	80	200	400	μA
FET Turn Off Current (DFET)	I _{DF(OFF)}	DFET voltage = V _{DFET} to 1V	100	180		mA
DFET Resistance to VSS	R _{DF(OFF)}	V _{DFET} < 1V (When turning off the FET)			11	Ω
SERIAL INTERFACE CHARACTERISTICS						
SCL Clock Frequency	f _{SCL}				100	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t _{IN}	Any pulse narrower than the max spec is suppressed.			50	ns
SCL Falling Edge to SDA Output Data Valid	t _{AA}	From SCL falling crossing V _{IH(min)} , until SDA exits the V _{IL(max)} to V _{IH(min)} window.			3.5	μs
Time the Bus Must Be Free Before Start of New Transmission	t _{BUF}	SDA crossing V _{IH(min)} during a STOP condition to SDA crossing V _{IH(min)} during the following START condition.	4.7			μs
Clock Low Time	t _{LOW}	Measured at the V _{IL(max)} crossing.	4.7			μs
Clock High Time	t _{HIGH}	Measured at the V _{IH(min)} crossing.	4.0			μs

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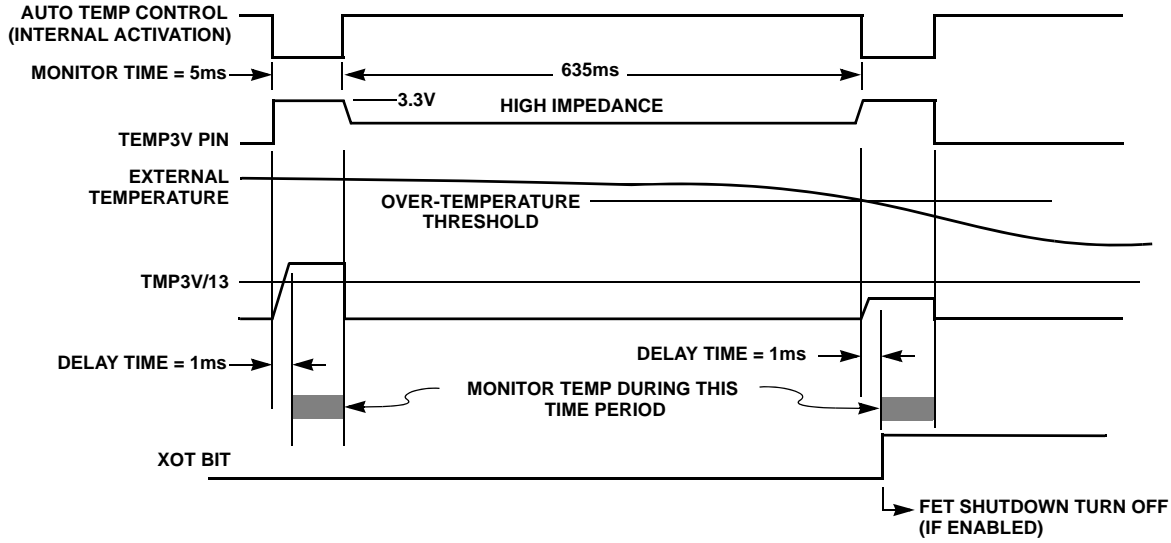
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Start Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing the $V_{IH(min)}$ level.	4.7			μs
Start Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing $V_{IL(max)}$ to SCL falling edge crossing $V_{IH(min)}$.	4.0			μs
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the $V_{IL(max)}$ to $V_{IH(min)}$ window to SCL rising edge crossing $V_{IL(min)}$.	250			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing $V_{IH(min)}$ to SDA entering the $V_{IL(max)}$ to $V_{IH(min)}$ window.	300			μs
Stop Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing $V_{IH(min)}$ to SDA rising edge crossing $V_{IL(max)}$.	4.0			μs
Stop Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing $V_{IH(min)}$.	4.0			μs
Data Output Hold Time	t_{DH}	From SCL falling edge crossing $V_{IL(max)}$ until SDA enters the $V_{IL(max)}$ to $V_{IH(min)}$ window. (Note 4)	0			ns
SDA and SCL Rise Time	t_R	From $V_{IL(max)}$ to $V_{IH(min)}$.			1000	ns
SDA and SCL Fall Time	t_F	From $V_{IH(min)}$ to $V_{IL(max)}$.			300	ns
Capacitive Loading Of SDA Or SCL (Note 5)	C_b	Total on-chip and off-chip			400	pF
SDA and SCL Bus Pull-up Resistor-Off-Chip (Note 5)	R_{OUT}	Maximum is determined by t_R and t_F . For $C_B = 400pF$, max is about $2k\Omega \sim 2.5k\Omega$ For $C_B = 40pF$, max is about $15k\Omega$ to $20k\Omega$	1			$k\Omega$
Input Leakage Current (SCL, SDA)	I_{LI}		-10		10	μA
Input Buffer Low Voltage (SCL, SDA)	V_{IL}	Voltage relative to V_{SS} of the device.	-0.3		$V_{RGO} \times 0.3$	V
Input Buffer High Voltage (SCL, SDA)	V_{IH}	Voltage relative to V_{SS} of the device.	$V_{RGO} \times 0.7$		$V_{RGO} + 0.1$	V
Output Buffer Low Voltage (SDA)	V_{OL}	$I_{OL} = 1mA$			0.4	V
SDA and SCL Input Buffer Hysteresis (Note 5)	I^2CHYST	Sleep bit = 0	$0.05 \times V_{RGO}$			V

NOTES:

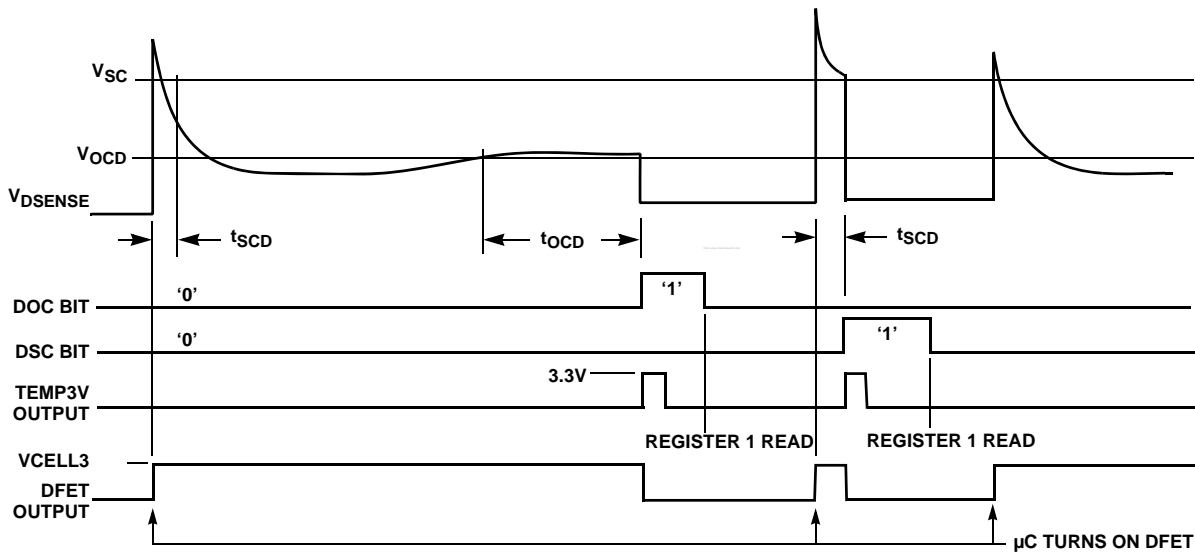
- Power-up of the device requires all V_{CELL1} , V_{CELL2} , V_{CELL3} , and V_{CC} to be above the limits specified.
- The device provides an internal hold time of at least 300ns for the SDA signal to bridge the unidentified region of the falling edge of SCL.
- Limits should be considered typical and are not production tested.
- Typical $5\Omega \pm 2\Omega$, based on characterization data.
- Maximum output capacitance = 15pF.

Wake-Up Timing (WKPOL = 0)**Wake up timing (WKPOL = 1)****Change in Voltage Source, FET Control**

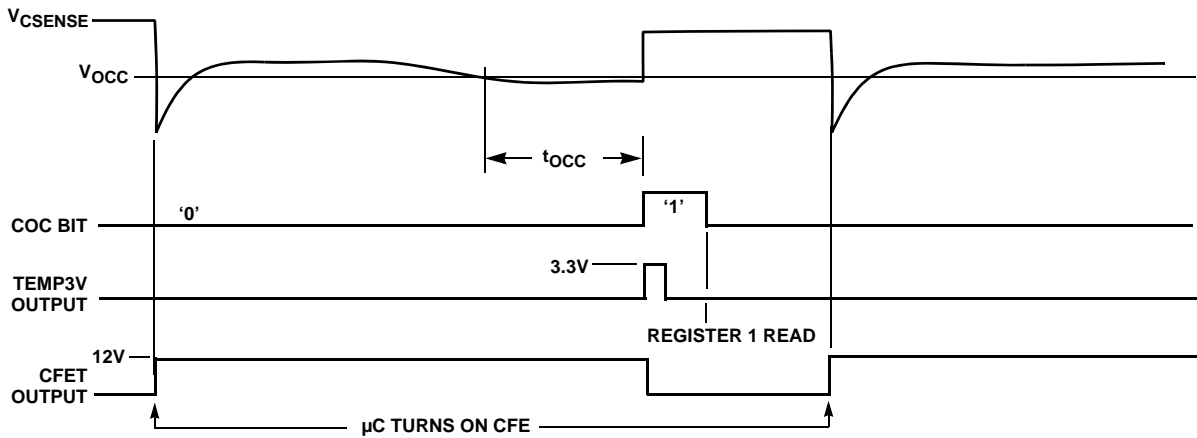
Automatic Temperature Scan



Discharge Overcurrent/Short Circuit Monitor (Assumes DENOCD and DENSCL bits are '0')

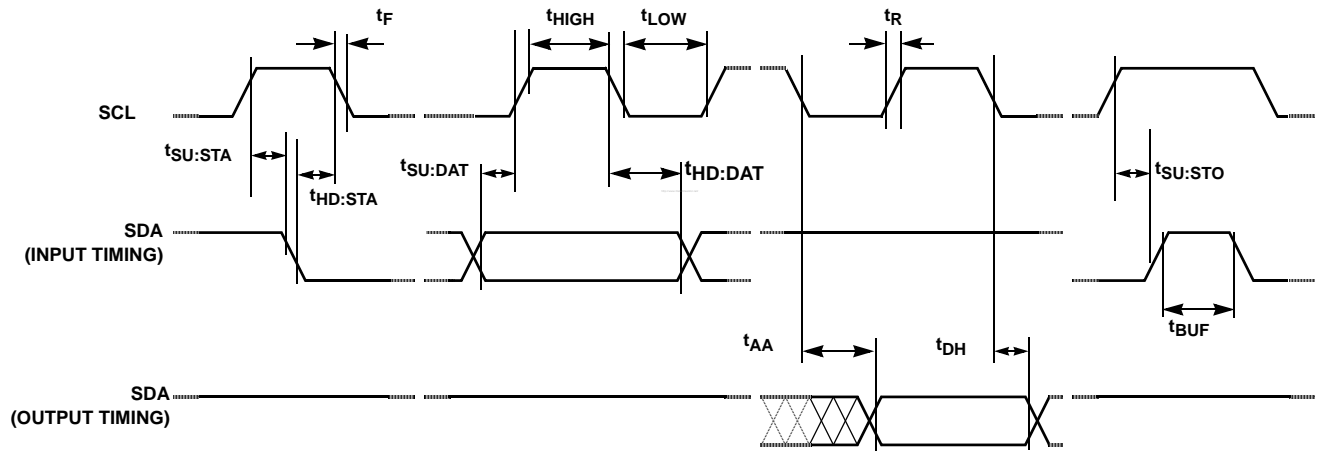


Charge Overcurrent Monitor (Assumes DENOCC bit is '0')



Serial Interface Timing Diagrams

Bus Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE: CHANGES ALLOWED	CHANGING: STATE NOT KNOWN
	MAY CHANGE FROM LOW TO HIGH	WILL CHANGE FROM LOW TO HIGH		N/A	CENTER LINE IS HIGH IMPEDANCE
	MAY CHANGE FROM HIGH TO LOW	WILL CHANGE FROM HIGH TO LOW			

Registers

TABLE 1. REGISTERS

ADDR	REGISTER	READ/WRITE	7	6	5	4	3	2	1	0
00H	Config/Op Status	Read only	Reserved	Reserved	SA Single AFE	WKUP WKUP pin Status	Reserved	Reserved	Reserved	Reserved
01H	Operating Status (Note 10)	Read only	Reserved	Reserved	XOT Ext over temp	IOT Int over Temp	LDFAIL Load Fail (VMON)	DSC Short Circuit	DOC Discharge OC	COC Charge OC
02H	Not Used	Read/Write	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
03H	Analog Out	Read/Write	UFLG1 User Flag 1	UFLG0 User Flag 0	Reserved	Reserved	AO3	AO2	AO1	AO0
Analog output select bits										
04H	FET Control	Read/Write	SLEEP Force Sleep (Note 11)	LDMONEN Turn on VMON connection	Reserved	Reserved	Reserved	Reserved	CFET Turn on Charge FET (Note 12)	DFET Turn on Discharge FET (Note 12)
05H	Discharge Set	Read/Write (Write only if DISSETEN bit set)	DEN OCD Turn off automatic OCD control	OCDV1 Overcurrent Discharge Threshold Voltage	OCDV0	DEN SCD Turn off automatic SCD control	SCDV1 Short Circuit Discharge Threshold Voltage	SCDV0	OC DT1 Overcurrent Discharge Time-out	OC DT0
06H	Charge Set	Read/Write (Write only if CHSETEN bit set)	DEN OCC Turn off automatic OCC control	OCCV1 Overcurrent Charge Threshold Voltage	OCCV0	SC LONG Long Short-circuit delay	CT DIV Divide charge time by 32	DT DIV Divide discharge time by 64	OC CT1 Overcurrent Charge Time-out	OC CT0
07H	Feature Set	Read/Write (Write only if FSETEN bit set)	ATMPOFF Turn off automatic external temp scan	DIS3 Disable 3.3V reg. (device requires external 3.3V)	TMP3ON Turn on Temp3V	DISXTSD Disable external thermal shutdown	DISITSD Disable internal thermal shutdown	POR Force POR	DISWKUP Disable WKUP pin	WKPOL Wake Up Polarity
08H	Write Enable	Read/Write	FSETEN Enable Feature Set writes	CHSETEN Enable Charge Set writes	DISSETEN Enable Discharge Set writes	UFLG3 User Flag 3	UFLG2 User Flag 2	Reserved	Reserved	Reserved
09H:FFH	Reserved	NA	RESERVED							

NOTES:

8. A "1" written to a control or configuration bit causes the action to be taken. A "1" read from a status bit indicates that the condition exists.
9. "Reserved" indicates that the bit or register is reserved for future expansion. When writing to addresses 2, 3, 4, and 8: write a reserved bit with the value "0". Do not write to reserved registers at addresses 09H through FFH. Ignore reserved bits that are returned in a read operation.
10. These status bits are automatically cleared when the register is read. All other status bits are cleared when the condition is cleared.
11. This SLEEP bit is cleared on initial power up, by the WKUP pin going high (when WKPOL = "1") or by the WKUP pin going low (when WKPOL = "0"), and by writing a "0" to the location with an I²C command.
12. When the automatic responses are enabled, these bits are automatically reset by hardware when an overcurrent or short circuit condition turns off the FETs. At all other times, an I²C write operation controls the output to the respective FET and a read returns the current state of the FET drive output circuit (though not the actual voltage at the output pin.)

Status Registers

TABLE 2. CONFIG/OP STATUS REGISTER (ADDR: 00H)

BIT	FUNCTION	DESCRIPTION
7	RESERVED	Reserved for future expansion.
6	RESERVED	Reserved for future expansion.
5	SA Single AFE	Indicates the device is an ISL94200. This bit is set in the chip and cannot be changed.
4	WKUP Wakeup pin status	This bit is set and reset by hardware. When 'WKPOL' is HIGH: 'WKUP' HIGH = WKUP pin > Threshold voltage 'WKUP' LOW = WKUP pin < Threshold voltage When 'WKPOL' is LOW: 'WKUP' HIGH = WKUP pin < Threshold voltage 'WKUP' LOW = WKUP pin > Threshold voltage
3	RESERVED	Reserved for future expansion.
2	RESERVED	Reserved for future expansion.
1	RESERVED	Reserved for future expansion.
0	RESERVED	Reserved for future expansion.

TABLE 3. OPERATING STATUS REGISTER (ADDR: 01H)

BIT	FUNCTION	DESCRIPTION
7	RESERVED	Reserved for future expansion.
6	RESERVED	Reserved for future expansion.
5	XOT Ext Over-temp	This bit is set to "1" when the external thermistor indicates an over-temperature condition. If the temperature condition has cleared, this bit is reset when the register is read.
4	IOT Int Over-temp	This bit is set to "1" when the internal thermistor indicates an over-temperature condition. If the temperature condition has cleared, this bit is reset when the register is read.
3	LDFAIL Load Fail (VMON)	When the function is enabled, this bit is set to "1" by hardware when a discharge overcurrent or short circuit condition occurs and the load remains heavy. When the load fail condition is cleared or under a light load, the bit is reset when the register is read.
2	DSC Short Circuit	This bit is set by hardware when a short circuit condition occurs during discharge. When the discharge short circuit condition is removed, the bit is reset when the register is read.
1	DOC Discharge OC	This bit is set by hardware when an overcurrent condition occurs during discharge. When the discharge overcurrent condition is removed, the bit is reset when the register is read.
0	COC Charge OC	This bit is set by hardware when an overcurrent condition occurs during charge. When the charge overcurrent condition is removed, the bit is reset when the register is read.

Control Registers

TABLE 4. ANALOG OUT CONTROL REGISTER (ADDR: 03H)

BITS	FUNCTION		DESCRIPTION	
7	UFLG1 User Flag 1		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
6	UFLG0 User Flag 0		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
5:4	RESERVED		Reserved for future expansion	
BIT 3 AO3	BIT 2 AO2	BIT 1 AO1	BIT 0 AO0	OUTPUT VOLTAGE
0	0	0	0	No Output (low power state)
0	0	0	1	V _{CELL1}
0	0	1	0	V _{CELL2}
0	0	1	1	V _{CELL3}
0	1	0	0	V _{CELL4}
0	1	0	1	V _{CELL5}
0	1	1	0	V _{CELL6}
0	1	1	1	V _{CELL7}
1	0	0	0	External Temperature
1	0	0	1	Internal Temperature
1	x	1	x	RESERVED
1	1	x	x	RESERVED

Configuration Registers

The device is configured for specific application requirements using the Configuration Registers. The configuration registers consist of SRAM memory.

This memory is powered by the RGO output. In a sleep condition, an internal switch converts power for the contents of these registers from RGO to the V_{CELL1} input.

TABLE 5. FET CONTROL REGISTER (ADDR: 04H)

BIT	FUNCTION	DESCRIPTION
7	SLEEP Force Sleep	Setting this bit to "1" forces the device to go into a sleep condition. This turns off both FET outputs and the voltage regulator. This also resets the CFET, DFET, and CB7ON:CB1ON bits. The SLEEP bit is automatically reset to "0" when the device wakes up. This bit does not reset the AO3:AO0 bits.
6	LDMONEN Turn on VMON connection	Writing a "1" to this bit turns on the VMON circuit. Writing a "0" to this bit turns off the VMON circuit. As such, the microcontroller has full control of the operation of this circuit.
5:2	RESERVED	Reserved for future expansion.
1	CFET	Setting this bit to "1" turns on the charge FET. Setting this bit to "0" turns off the charge FET. This bit is automatically reset in the event of a charge overcurrent condition, unless the automatic response is disabled by the DENOCC bit.
0	DFET	Setting this bit to "1" turns on the discharge FET. Setting this bit to "0" turns off the discharge FET. This bit is automatically reset in the event of a discharge overcurrent or discharge short circuit condition, unless the automatic response is disabled by the DENOCD or DENS CD bits.

TABLE 6. DISCHARGE SET CONFIGURATION REGISTER (ADDR: 05H)

SETTING		FUNCTION
Bit 7	DEN OCD Turn off automatic OC discharge control	When set to '0', a discharge overcurrent condition automatically turns off the FETs. When set to '1', a discharge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the DOC bit, which also turns on the TEMP3V output.
BIT 6 OCDV1	BIT 5 OCDV0	OVERCURRENT DISCHARGE VOLTAGE THRESHOLD
0	0	$V_{OCD} = 0.10V$
0	1	$V_{OCD} = 0.12V$
1	0	$V_{OCD} = 0.14V$
1	1	$V_{OCD} = 0.16V$
Bit 4	DEN SCD Turn off automatic SC discharge control	When set to '0', a discharge short circuit condition turns off the FETs. When set to '1', a discharge short circuit condition will not automatically turn off the FETs. In either case, the condition sets the SCD bit, which also turns on the TEMP3V output.
BIT 3 SCDV1	BIT 2 SCDV0	SHORT CIRCUIT DISCHARGE VOLTAGE THRESHOLD
0	0	$V_{SCD} = 0.20V$
0	1	$V_{SCD} = 0.35V$
1	0	$V_{SCD} = 0.65V$
1	1	$V_{SCD} = 1.20V$
BIT 1 OCDT1	BIT 0 OCDT0	OVERCURRENT DISCHARGE TIME-OUT
0	0	$t_{OCD} = 160ms$ (2.5ms if DTDIV = 1)
0	1	$t_{OCD} = 320ms$ (5ms if DTDIV = 1)
1	0	$t_{OCD} = 640ms$ (10ms if DTDIV = 1)
1	1	$t_{OCD} = 1280ms$ (20ms if DTDIV = 1)

TABLE 7. CHARGE/TIME SCALE CONFIG REGISTER (ADDR: 06H)

SETTING		FUNCTION
Bit 7	DENOC Turn off automatic OC charge control	When set to '0', a charge overcurrent condition automatically turns off the FETs. When set to '1', a charge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the COC bit, which also turns on the TEMP3V output.
BIT 6 OCCV1	BIT 5 OCCV0	OVERCURRENT CHARGE VOLTAGE THRESHOLD
0	0	$V_{OCD} = 0.10V$
0	1	$V_{OCD} = 0.12V$
1	0	$V_{OCD} = 0.14V$
1	1	$V_{OCD} = 0.16V$
Bit 4	SCLONG Short circuit long delay	When this bit is set to '0', a short circuit needs to be in effect for 190 μ s before a shutdown begins. When this bit is set to '1', a short circuit needs to be in effect for 10ms before a shutdown begins.
Bit 3	CTDIV Divide charge time by 32	When set to "1", the charge overcurrent delay time is divided by 32. When set to "0", the charge overcurrent delay time is divided by 1.
Bit 2	DTDIV Divide discharge time by 64	When set to "1", the discharge overcurrent delay time is divided by 64. When set to "0", the discharge overcurrent delay time is divided by 1.
BIT 1 OCCT1	BIT 0 OCCT0	OVERCURRENT CHARGE TIME-OUT
0	0	$t_{OCC} = 80ms$ (2.5ms if CTDIV=1)
0	1	$t_{OCC} = 160ms$ (5ms if CTDIV=1)
1	0	$t_{OCC} = 320ms$ (10ms if CTDIV=1)
1	1	$t_{OCC} = 640ms$ (20ms if CTDIV=1)

TABLE 8. FEATURE SET CONFIGURATION REGISTER (ADDR: 07H)

BIT	FUNCTION	DESCRIPTION
7	ATMPOFF Turn off automatic external temp scan	When set to '1' this bit disables the automatic temperature scan. When set to '0', the temperature is turned on for 5ms in every 640ms.
6	DIS3 Disable 3.3V regulator	Setting this bit to "1" disables the internal 3.3V regulator. Setting this bit to "1" requires that there be an external 3.3V regulator connected to the RGO pin.
5	TMP3ON Turn on Temp 3.3V	Setting this bit to "1" turns ON the TEMP3V output to the external temperature sensor. The output will remain on as long as this bit remains "1".
4	DISXTSD Disable external thermal shutdown	Setting this bit to "1" disables the automatic shutdown of the power FETs in response to an external over-temperature condition. While the automatic response is disabled, the XOT flag is set so the microcontroller can initiate a shutdown based on the XOT flag.
3	DISITS Disable internal thermal shutdown	Setting this bit to "1" disables the automatic shutdown of the power FETs in response to an internal over-temperature condition. While the automatic response is disabled, the IOT flag is set so the microcontroller can initiate a shutdown based on the IOT flag.
2	POR Force POR	Setting this bit to "1" forces a POR condition. This resets all internal registers to zero.
1	DISWKUP Disable WKUP pin	Setting this bit to "1" disables the WKUP pin function. CAUTION: Setting this pin to '1' prevents a wake up condition. If the device then goes to sleep, it cannot be waken without a communication link that resets this bit, or by power cycling the device.
0	WKPOL Wake Up Polarity	Setting this bit to "1" sets the device to wake up on a rising edge at the WKUP pin. Setting this bit to "0" sets the device to wake up on a falling edge at the WKUP pin.

TABLE 9. WRITE ENABLE REGISTER (ADDR: 08H)

BIT	FUNCTION	DESCRIPTION
7	FSETEN Enable discharge set writes	When set to "1", allows writes to the Feature Set register. When set to "0", prevents writes to the Feature Set register (Addr: 07H). Default on initial power up is "0".
6	CHSETEN Enable charge set writes	When set to "1", allows writes to the Charge Set register. When set to "0", prevents writes to the Feature Set register (Addr: 06H). Default on initial power up is "0".
5	DISSETEN Enable discharge set writes	When set to "1", allows writes to the Discharge Set register (Addr: 05H). When set to "0", prevents writes to the Feature Set register. Default on initial power up is "0".
4	UFLG3 User Flag 3	General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.
3	UFLG2 User Flag 3	General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.
2	RESERVED	Reserved for future expansion.
1	RESERVED	Reserved for future expansion.
0	RESERVED	Reserved for future expansion.

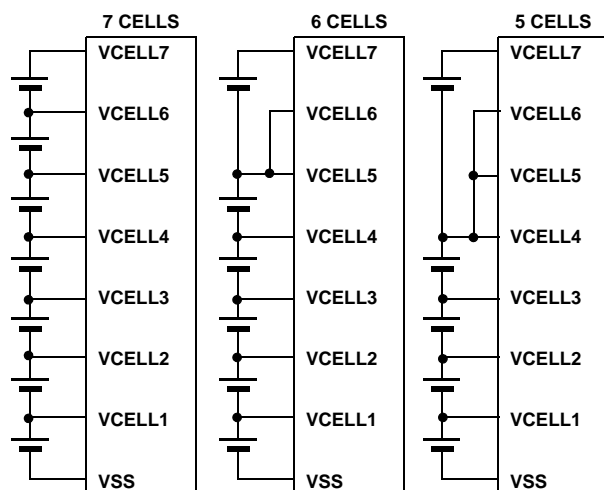
Device Description

Design Theory

Instructed by the microcontroller, the ISL94200 performs cell voltage monitoring operations, overcurrent and short circuit monitoring with automatic pack shutdown using built-in selectable time delays, and automatic turn off of the power FETs in an over-temperature condition. All automatic functions of the ISL94200 can be turned off and the microcontroller can manage the operations through software.

Battery Connection

The ISL94200 supports packs of 5 to 7 series connected Li-ion cells. Connection guidelines for each cell combination are shown in Figure 1.



Note: Multiple cells can be connected in parallel

FIGURE 1. BATTERY CONNECTION OPTIONS

System Power-Up/Power-Down

The ISL94200 powers up when the voltages on V_{CELL1} , V_{CELL2} , V_{CELL3} , and V_{CC} all exceed their POR threshold. At this time, the ISL94200 wakes up and turns on the RGO output.

RGO provides a regulated 3.3VDC $\pm 10\%$ voltage at pin RGO. It does this by using a control voltage on the RGC pin to drive an external NPN transistor (see Figure 2.) The transistor should have a beta of at least 70 to provide ample current to the device and external circuits and should have a V_{CE} of greater than 30V (preferably 50V). The voltage at the emitter of the NPN transistor is monitored and regulated to 3.3V by the control signal RGC. RGO also powers most of the ISL94200 internal circuits. A 500 Ω resistor is recommended in the collector of the NPN transistor to minimize initial current surge when the regulator turns on.

Once powered up, the device remains in a wake up state until put to sleep by the microcontroller (typically when the cells drop too low in voltage) or until the V_{CELL1} , V_{CELL2} , V_{CELL3} , or V_{CC} voltages drop below their POR threshold.

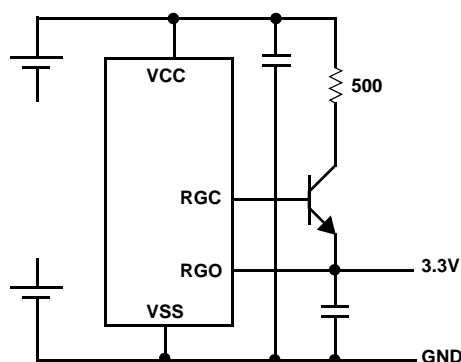


FIGURE 2. VOLTAGE REGULATOR CIRCUITS

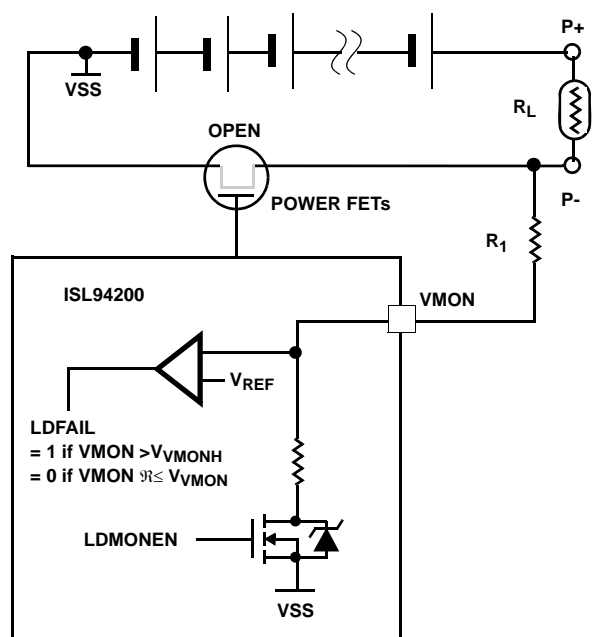


FIGURE 4. LOAD MONITOR CIRCUIT

LOAD MONITORING

The load monitor function in the ISL94200 (see Figure 4) is used primarily to detect that the load has been removed following an overcurrent or short circuit condition during discharge. This can be used in a control algorithm to prevent the FETs from turning on while the overload or short circuit condition remains.

The load monitor can also be used by the microcontroller algorithms after an undervoltage condition on any cells causes the FETs to turn off. Use of the load monitor prevents the FETs from turning on while the load is still present. This minimizes the possible “oscillations” that can occur when a load is applied in a low capacity pack. It can also be part of a system protection mechanism to prevent the load from turning on automatically - i.e. some action must be taken before the pack is again turned on.

The load monitor circuit can be turned on or off by the microcontroller. It is normally turned off to minimize current consumption. It must be activated by the external microcontroller for it to operate. The circuit works by internally connecting the VMON pin to VSS through a resistor. The circuit operates shown as in Figure 4.

In a typical pack operation, when an overcurrent or short circuit event happens, the DFET turns off, opening the battery circuit to the load. At this time, the R_L is small and the load monitor is initially off. In this condition, the voltage at VMON rises to nearly the pack voltage.

Once the power FETs turn off, the microcontroller activates the load monitor by setting the LDMONEN bit. This turns on an internal FET that adds a pull down resistor to the load monitor circuit. While still in the overload condition the

combination of the load resistor, an external adjustment resistor (R_1), and the internal load monitor resistor form a voltage divider. R_1 is chosen so that when the load is released to a sufficient level, the LDFAIL condition is reset.

OVER-TEMPERATURE SAFETY FUNCTIONS

External Temperature Monitoring

The external temperature is monitored by using a voltage divider consisting of a fixed resistor and a thermistor. This divider is powered by the ISL94200 TEMP3V output. This output is normally controlled so it is on for only short periods to minimize current consumption.

Without microcontroller intervention, and in the default state, the ISL94200 provides an automatic temperature scan. This scan circuit repeatedly turns on TEMP3V output (and the external temperature monitor) for 5ms out of every 640ms. In this way, the external temperature is monitored even if the microcontroller is asleep.

When the TEMP3V output turns on, the ISL94200 waits 1ms for the temperature reading to stabilize, then compares the external temperature voltage with an internal voltage divider that is set to TEMP3V/13. When the thermistor voltage is below the reference threshold after the delay, an external temperature fail condition exists. To set the external over-temperature limit, set the value of R_X resistor to the 12 times the resistance of the thermistor at the over-temp threshold.

The TEMP3V output pin also turns on when the microcontroller sets the AO3:AO0 bits to select that the external temperature voltage. This causes the TEMPI voltage to be placed on AO and activates (after 1ms) the over-temperature detection. As long as the AO3:AO0 bits point to the external temperature, the TEMP3V output remains on.

Because of the manual scan of the temperature, it may be desired to turn off the automatic scan, although they can be used at the same time without interference. To turn off the automatic scan, set the ATMPOFF bit.

The microcontroller can over-ride both the automatic temperature scan and the microcontroller controlled temperature scan by setting the TEMP3ON configuration bit. This turns on the TEMP3V output to keep the temperature control voltage on all the time, for a continuous monitoring of an over-temperature condition. This likely will consume a significant amount of current, so this feature is usually used for special or test purposes.

Protection

As a default, when the ISL94200 detects an internal or external over-temperature condition, the FETs are turned off, and the IOT bit or XOT bit (respectively) is set.

External VMON/CFET Protection Mechanisms

When there is a single charge/discharge path, a blocking diode is recommended in the VMON to P- path in ISL94200 solution. See D₁ in Figure 7. This diode is to protect against a negative voltage on the VMON pin that can occur when the FETs are off and the charger connects to the pack. This diode is not needed when there is a separate charge and discharge path, because the voltages on P- (discharge) are likely always positive. The diode also is not needed if the differential between the minimum pack voltage and maximum charger voltage does not exceed 22V.

When the pack is designed with a single set of charge/discharge FETs, the ISL94200 CFET pin should be protected in the event of an over-current or short circuit shutdown. When this happens, the FET opens suddenly. The flyback voltage from the motor windings could exceed the maximum input voltage on the CFET pin. So, it is recommended that an additional external series diode be placed between the CFET pin of the ISL94200 and the gate of the Charge FET. See Diode D₃ in Figure 7. This will reduce the CFET gate voltage, but not significantly.

Finally, to protect the Charge FET itself in the event of a large negative voltage on the Pack- pin, zener diode D₄ is added. The large negative voltage can occur when the P- pin goes significantly negative, while the CFET pin is being internally clamped at V_{SS}. The zener voltage of D₄ should be less than the V_{GS(max)} specification of the FET.

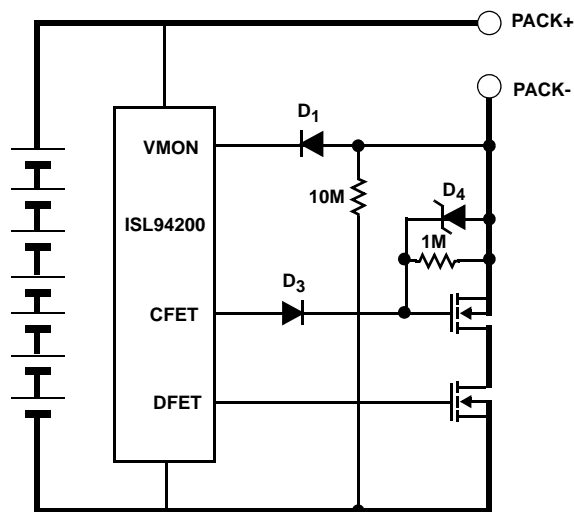


FIGURE 7. USE OF A DIODES FOR PROTECTING THE CFET AND VMON PINS

User Flags

The ISL94200 contains four flags in the register area that the microcontroller can use for general purpose indicators. These bits are designated UFLG3, UFLG2, UFLG1, and UFLG0. The microcontroller can set or reset these bits by writing into the appropriate register.

The user flag bits are battery backed up, so the contents remain even after exiting a sleep mode. However, if the

microcontroller sets the POR bit to force a power on reset, all of the user flags will also be reset. In addition, if the voltage on cell-1 ever drops below the POR voltage, the contents of the user flags (as well as all other register values) could be lost.

Serial Interface

INTERFACE CONVENTIONS

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the ISL94200 devices operate as slaves in all applications.

When sending or receiving data, the convention is the most significant bit (MSB) is sent first. So, the first address bit sent is Bit 7.

CLOCK AND DATA

Data states on the SDA line can change only while SCL is LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 8.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 9.

STOP CONDITION

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition is only issued after the transmitting device has released the bus. See Figure 9.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge that it received the eight bits of data. See Figure 10.

The device responds with an acknowledge after recognition of a start condition and the correct slave byte. If a write operation is selected, the device responds with an acknowledge after the receipt of each subsequent eight bits. The device acknowledges all incoming data and address bytes, except for the slave byte when the contents do not match the device's internal slave address.

In the read mode, the device transmits eight bits of data, releases the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device terminates further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

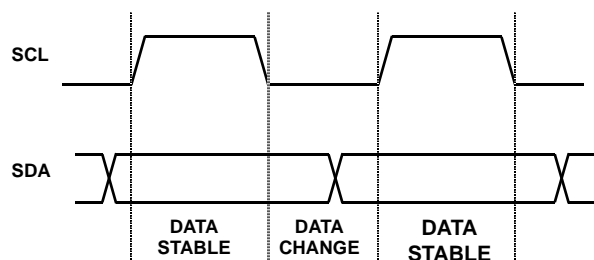


FIGURE 8. VALID DATA CHANGES ON I²C BUS

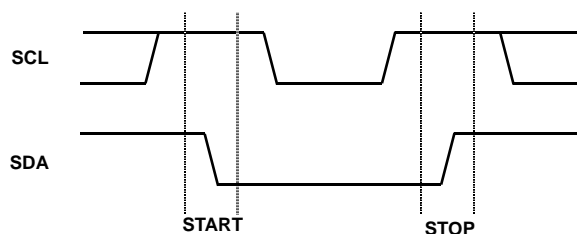


FIGURE 9. I²C START AND STOP BITS

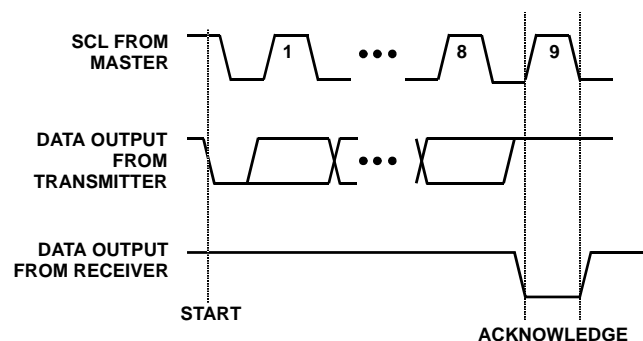


FIGURE 10. ACKNOWLEDGE RESPONSE FROM RECEIVER

WRITE OPERATIONS

For a write operation, the device requires a slave byte and an address byte. The slave byte specifies the particular device on the I²C bus that the master is writing to. The address specifies one of the registers in that device. After receipt of each byte, the device responds with an acknowledge, and awaits the next eight bits from the master. After the acknowledge, following the transfer of data, the master terminates the transfer by generating a stop condition. See Figure 11.

When receiving data from the master, the value in the data byte is transferred into the register specified by the address byte on the falling edge of the clock following the 8th data bit.

After receiving the acknowledge after the data byte, the device automatically increments the address. So, before sending the stop bit, the master may send additional data to the device without re-sending the slave and address bytes. After writing to address 0AH, the address “wraps around” to address 0. Do not continue to write to addresses higher than address 08H, since these addresses access registers that are reserved. Writing to these locations can result in unexpected device operation.

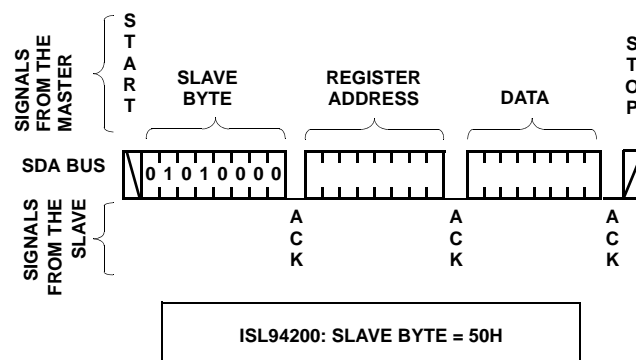


FIGURE 11. WRITE SEQUENCE

Read Operations

Read operations are initiated in the same manner as write operations with the host sending the address where the read is to start (but no data). Then, the host sends an ACK, a repeated start, and the slave byte with the LSB = 1. After the device acknowledges the slave byte, the device sends out one bit of data for each master clock. After the slave sends eight bits to the master, the master sends a NACK (Not acknowledge) to the device, to indicate the data transfer is complete, then the master sends a stop bit. See Figure 12.

After sending the eighth data bit to the master, the device automatically increments its internal address pointer. So the master, instead of sending a NACK and the stop bit, can send additional clocks to read the contents of the next register - without sending another slave and address byte.

If the last address read or written is known, the master can initiate a current address read. In this case, only the slave byte is sent before data is returned. (See Figure 12.)

Register Protection

The Discharge Set, Charge Set, and Feature Set configuration registers are write protected on initial power up. In order to write to these registers it is necessary to set a bit to enable each one. These write enable bits are in the Write Enable register (Address 08H).

Write the FSETEN bit (Addr 8:bit 7) to “1” to enable changes to the data in the Feature Set register (Address 7).

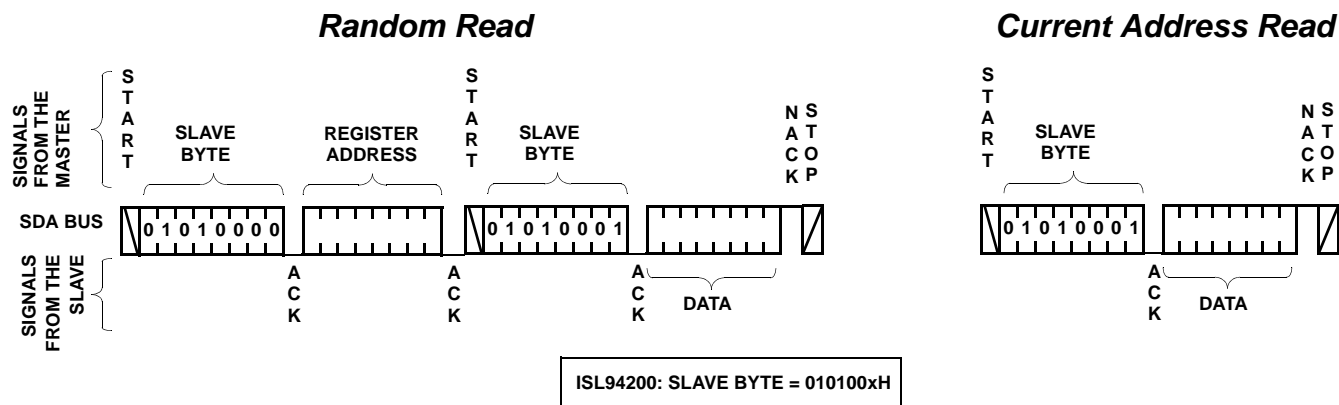


FIGURE 12. READ SEQUENCE

Write the CHSETEN bit (Addr 8:bit 6) to “1” to enable changes to the data in the Feature Set register (Address 6).

Write the DISSETEN bit (Addr 8:bit 5) to “1” to enable changes to the data in the Feature Set register (Address 5).

The microcontroller can reset these bits back to zero to prevent inadvertent writes that change the operation of the pack.

Operation State Machine

Figure 13 shows a device state machine which defines how the ISL94200 responds to various conditions.

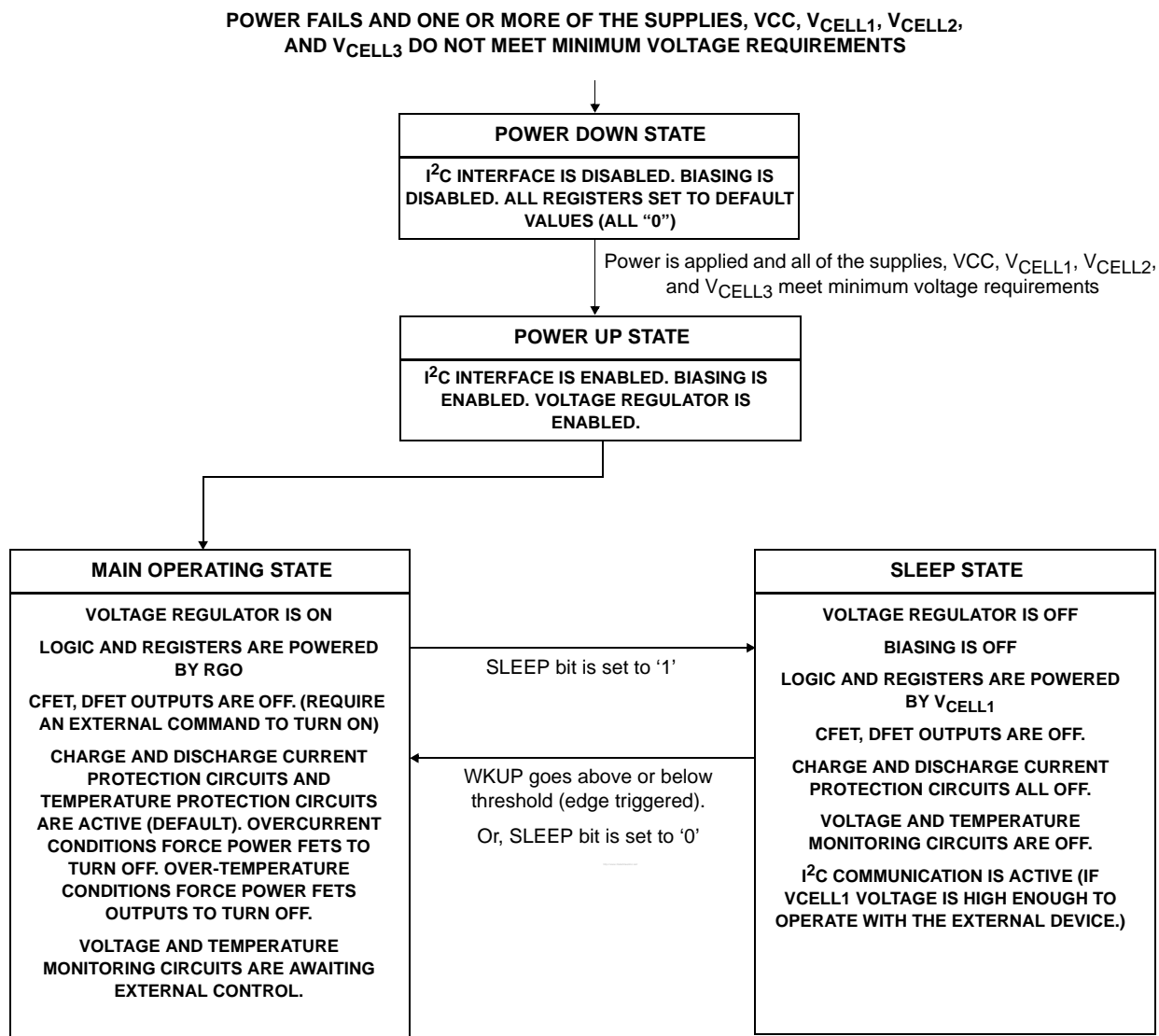


FIGURE 13. DEVICE OPERATION STATE MACHINE



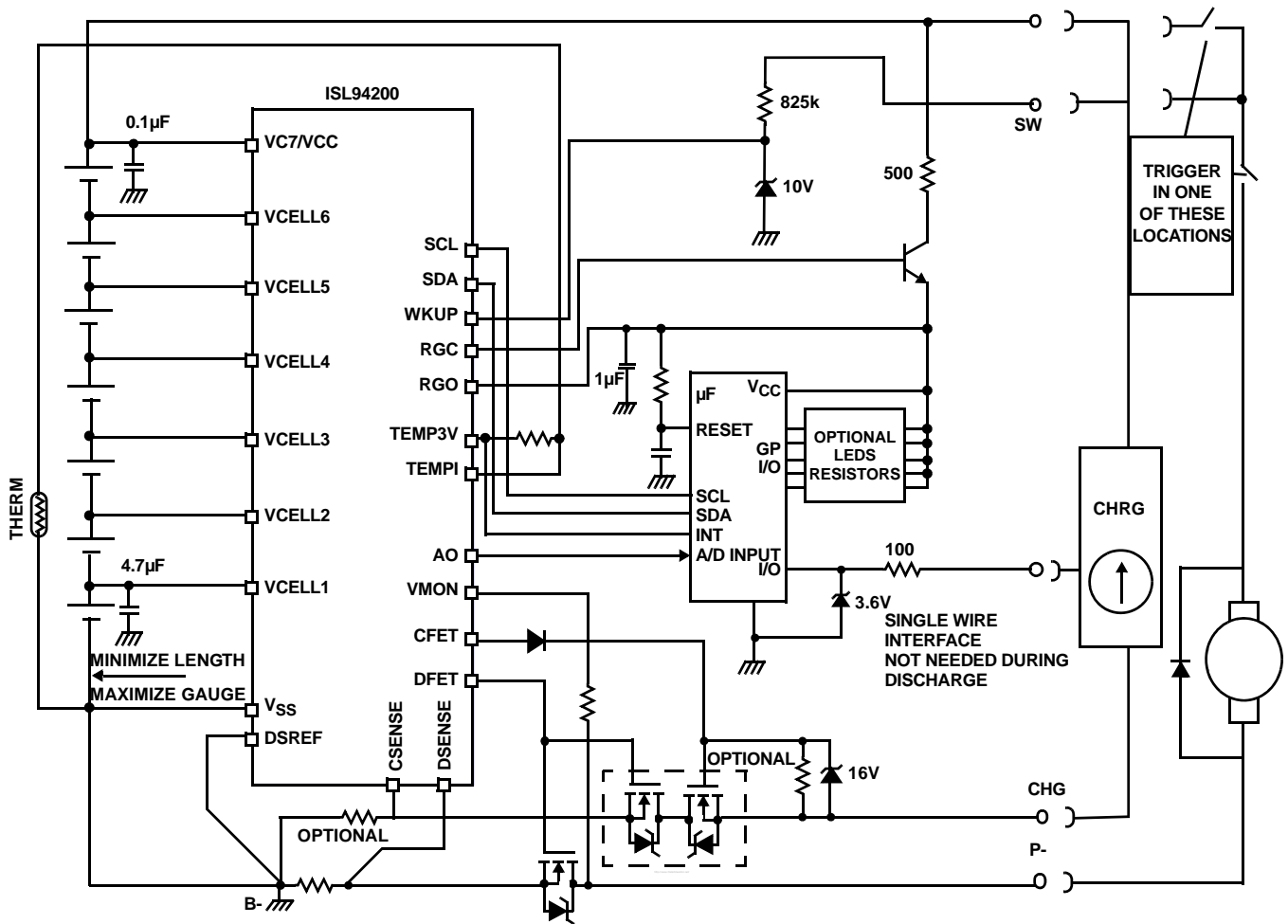


FIGURE 16. 7-CELL APPLICATION CIRCUIT WITH SWITCH WAKE-UP AND SEPARATE CHARGE/DISCHARGE

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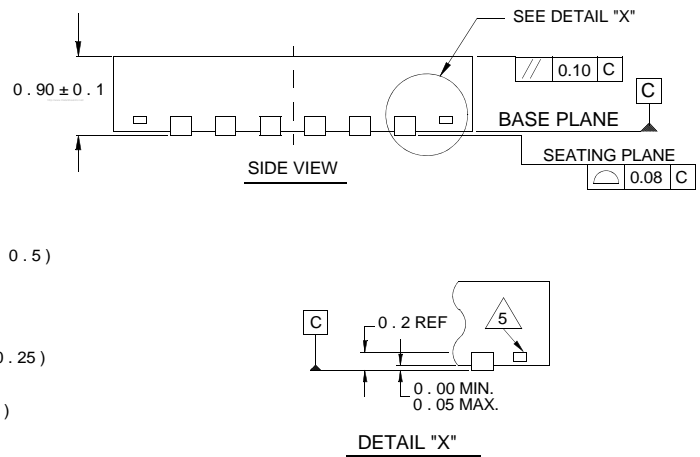
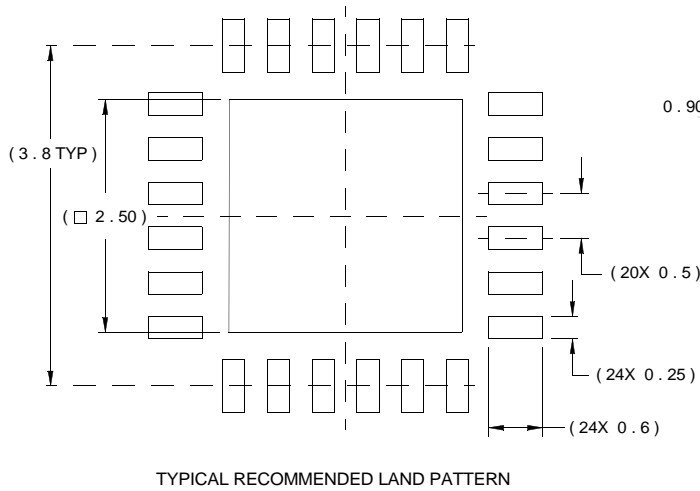
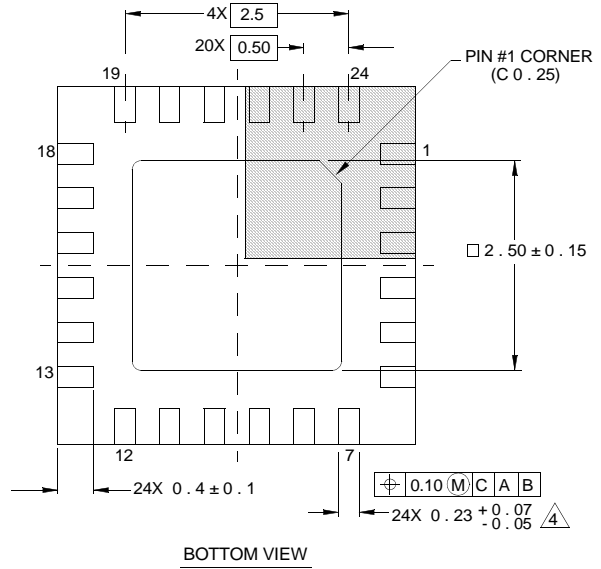
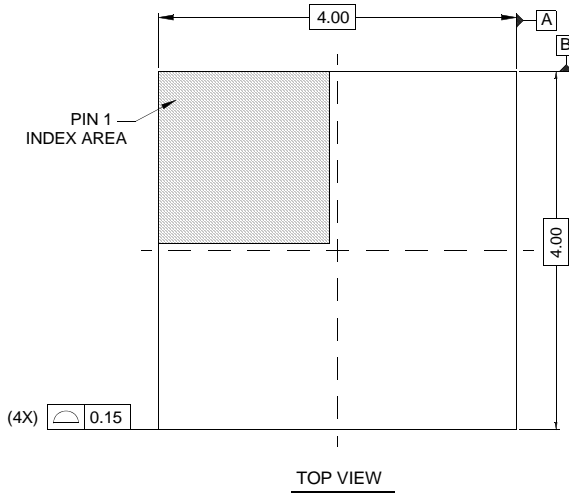
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Package Outline Drawing

L24.4x4D

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 2, 10/06



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.