ISL84516, ISL84517

Low-Voltage, Dual Supply, SPST, Analog Switches

FN6030
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Low-Voltage, Dual Supply, SPST, Analog Switches

The Intersil ISL84516 and ISL84517 devices are precision, analog switches designed to operate from ±1.5V to ±6V supplies. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (350mW), low leakage currents, and fast switching speeds. Additionally, excellent R_{ON} flatness maintains signal fidelity over the whole input range, while micro packaging alleviates board space limitations.

The ISL8451X are single-pole/single-throw (SPST) switches, with the ISL84516 being normally open (NO), and the ISL84517 being normally closed (NC).

Table 1 summarizes the performance of this family. For higher performance, pin compatible versions, see the ISL43112, ISL43113 data sheet. For single supply versions, see the ISL84514, ISL84515 data sheet.

TABLE 1. FEATURES AT A GLANCE

	ISL84516	ISL84517
Number of Switches	1	1
Configuration	NO	NC
±5V R_{ON}	13Ω	13Ω
±5V t_{ON}/t_{OFF}	40ns / 30ns	40ns / 30ns
Packages	8 Ld SOIC, 5 Ld SOT-23	

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Application Note AN557 "Recommended Test Procedures for Analog Switches"

Features

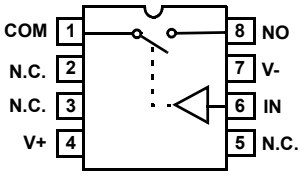
- Drop-in Replacements for MAX4516 and MAX4517 at V_S = ±5V
- Available in SOT-23 Packaging
- Dual Supply Operation . . . . . ±1.5V to ±6V
- ON Resistance (R_{ON} Max). 20Ω
- R_{ON} Flatness 3Ω
- Charge Injection . . . . . 20pC (Max)
- Low Leakage Current (Max at 85°C) . 20nA (Off Leakage) . . . . . 40nA (On Leakage)
- Fast Switching Action
  - t_{ON} (Max) 100ns
  - t_{OFF} (Max) 75ns
- Minimum 2000V ESD Protection per Method 3015.7
- CMOS Logic Compatible
- Pb-Free Available (RoHS Compliant)

Applications

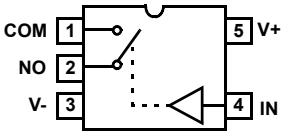
- Battery Powered, Handheld, and Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrustructure
- Medical Equipment
  - Ultrasound, MRI, CAT/PET SCAN
  - Electrocardiograph, Blood Analyzer
- Test Equipment
  - Logic and Spectrum Analyzers
  - Portable Meters, DVM, DMM
- Audio and Video Switching
- General Purpose Circuits
  - Low Voltage DACs and ADCs
  - Sample and Hold Circuits
  - Digital Filters
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Pinouts (Note 1)

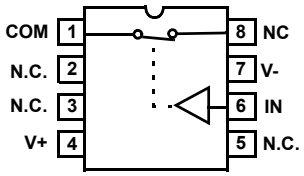
ISL84516 (SOIC)
TOP VIEW



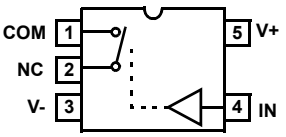
ISL84516 (SOT-23)
TOP VIEW



ISL84517 (SOIC)
TOP VIEW



ISL84517 (SOT-23)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL84516	ISL84517
0	OFF	ON
1	ON	OFF

NOTE: Logic “0” ≤ 1.5V; Logic “1” ≥ 3.5V at V_S = ±5V

Pin Descriptions

PIN	FUNCTION
V+	System Positive Power Supply Input (+1.5V to +6V)
V-	System Negative Power Supply Input (-1.5V to -6V)
IN	CMOS Compatible Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Ordering Information

PART NO. (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL84516IB	-40 to 85	8 Ld SOIC	M8.15
ISL84516IB-T	8 Ld SOIC Tape and Reel		M8.15
ISL84516IBZ (Note)	-40 to 85	8 Ld SOIC (Pb-free)	M8.15
ISL84516IBZ-T (Note)	8 Ld SOIC Tape and Reel (Pb-free		M8.15

Ordering Information (Continued)

PART NO. (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL84516IH-T (516I)	5 Ld SOT-23, Tape and Reel		P5.064
ISL84516IHZ-T (516I) (Note)	5 Ld SOT-23, Tape and Reel (Pb-free)		P5.064
ISL84517IB	-40 to 85	8 Ld SOIC	M8.15
ISL84517IB-T	8 Ld SOIC, Tape and Reel		M8.15
ISL84517IBZ (Note)	-40 to 85	8 Ld SOIC (Pb-free)	M8.15
ISL84517IBZ-T (Note)	8 Ld SOIC, Tape and Reel (Pb-free)		M8.15
ISL84517IH-T (517I)	5 Ld SOT-23, Tape and Reel		P5.064
ISL84517IHZ-T (517I) (Note)	5 Ld SOT-23, Tape and Reel (Pb-free)		P5.064

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to 15V
Input Voltages
IN (Note 2). . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
NO, NC (Note 2) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Output Voltages
COM (Note 2) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Continuous Current (Any Terminal) 20mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 30mA
ESD Rating (Per MIL-STD-883 Method 3015). . . . . >2kV

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (^{o}C/W)
5 Ld SOT-23 Package 225
8 Ld SOIC Package 170
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Moisture Sensitivity (See Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Storage Temperature Range. . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(Lead Tips Only)

Operating Conditions

Temperature Range
ISL8451XIX . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NO, NC, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, V_{INH} = 3.5V, V_{INL} = 1.5V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	V-	-	V+	V
ON Resistance, R_{ON}	V_S = ±5V, I_{COM} = 1.0mA, V_{COM} = 3V (See Figure 4)	25	-	13	20	Ω
		Full	-	-	25	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±5V, I_{COM} = 1.0mA, V_{COM} = -3V, 0V, 3V	25	-	3	4	Ω
		Full	-	4	6	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V (Note 6)	25	-1	0.01	1	nA
		Full	-20	-	20	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V (Note 6)	25	-1	0.01	1	nA
		Full	-20	-	20	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V (Note 6)	25	-2	0.01	2	nA
		Full	-40	-	40	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	(V+) - 1.5	-	V+	V
Input Voltage Low, V_{INL}		Full	V-	-	(V+) - 3.5	V
Input Current, I_{INH}, I_{INL}	V_S = ±5.5V, V_{IN} = 0V or V+	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to V+ (See Figure 1)	25	-	40	100	ns
		Full	-	-	150	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to V+ (See Figure 1)	25	-	30	75	ns
		Full	-	-	125	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	10	20	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz (See Figure 3)	25	-	>86	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	9	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	9	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	22	-	pF

Electrical Specifications - ±5V Supply Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, V_{INH} = 3.5V, V_{INL} = 1.5V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	±1.5	-	±6	V
Positive Supply Current, I+	V_S = ±5.5V, V_{IN} = 0V or V+, Switch On or Off	25	-	40	125	µA
		Full	-	-	200	µA
Negative Supply Current, I-	V_S = ±5.5V, V_{IN} = 0V or V+, Switch On or Off	25	-125	30	-	µA
		Full	-200	-	-	µA

NOTES:

4. V_{IN} = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25°C.

Test Circuits and Waveforms

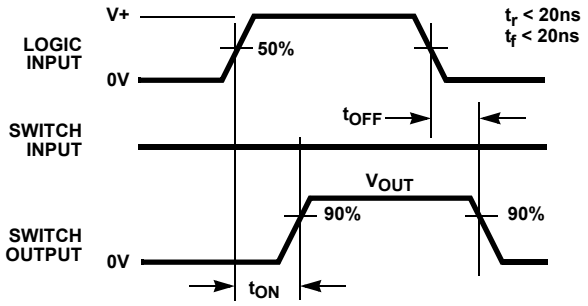


FIGURE 1A. MEASUREMENT POINTS

Logic input waveform is inverted for switches that have the opposite logic sense.

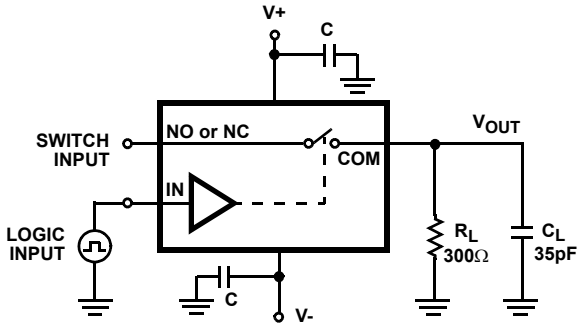


FIGURE 1B. TEST CIRCUIT

C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1. SWITCHING TIMES

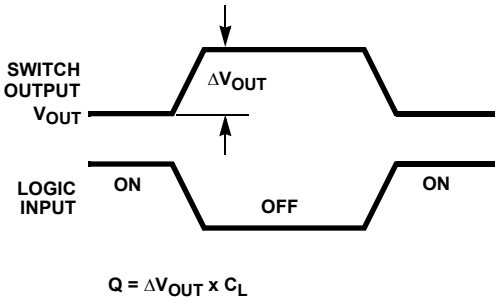


FIGURE 2A. MEASUREMENT POINTS

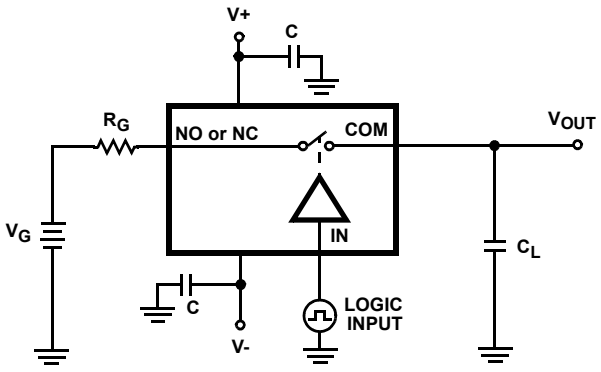


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

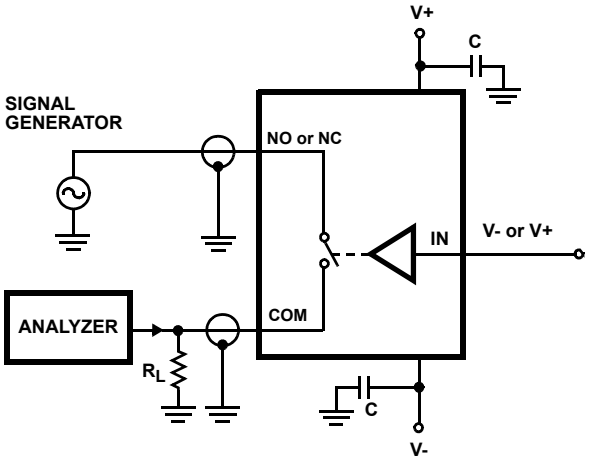


FIGURE 3. OFF ISOLATION TEST CIRCUIT

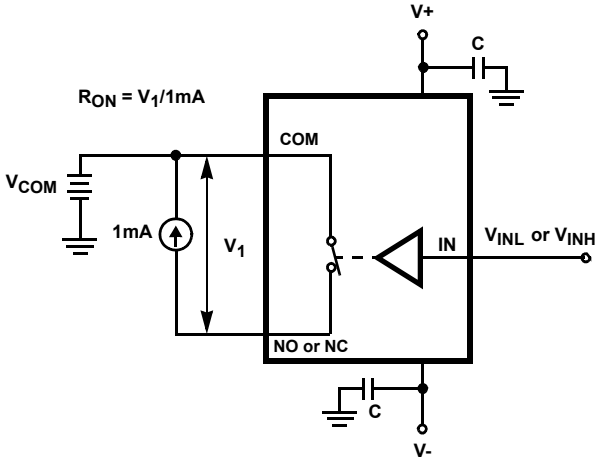


FIGURE 4. R_{ON} TEST CIRCUIT

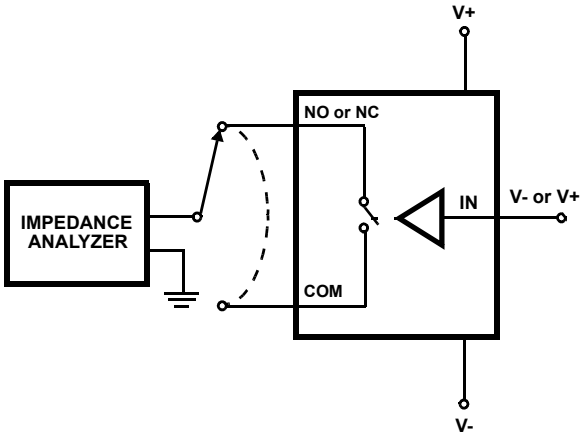


FIGURE 5. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL84516 and ISL84517 analog switches offer precise switching capability from ±1.5V to ±6V supplies with low on-resistance (13Ω) and high speed operation (t_{ON} = 40ns, t_{OFF} = 30ns). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (±1.5V), low power consumption (350µW), low leakage currents (2nA max), and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 6). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 6). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 6). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this

approach, but the switch resistance may increase, especially at low supply voltage.

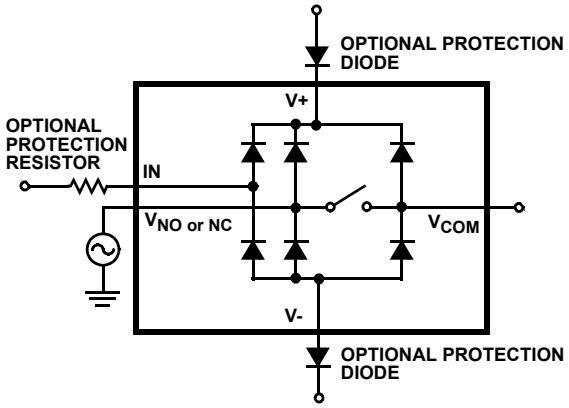


FIGURE 6. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL8451X construction is typical of most CMOS analog switches, except that there are only two supply pins: V+ and V- . The power supplies need not be symmetrical for useful operation. As long as the total supply voltage (V+ to V-, including supply tolerances, overshoot, and noise spikes) is less than the15V maximum supply rating, and the digital input switching point remains reasonable (see “Logic-Level Thresholds” section), the ISL84516, ISL84517 function well. The 15V maximum supply rating provides the designer of 12V systems much greater flexibility than switches with a 13V maximum supply voltage.

The minimum recommended supply voltage is ±1.5V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages, and the digital input V_{IL} becomes negative at $V_S \leq \pm 2V$. Refer to the “Typical Performance” curves for details.

V+ and V- power the internal CMOS switches and set their analog voltage limits. These supplies also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

This family of switches is not recommended for single supply applications. For single supply, similar performance, pin compatible, TTL compatible versions of these switches, see the ISL84514, ISL84515 data sheet.

Logic-Level Thresholds

Due to the lack of a GND pin, the switching point of the digital input is referenced predominantly to V+. The digital input is CMOS compatible at ±5V supplies, and is TTL compatible for ±3.3V supplies. For other supply combinations refer to Figure 11.

The switching point has a very low temperature sensitivity, and changes by only 100mV from 85ºC to -40ºC, regardless of supply voltage.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat to 30MHz, with a -3dB bandwidth of nearly 400MHz (see Figure 13). Figure 13 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch’s input to its output. OFF Isolation is the resistance to this feedthrough. Figure 14 details the high OFF Isolation provided by this family. At 10MHz, OFF Isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease OFF Isolation due to the voltage divider action of the switch OFF Impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog-signal paths and V+ or V-.

Typical Performance Curves $T_A = 25^oC$, $V_{IH} = V+$, $V_{IL} = 0V$, Unless Otherwise Specified

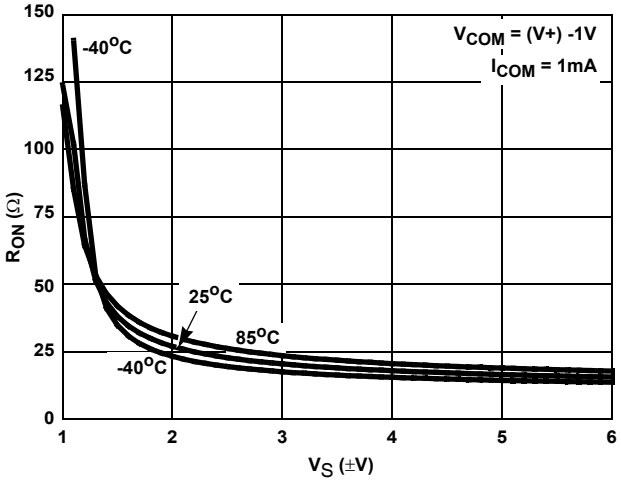


FIGURE 7. ON RESISTANCE vs SUPPLY VOLTAGE

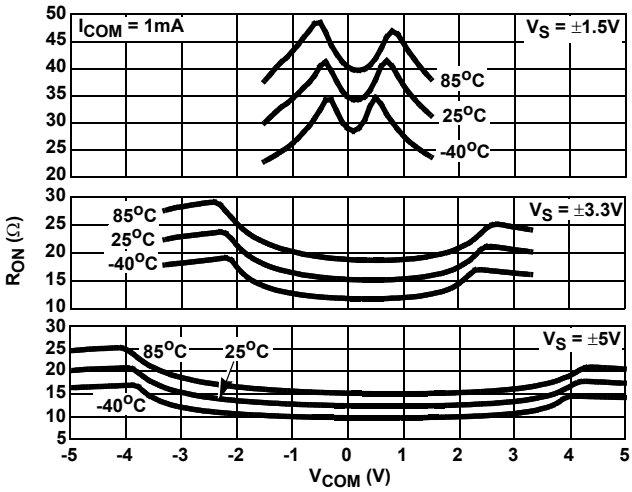


FIGURE 8. ON RESISTANCE vs SWITCH VOLTAGE

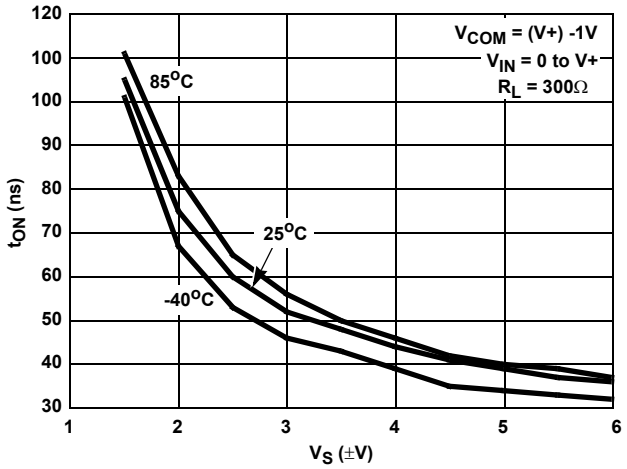


FIGURE 9. TURN - ON TIME vs SUPPLY VOLTAGE

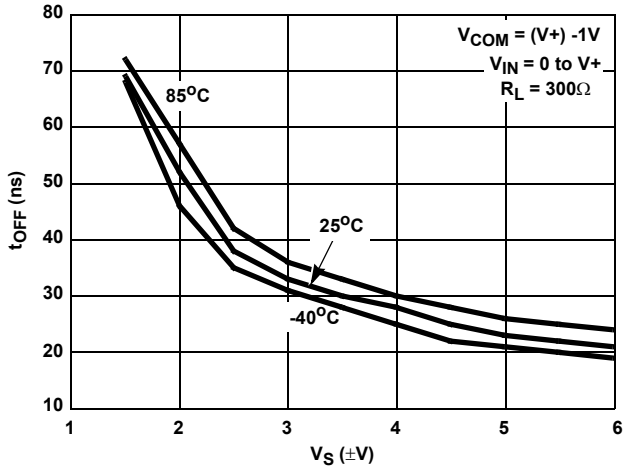


FIGURE 10. TURN - OFF TIME vs SUPPLY VOLTAGE

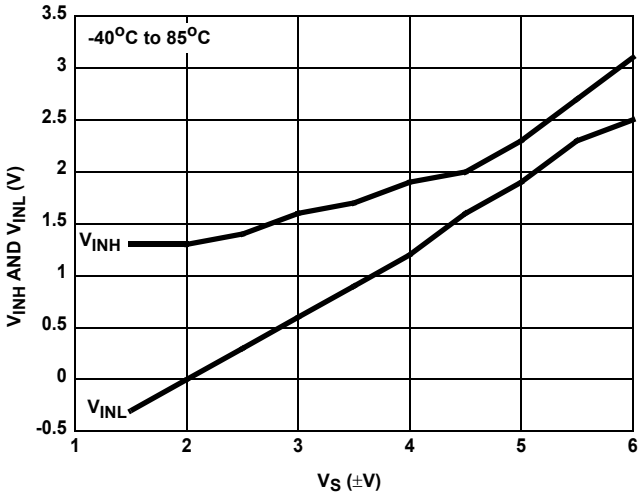


FIGURE 11. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

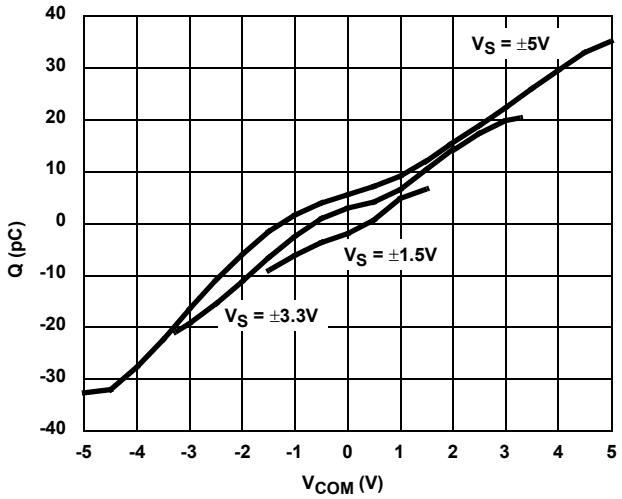


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

Typical Performance Curves $T_A = 25^oC$, $V_{IH} = V+$, $V_{IL} = 0V$, Unless Otherwise Specified **(Continued)**

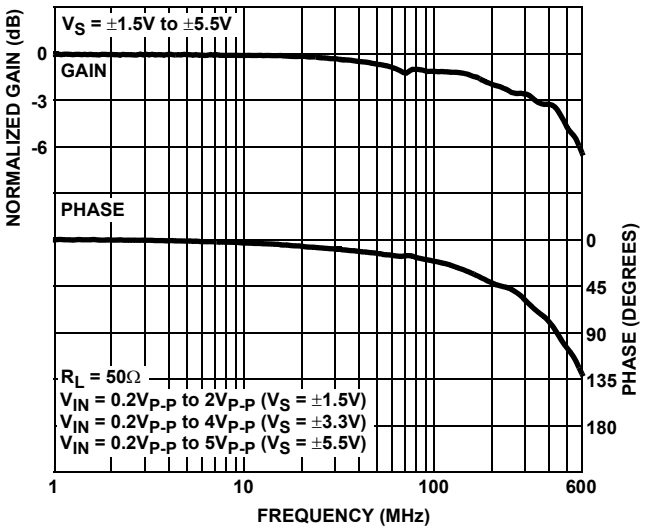


FIGURE 13. FREQUENCY RESPONSE

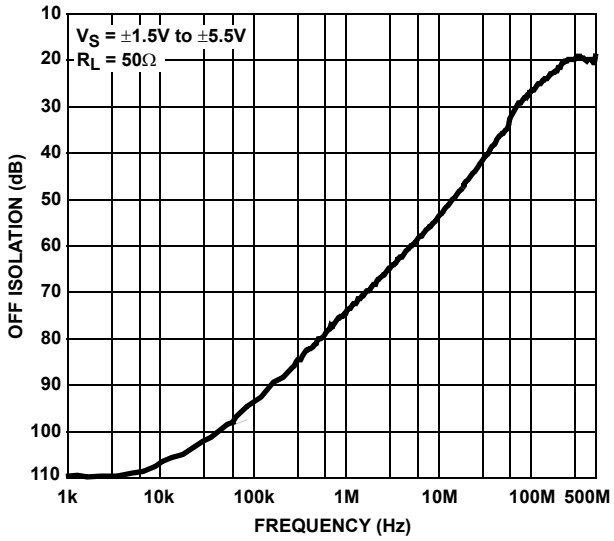


FIGURE 14. OFF ISOLATION

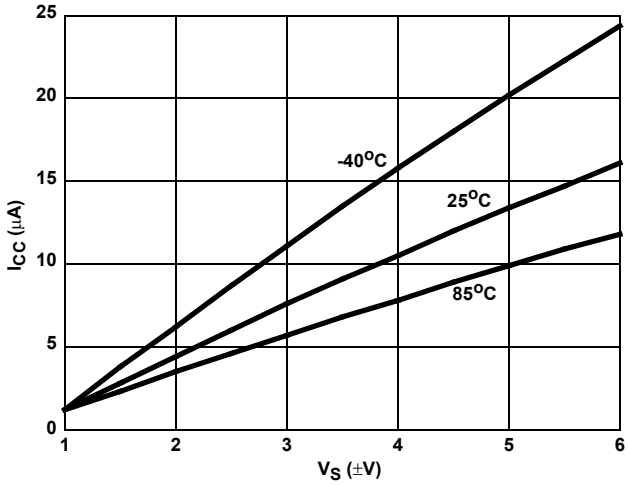


FIGURE 15. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

V-

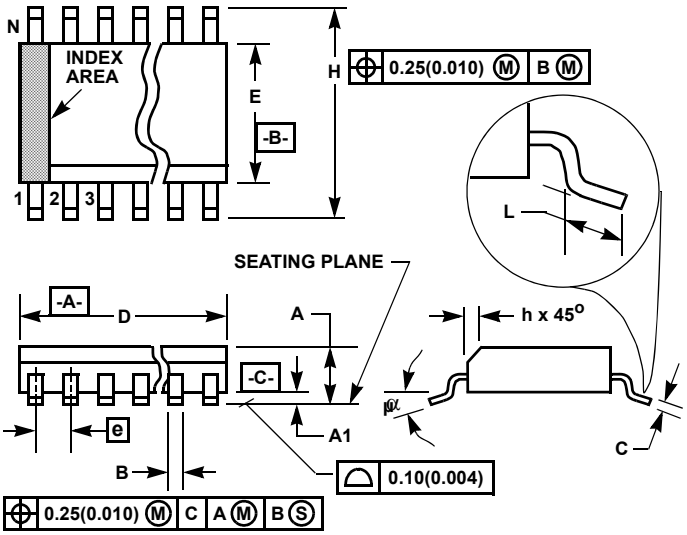
TRANSISTOR COUNT:

ISL84516: 55
ISL84517: 55

PROCESS:

Si Gate CMOS

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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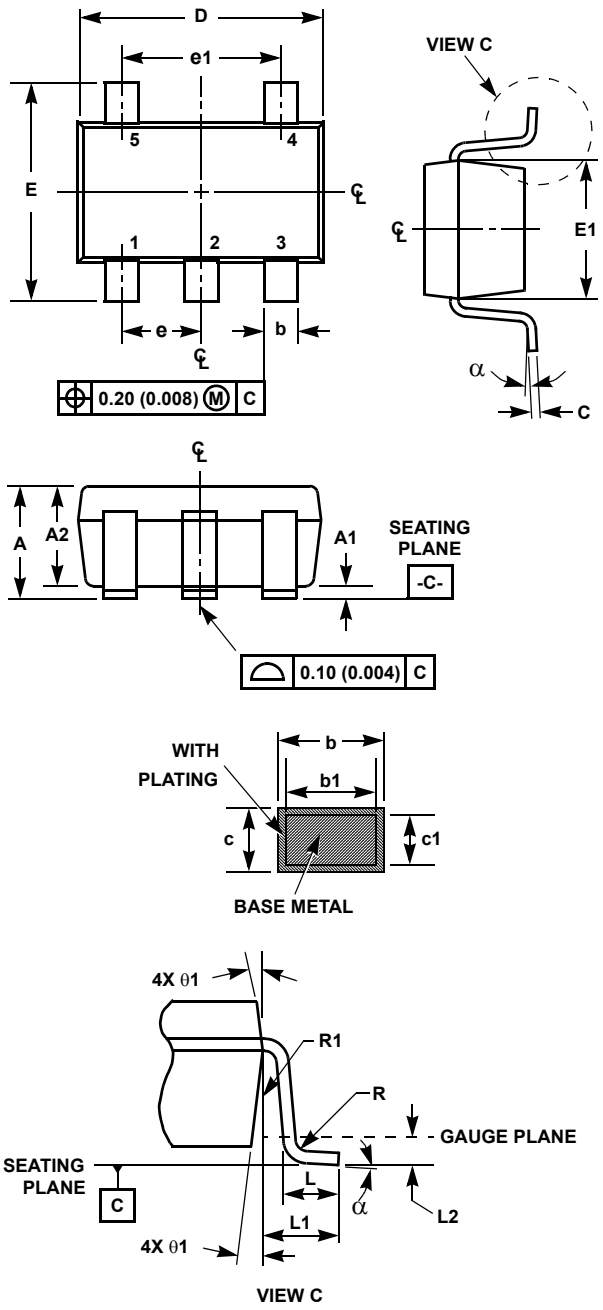
Small Outline Transistor Plastic Packages (SOT23-5)



P5.064

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.012	0.020	0.30	0.50	-
b1	0.012	0.018	0.30	0.45	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.008	0.08	0.20	6
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.067	1.50	1.70	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.90 Ref		-
L	0.014	0.022	0.35	0.55	4
L1	0.024 Ref.		0.60 Ref.		
L2	0.010 Ref.		0.25 Ref.		
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.10	0.25	
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.