ISL8273M

80A Single Channel Digital PMBus Step-Down Power Module

FN8704
Rev.4.00
Nov 9, 2017

The ISL8273M is a complete PMBus enabled DC/DC single channel step-down advance power supply capable of delivering up to 80A of current and optimized for high power density applications. For higher output current, up to four ISL8273Ms can be paralleled to supply up to 320A in a multiphase current sharing configuration.

Operating over an input voltage range of 4.5V to 14V, the ISL8273M offers adjustable output voltages down to 0.6V and achieves up to 93% conversion efficiencies. A unique ChargeMode™ control architecture provides a single clock cycle response to an output load step and can support switching frequencies up to 1MHz. The power module integrates all power and most passive components and requires only a few external components to operate. A set of optional external resistors allows the user to easily configure the device for standard operation. For advanced configurations, a standard PMBus interface addresses sequencing and fault management, as well as real-time full telemetry and point-of-load monitoring. Additionally, on-board nonvolatile memory can store the desired custom configuration and settings.

A fully customizable voltage, current, and temperature protection scheme ensures safe operation for the ISL8273M under abnormal operating conditions. The device is also supported by the PowerNavigator™ software, a full digital power train development environment.

The ISL8273M is available in a low profile compact 18mmx23mmx7.5mm fully encapsulated thermally enhanced HDA package.

Applications

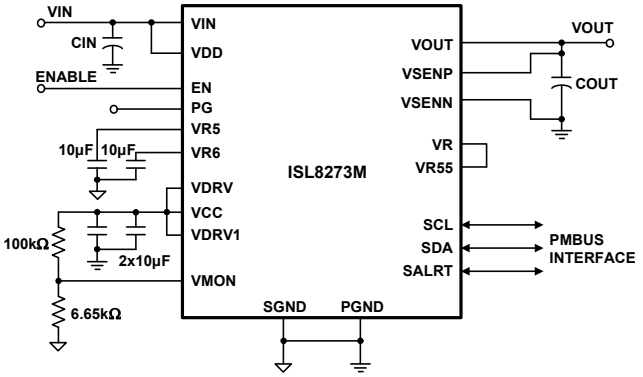
- Server, telecommunications, storage, and data communications
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

Features

- Complete digital power supply
- 80A single channel output current
  - 4.5V to 14V single rail input voltage
  - Up to 93% efficiency
  - Up to 320A/4 parallel modules capable solution
  - Multiphase and current sharing operations (180°/22.5° steps)
- Programmable output voltage
  - 0.6V to 2.5V output voltage settings
  - ±1% accuracy over line, load, and temperature
- ChargeMode control loop architecture
  - 296kHz to 1.06MHz fixed switching frequency operations
  - No compensation required
  - Fast single clock cycle transient response
- PMBus interface and/or pin-strap mode
  - Fully programmable through PMBus
  - Pin-strap mode for standard settings
  - Real-time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, and f_{SW}
- Advanced soft-start/stop, sequencing, and margining
- On-board nonvolatile memory
- Complete over/undervoltage, current, and temperature protections with fault logging
- PowerNavigator supported
- Thermally enhanced 18mmx23mmx7.5mm HDA package

Related Literature

- For a full list of related documents, visit our website
  - ISL8273M product page



NOTE: Figure 1 represents a typical implementation of the ISL8273M. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.

FIGURE 1. 80A APPLICATION CIRCUIT

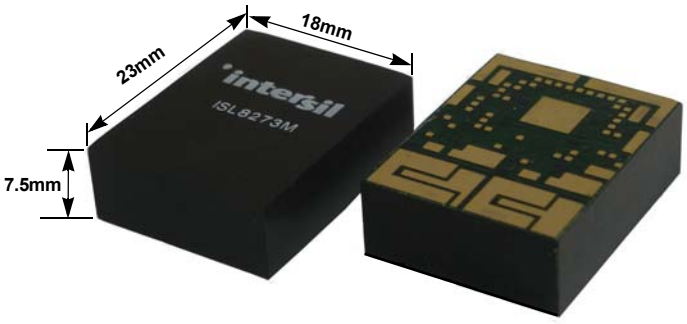


FIGURE 2. A SMALL PACKAGE FOR HIGH POWER DENSITY

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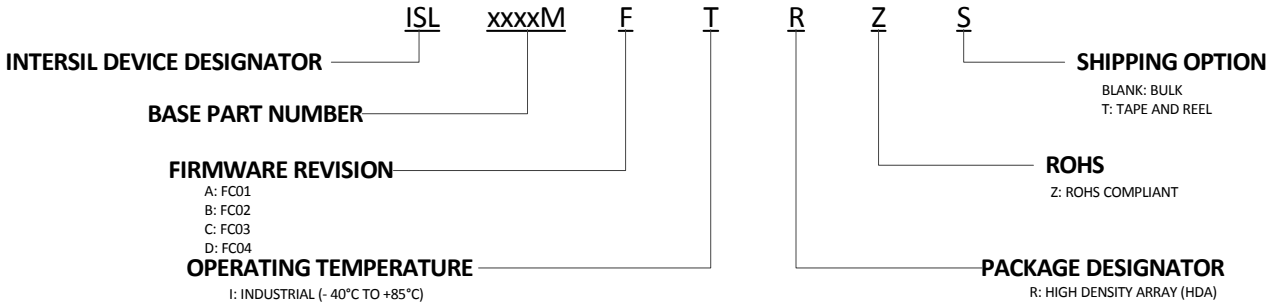
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL8273MAIRZ	ISL8273M	-40 to +85	58 LD 18x23 HDA Module	Y58.18x23
ISL8273MCIRZ	ISL8273MC	-40 to +85	58 LD 18x23 HDA Module	Y58.18x23
ISL8273MDIRZ	ISL8273MD	-40 to +85	58 LD 18x23 HDA Module	Y58.18x23
ISL8273MEVAL1Z	Single-Module Evaluation Board (see UG036, "ISL8273MEVAL1Z Evaluation Board User Guide")			

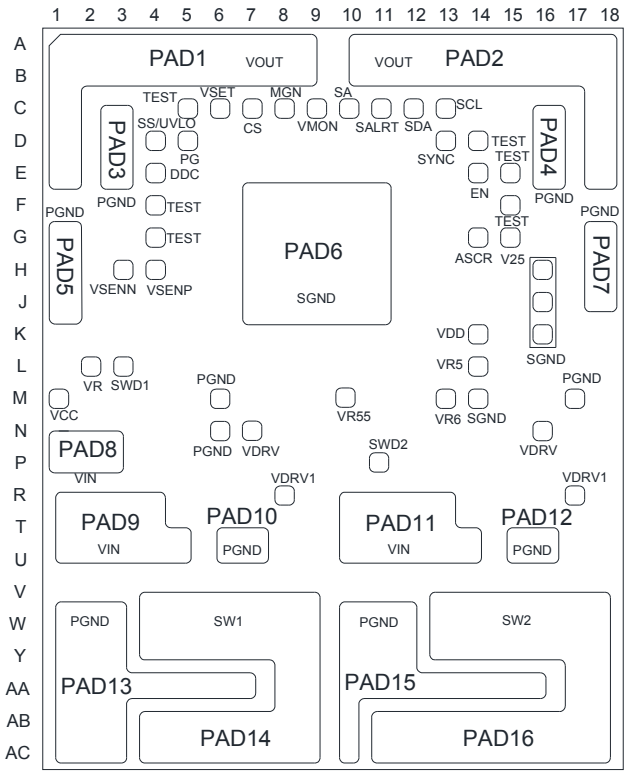
NOTES:

1. Add "-T" suffix for 100 unit tape and reel options. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL8273M product information page. For more information about MSL, refer to TB363.



Pin Configuration

ISL8273M
(58 LD HDA)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
PAD1, PAD2	VOUT	PWR	Power supply output voltage. Output voltage ranges from 0.6V to 2.5V. Tie these two pins together to achieve a single output. For higher output voltage, refer to the derating curves starting on page 15 to set the maximum output current from these pads.
PAD3, PAD4, PAD5, PAD7, PAD10, PAD12, PAD13, PAD15	PGND	PWR	Power ground. Refer to the "Layout Guide" on page 22 for the PGND pad connections and I/O capacitor placement.
PAD6	SGND	PWR	Signal ground. Refer to "Layout Guide" on page 22 for the SGND pad connections.
PAD8, PAD9, PAD11	VIN	PWR	Input power supply voltage to power the module. Input voltage ranges from 4.5V to 14V.
PAD14	SW1	PWR	Switching node pads. The SW pads dissipate the heat and provide the good thermal performance. Refer to "Layout Guide" on page 22 for the SW pad connections.
PAD16	SW2		
C6	VSET	I	Output voltage selection pin. Used to set V_{OUT} set point and V_{OUT} max.
C7	CS	I	Current sharing configuration pin. Used to program current sharing configurations such as SYNC selection, phase spreading, and V_{OUT} droop.
C8	MGN	I	External V_{OUT} margin control pin. Active high (>2V) sets V_{OUT} margin high; active low (<0.8V) sets V_{OUT} margin low; high impedance (floating) sets V_{OUT} to normal voltage. Factory default range for margining is nominal V_{OUT} ±5%. When using PMBus to control the margin, leave this pin as no connection.
C9	VMON	I	Driver voltage monitoring. Use this pin to monitor VDRV through an external 16:1 resistor divider.
C10	SA	I	Serial address selection pin. Used to assign a unique address for each individual device or to enable certain management features.
C11	SALRT	O	Serial alert. Connect to external host if desired. SALRT is asserted low upon a warning or a fault event and deasserted when the warning or fault is cleared. A pull-up resistor is required.
C12	SDA	I/O	Serial data. Connect to external host and/or to other Digital-DC™ devices. A pull-up resistor is required.
C13	SCL	I/O	Serial clock. Connect to external host and/or to other Digital-DC devices. A pull-up resistor is required.
D4	SS/ UVLO	I	Soft-start/stop and undervoltage lockout selection pin. Used to set turn on/off delay and ramp time as well as input UVLO threshold levels.
D5	PG	O	Power-good output. The power-good output can be an open drain that requires a pull-up resistor or a push-pull output that can drive a logic input.
D13	SYNC	I/O	Clock synchronization input. Used to set the frequency of the internal switch clock, to sync to an external clock, or to output an internal clock. If external synchronization is used, the external clock must be active before enable.
E14	EN	I	Enable pin. Set logic high to enable the module output.
E4	DDC	I/O	A Digital-DC bus. This dedicated bus provides the communication between devices for features such as sequencing, fault spreading, and current sharing. The DDC pin on all Digital-DC devices should be connected together. A pull-up resistor is required.
C5, D14, E15, F4, F15, G4	TEST	-	Test pins. Do not connect these pins.
G14	ASCR	I	ChargeMode control ASCR parameters selection pin. Used to set ASCR gain and residual values.
G15	V25	PWR	Internal 2.5V reference used to power internal circuitry. No external capacitor required for this pin. Not recommended to power external circuit.
H3	VSENN	I	Differential output voltage sense feedback. Connect to a negative output regulation point.
H4	VSENP	I	Differential output voltage sense feedback. Connect to a positive output regulation point.
H16, J16, K16, M14	SGND	PWR	Signal grounds. Use multiple vias to connect the SGND pins to the internal SGND layer.
K14	VDD	PWR	Input supply voltage for controller. Connect the VDD pad to the VIN supply.
L2	VR	PWR	Internal LDO bias pin. Tie VR to VR55 directly with a short loop trace. Not recommended to power the external circuit.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
L3	SWD1	PWR	Switching node driving pins. Directly connect to the SW1 and SW2 pads with short loop wires.
P11	SWD2		
L14	VR5	PWR	Internal 5V reference used to power internal circuitry. Place a 10µF decoupling capacitor for this pin. Maximum external loading current is 5mA.
M1	VCC	PWR	Internal LDO output. Connect VCC to VDRV for internal LDO driving.
M5, M17, N5	PGND	PWR	Power grounds. Use multiple vias to connect the PGND pins to the internal PGND layer.
M10	VR55	PWR	Internal 5.5V bias voltage for internal LDO use only. Tie VR55 pin directly to the VR pin. Not recommended to power external circuits.
M13	VR6	PWR	Internal 6V reference used to power internal circuitry. Place a 10µF decoupling capacitor for this pin. Not recommended to power external circuits.
N6, N16	VDRV	PWR	Power supply for internal FET drivers. Connect a 10µF bypass capacitor to each of these pins. These pins can be driven by the internal LDO through VCC pin or by the external power supply directly. Keep the driving voltage between 4.5V and 5.5V. For 5V input application, use an external supply or connect this pin to VIN.
R8, R17	VDRV1	I	Bias pin of the internal FET drivers. Always tie to VDRV.

ISL8273M Internal Block Diagram

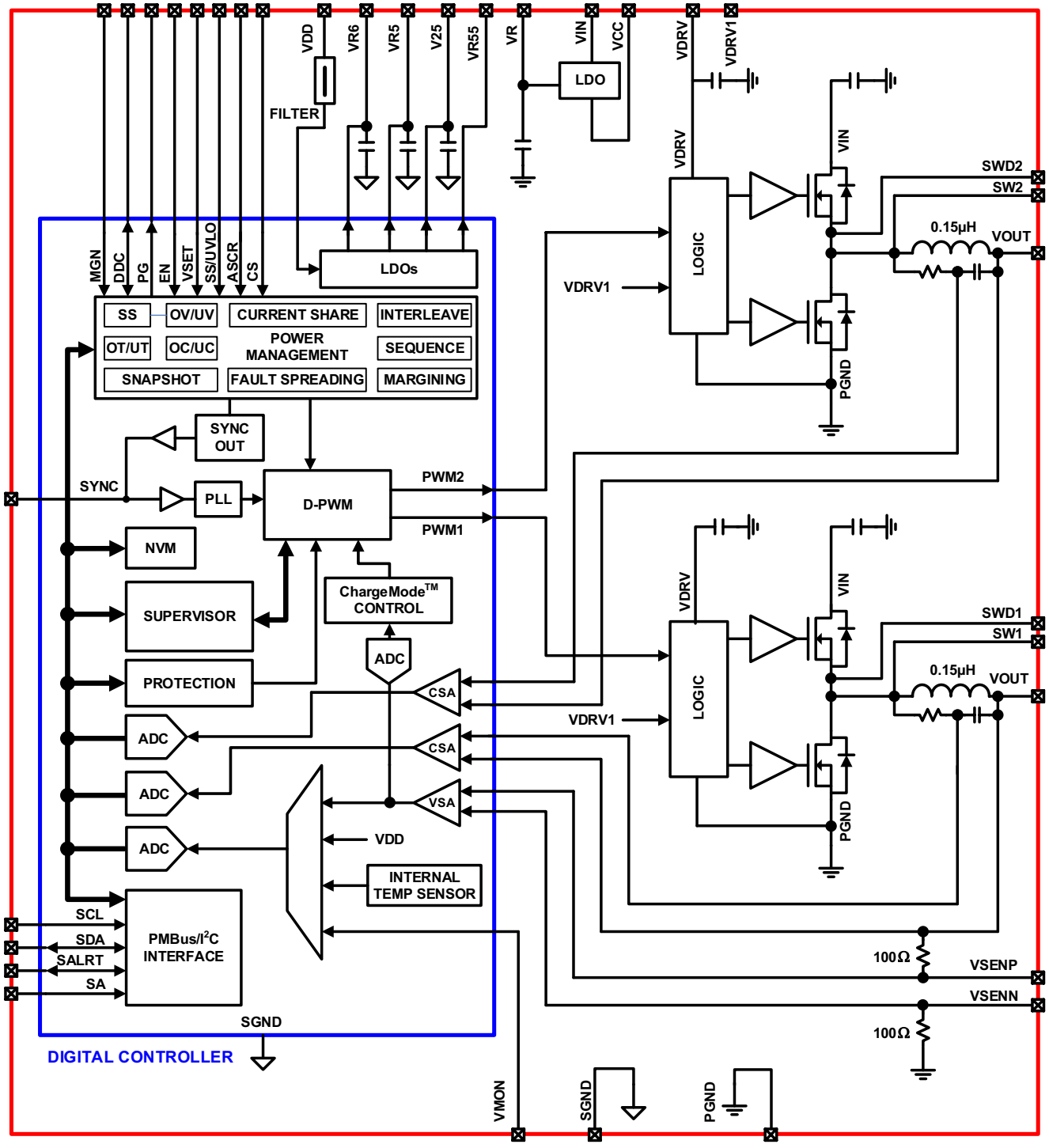
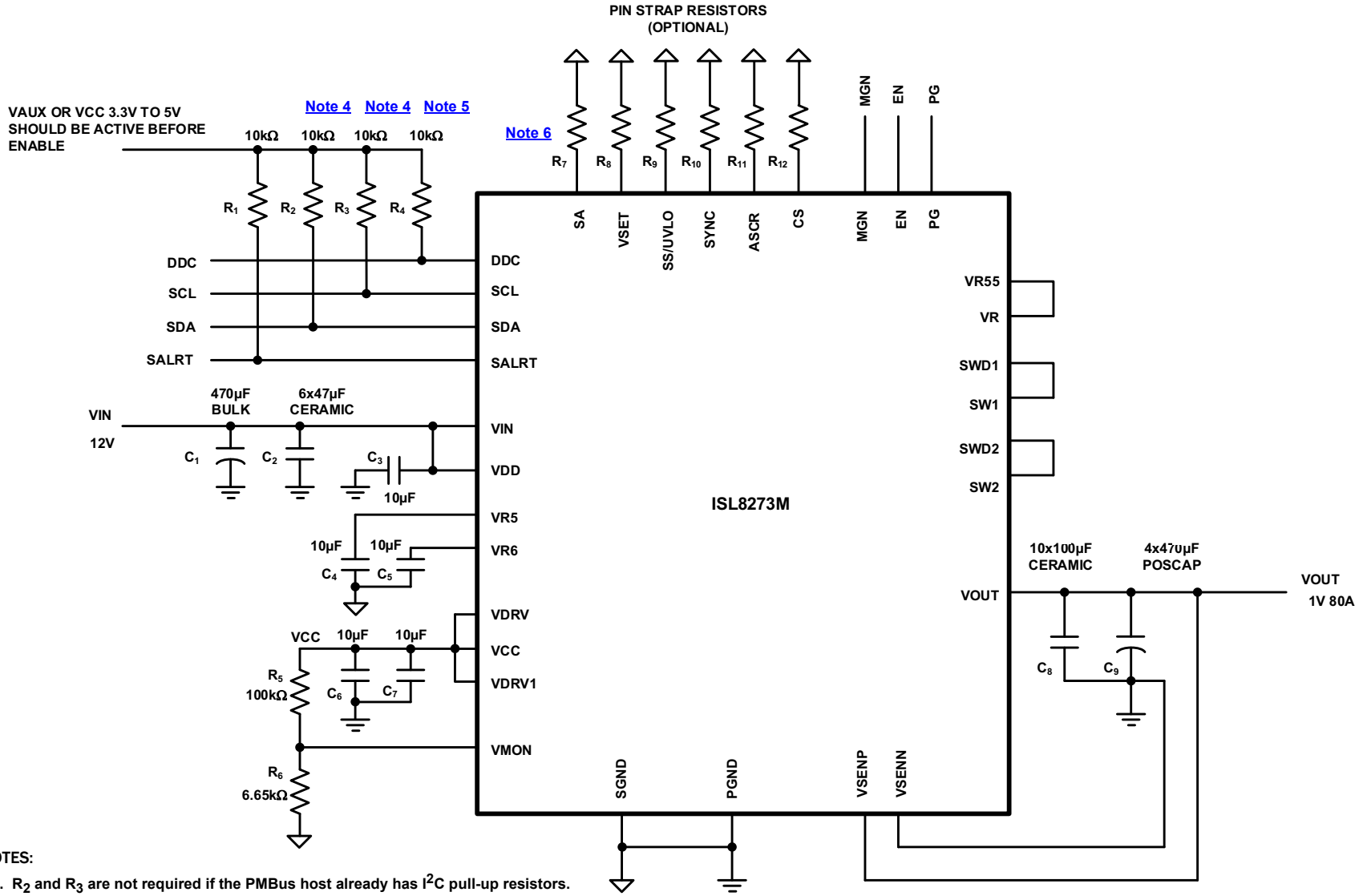


FIGURE 3. INTERNAL BLOCK DIAGRAM

Typical Application Circuit - Single Module



NOTES:

4. R_2 and R_3 are not required if the PMBus host already has I^2C pull-up resistors.
5. Only one R_4 per DDC bus is required when multiple modules share the same DDC bus.
6. R_7 through R_{12} can be selected according to the tables for the pin-strap resistor setting in this document. If the PMBus configuration is chosen to overwrite the pin-strap configuration, R_8 through R_{12} can be non-populated.
7. V25, VR and VR55 do not need external capacitors. V25 can be no connection.

FIGURE 4. TYPICAL APPLICATION CIRCUIT - SINGLE MODULE

Typical Application Circuit - Three Module Current Sharing

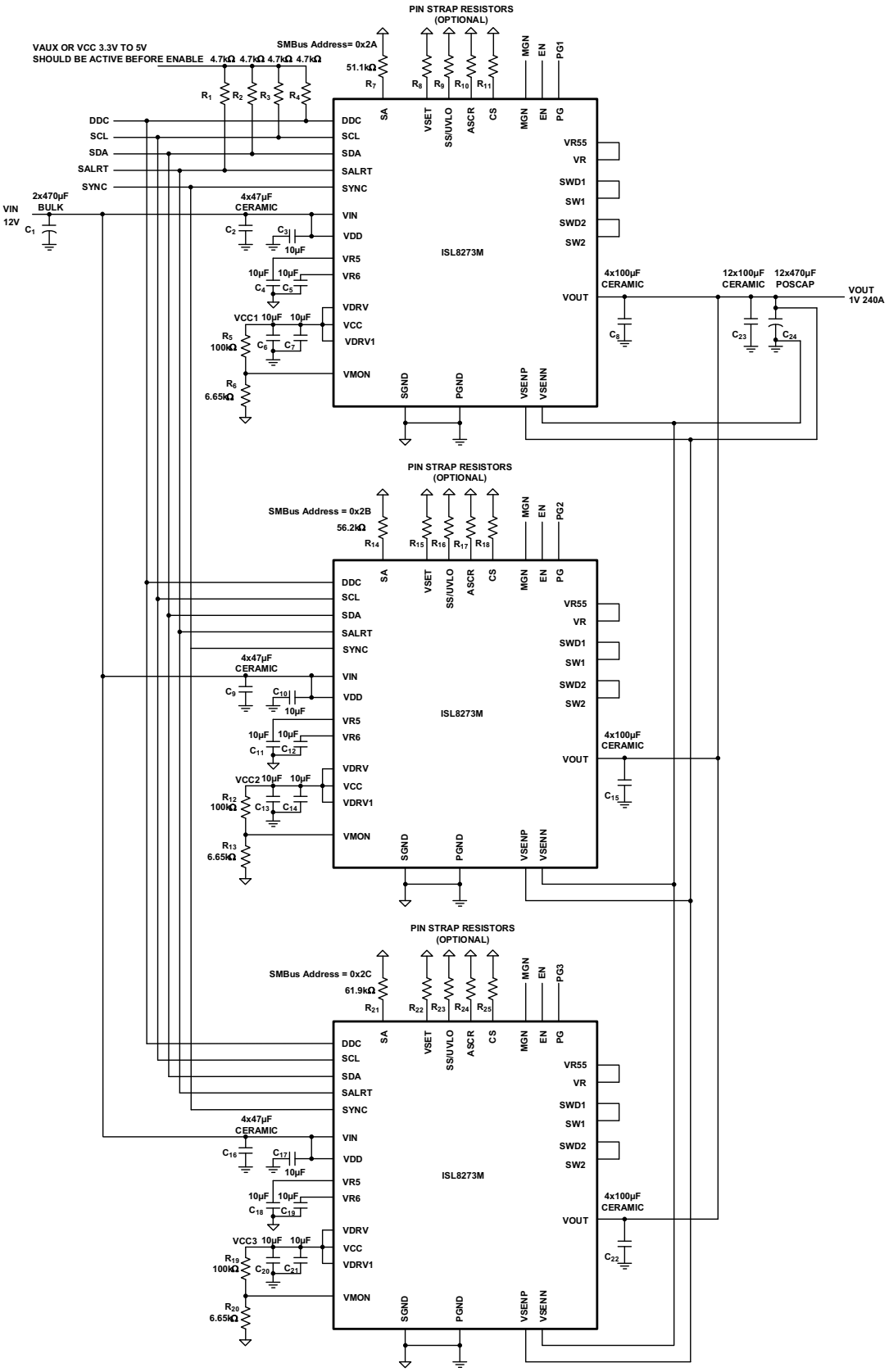


FIGURE 5. TYPICAL APPLICATION CIRCUIT - THREE MODULE CURRENT SHARING

TABLE 1. ISL8273M DESIGN GUIDE MATRIX AND OUTPUT VOLTAGE RESPONSE

V_{IN} (V)	V_{OUT} (V)	C_{IN} (BULK) (µF) (Note 8)	C_{IN} (CERAMIC) (µF)	C_{OUT} (BULK) (µF)	C_{OUT} (CERAMIC) (µF)	ASCR GAIN (Note 9)	ASCR RESIDUAL (Note 9)	VOUT DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A) (Note 10)	FREQ. (kHz)
5	1	1x470	6x47	6x470	12x100	100	90	80	25	0 to 40	300
5	1	1x470	4x47	4x470	8x100	220	90	95	20	0 to 40	571
5	1.5	1x470	6x47	6x470	14x100	110	90	82	35	0 to 40	300
5	1.5	1x470	4x47	4x470	10x100	240	90	85	20	0 to 40	571
12	1	1x470	8x47	6x470	14x100	140	90	80	30	0 to 40	300
12	1	1x470	6x47	4x470	10x100	240	90	82	20	0 to 40	571
12	1.5	1x470	8x47	6x470	12x100	140	90	85	35	0 to 40	364
12	1.5	1x470	6x47	4x470	10x100	220	90	85	30	0 to 40	571
12	2.5	1x470	8x47	4x470	8x100	180	90	105	45	0 to 40	571
12	2.5	1x470	6x47	3x470	6x100	220	90	110	40	0 to 40	800

NOTES:

8. C_{IN} bulk capacitor is optional only for energy buffer from the long input power supply cable.
9. ASCR gain and residual are selected to ensure phase margin higher than 60° and gain margin higher than 6dB at ambient room temperature and full load (80A).
10. Output voltage response is tested with load step slew rate higher than 100A/µs.

TABLE 2. RECOMMENDED INPUT/OUTPUT CAPACITOR

VENDORS	VALUE	PART NUMBER
MURATA, Input Ceramic	47µF, 16V, 1210	GRM32ER61C476ME15L
MURATA, Input Ceramic	22µF, 16V, 1210	GRM32ER61E226KE15L
TAIYO YUDEN, Input Ceramic	47µF, 16V, 1210	EMK325BJ476MM-T
TAIYO YUDEN, Input Ceramic	22µF, 25V, 1210	TMK325BJ226MM-T
MURATA, Output Ceramic	100µF, 6.3V, 1210	GRM32ER60J107M
TDK, Output Ceramic	100µF, 6.3V, 1210	C3225X5R0J107M
AVX, Output Ceramic	100µF, 6.3V, 1210	12106D107MAT2A
SANYO POSCAP, Output Bulk	470µF, 4V	4TPE470MCL
SANYO POSCAP, Output Bulk	470µF, 6.3V	6TPF470MAH
PANASONIC, Input Bulk	150µF, 16V	16TQC150MYF

Absolute Maximum Ratings

Input Supply Voltage, VIN Pin . . . . . -0.3V to 17V
Input Supply Voltage for Controller, VDD Pin . . . . . -0.3V to 17V
MOSFET Switch Node Voltage, SW1/2, SWD1/2 . . . . . -0.3V to 17V
MOSFET Driver Supply Voltage, VDRV, VDRV1 Pin . . . . . -0.3V to 6.0V
Output Voltage, VOUT pin. . . . . -0.3V to 6.0V
Internal Reference Supply Voltage, VR6 Pin . . . . . -0.3V to 6.6V
Internal Reference Supply Voltage, VR, VR5, VR55 Pin. . . . . -0.3V to 6.5V
Internal Reference Supply Voltage, V25 Pin . . . . . -0.3V to 3V
Logic I/O Voltage for DDC, EN, MGN, PG, ASCR, CS
SA, SCL, SDA, SALRT, SYNC, SS/UVLO, VMON, VSET . . . . . -0.3V to 6.0V
Analog Input Voltages
VSENP . . . . . -0.3V to 6.0V
VSENN . . . . . -0.3V to 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per JESD22-C110D) 750V
Latch-up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
58 LD HDA Package (Notes 11, 12).	5.3	1.1

Maximum Junction Temperature (Plastic Package) . . . . . +125°C
Storage Temperature Range. . . . . -55°C to +150°C
Pb-free Reflow Profile . . . . . see Figure 28

Recommended Operating Conditions

Input Supply Voltage Range, V_{IN} . . . . . 4.5V to 14V
Input Supply Voltage Range for Controller, V_{DD} . . . . . 4.5V to 14V
Output Voltage Range, V_{OUT} . . . . . 0.6V to 2.5V
Output Current Range, $I_{OUT(DC)}$ (Note 15). . . . . 0A to 80A
Operating Junction Temperature Range, T_J. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

11. θ_{JA} is measured in free air with the module mounted on an 8-layer evaluation board 4.7x4.8inch in size with 2oz Cu on all layers and multiple via interconnects as specified in the ISL8273MEVAL1Z evaluation board user guide.
12. For θ_{JC}, the "case temp" location is the center of the package underside.

Electrical Specifications

$V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
INPUT AND SUPPLY CHARACTERISTICS						
Input Supply Current for Controller	I_{DD}	$V_{IN} = V_{DD} = 12V$, $V_{OUT} = 0V$, module not enabled		40	**50**	mA
6V Internal Reference Supply Voltage	V_{R6}		**5.5**	6.1	**6.6**	V
5V Internal Reference Supply	V_{R5}	I_{VR5} <5mA	**4.5**	5.2	**5.5**	V
2.5V Internal Reference Supply	V_{25}		**2.25**	2.5	**2.75**	V
Internal LDO Output Voltage	Vcc			5.3		V
Internal LDO Output Current	I_{VCC}	$V_{IN} = V_{DD} = 12V$, V_{CC} connected to VDRV, module enabled	**50**			mA
Input Supply Voltage for Controller Read Back Resolution	$V_{DD\_READ\_RES}$			±20		mV
Input Supply Voltage for Controller Read Back Total Error (Note 16)	$V_{DD\_READ\_ERR}$	PMBus Read		±2		% FS
OUTPUT CHARACTERISTICS						
Output Voltage Adjustment Range	V_{OUT_RANGE}	$V_{IN} > V_{OUT} + 1.8V$	**0.54**		**2.75**	V
Output Voltage Set-Point Range	V_{OUT_RES}	Configured using PMBus		±0.025		%
Output Voltage Set-Point Accuracy (Notes 14, 16)	V_{OUT_ACCY}	Includes line, load, and temperature (-20°C ≤ TA ≤ +85°C)	**-1**		**+1**	% FS
Output Voltage Read Back Resolution	$V_{OUT\_READ\_RES}$			±0.15		% FS
Output Voltage Read Back Total Error (Note 16)	$V_{OUT\_READ\_ERR}$	PMBus read	**-2**		**+2**	% FS
Output Ripple Voltage	V_{OUT_RIPPLE}	$V_{OUT} = 1V$, $C_{OUT} = 6$ x 470µF POSCAP + 12 x 100µF CERAMIC		8		mV

Electrical Specifications $V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
Output Current Read Back Resolution	$I_{OUT\_READ\_RES}$			0.087		A
Output Current Range (Note 15)	I_{OUT_RANGE}				**80**	A
Output Current Read Back Total Error	$I_{OUT\_READ\_ERR}$	PMBus read at max load. V_{OUT} = 1V		±3		A
SOFT-START AND SEQUENCING						
Delay Time from Enable to V_{OUT} Rise	t_{ON_DELAY}	Configured using PMBus	**2**		**5000**	ms
t_{ON_DELAY} Accuracy	$t_{ON\_DELAY\_ACCY}$			±2		ms
Output Voltage Ramp-Up Time	t_{ON_RISE}	Configured using PMBus. Single module standalone	**0.5**		**100**	ms
Output Voltage Ramp-Up Time Accuracy	$t_{ON\_RISE\_ACCY}$	Single module standalone		±250		µs
Delay Time from Disable to V_{OUT} Fall	t_{OFF_DELAY}	Configured using PMBus	**2**		**5000**	ms
t_{OFF_DELAY} Accuracy	$t_{OFF\_DELAY\_ACCY}$			±2		ms
Output Voltage Fall Time	t_{OFF_FALL}	Configured using PMBus. Single module standalone	**0.5**		**100**	ms
Output Voltage Fall Time Accuracy	$t_{ON\_FALL\_ACCY}$	Single module standalone		±250		µs
POWER-GOOD						
Power-Good Delay	V_{PG_DELAY}	Configured using PMBus	**0**		**5000**	ms
TEMPERATURE SENSE						
Temperature Sense Range	T_{SENSE_RANGE}	Configurable using PMBus	**-50**		**150**	°C
Internal Temperature Sensor Accuracy	INT_TEMP_{ACCY}	Tested at +100°C	-5		+5	°C
FAULT PROTECTION						
V_{DD} Undervoltage Threshold Range	$V_{DD\_UVLO\_RANGE}$	Measured internally	**4.18**		**16**	V
V_{DD} Undervoltage Threshold Accuracy (Note 16)	$V_{DD\_UVLO\_ACCY}$			±2		%FS
V_{DD} Undervoltage Response Time	$V_{DD\_UVLO\_DELAY}$			10		µs
V_{OUT} Overvoltage Threshold Range	$V_{OUT\_OV\_RANGE}$	Factory default		$1.15V_{OUT}$		V
		Configured using PMBus	**$1.05V_{OUT}$**		**V_{OUT_MAX}**	V
V_{OUT} Undervoltage Threshold Range	$V_{OUT\_UV\_RANGE}$	Factory default		$0.85V_{OUT}$		V
		Configured using PMBus	**0**		**$0.95V_{OUT}$**	V
V_{OUT} OV/UV Threshold Accuracy (Note 14)	V_{OUT_OV/UV_ACCY}		**-2**		**+2**	%
V_{OUT} OV/UV Response Time	V_{OUT_OV/UV_DELAY}			10		µs
Output Current Limit Set-Point Accuracy (Note 16)	I_{LIMIT_ACCY}	Tested at I_{OUT}_OC_FAULT_LIMIT = 80A		±10		% FS
Output Current Fault Response Time	I_{LIMIT_DELAY}	Factory default		3		t_{SW} (Note 17)
Over-temperature Protection Threshold (Controller Junction Temperature)	$T_{JUNCTION}$	Factory default		125		°C
		Configured using PMBus	**-40**		**125**	°C
Thermal Protection Hysteresis	$T_{JUNCTION\_HYS}$			15		°C

Electrical Specifications $V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
OSCILLATOR AND SWITCHING CHARACTERISTICS						
Switching Frequency Range	f_{SW_RANGE}		**296**		**1067**	kHz
Switching Frequency Set-Point Accuracy	f_{SW_ACCY}		**-5**		**+5**	%
Minimum Pulse Width Required from External SYNC Clock	EXT_SYNC_{PW}	Measured at 50% Amplitude	**150**			ns
Drift Tolerance for External SYNC Clock	EXT_SYNC_{DRIFT}	External SYNC Clock equal to 500kHz is not supported	**-10**		**+10**	%
LOGIC INPUT/OUTPUT CHARACTERISTICS						
Bias Current at the Logic Input Pins	I_{LOGIC_BIAS}	DDC, EN, MGN, PG, SA, SCL, SDA, SALRT, SYNC, UVLO, V_{MON}, V_{SET}	**-100**		**+100**	nA
Logic Input Low Threshold Voltage	$V_{LOGIC\_IN\_LOW}$				**0.8**	V
Logic Input High Threshold Voltage	$V_{LOGIC\_IN\_HIGH}$		**2.0**			V
Logic Output Low Threshold Voltage	$V_{LOGIC\_OUT\_LOW}$	2mA sinking			**0.5**	V
Logic Output High Threshold Voltage	$V_{LOGIC\_OUT\_HIGH}$	2mA sourcing	**2.25**			V
PMBus INTERFACE TIMING CHARACTERISTIC						
PMBus Operating Frequency	f_{SMB}		**100**		**400**	kHz

NOTES:

13. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design. Controller is independently tested before module assembly.
14. V_{OUT} measured at the termination of the VSENP and VSENN sense points.
15. The MAX load current is determined by the thermal "Derating Curves" on page 15,
16. "FS" stands for full scale of recommended maximum operation range.
17. "t_{SW}" stands for time period of operation switching frequency.

Typical Performance Curves

Efficiency Performance

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 6 x 470µF POSCAP + 12 x 100µF CERAMIC. Typical values are used unless otherwise noted.

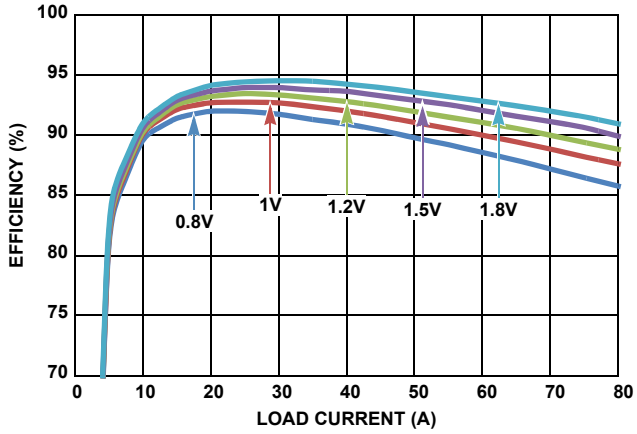


FIGURE 6. EFFICIENCY vs OUTPUT CURRENT AT V_{IN} = 5V, f_{SW} = 300kHz FOR VARIOUS OUTPUT VOLTAGES

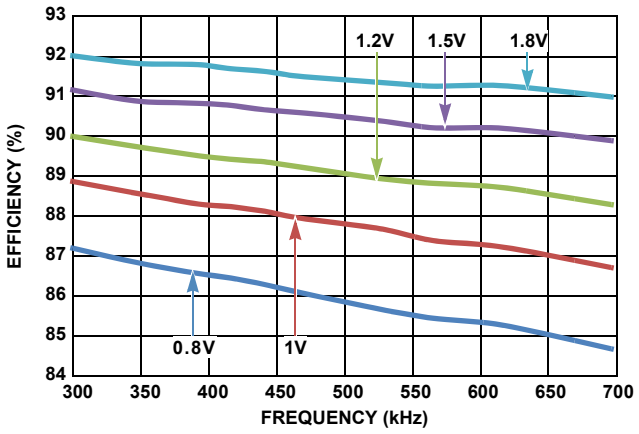


FIGURE 7. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 5V, I_{OUT} = 70A FOR VARIOUS OUTPUT VOLTAGES

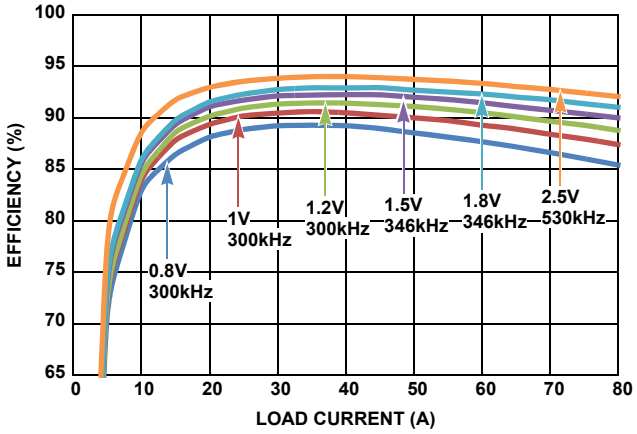


FIGURE 8. EFFICIENCY vs OUTPUT CURRENT AT V_{IN} = 9V, FOR VARIOUS OUTPUT VOLTAGES

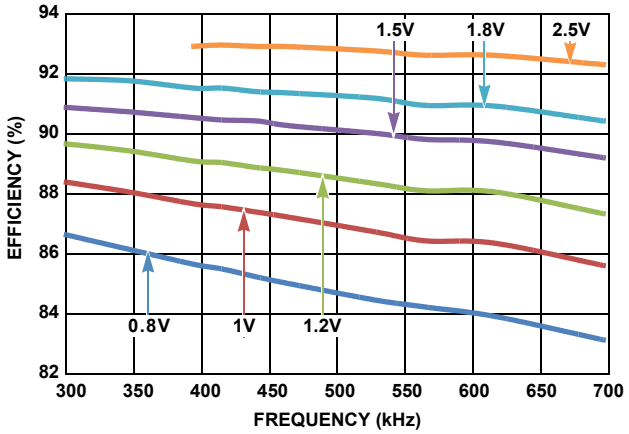


FIGURE 9. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 9V, I_{OUT} = 70A FOR VARIOUS OUTPUT VOLTAGES

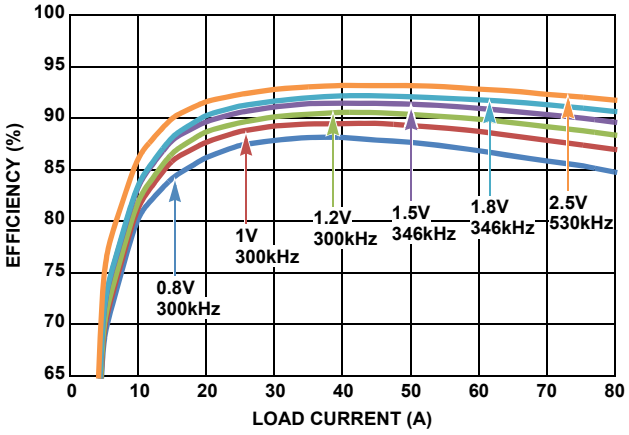


FIGURE 10. EFFICIENCY vs OUTPUT CURRENT AT V_{IN} = 12V, FOR VARIOUS OUTPUT VOLTAGES

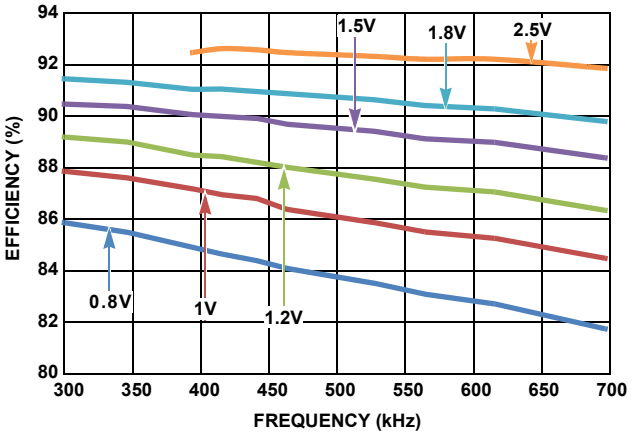


FIGURE 11. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 12V, I_{OUT} = 70A FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves (Continued)

Transient Response Performance

Operating conditions: I_{OUT} = 0A/40A, I_{OUT} slew rate > 100A/µs, T_A = +25°C, 0LFM. Typical values are used unless otherwise noted.

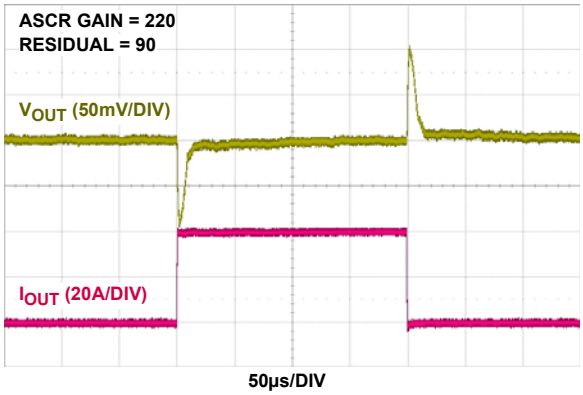


FIGURE 12. $5V_{IN}$ TO $1V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 571kHz, C_{OUT} = 8x100µF CERAMIC + 4x470µF POSCAP

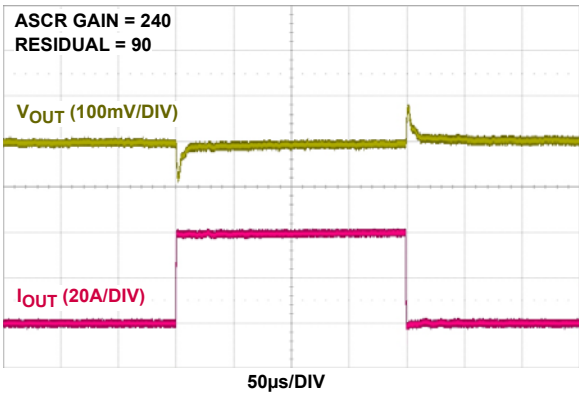


FIGURE 13. $5V_{IN}$ TO $1.5V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 571kHz, C_{OUT} = 10x100µF CERAMIC + 4x470µF POSCAP

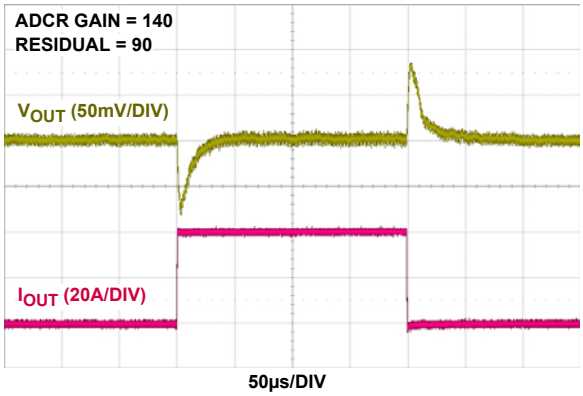


FIGURE 14. $12V_{IN}$ TO $1V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 300kHz, C_{OUT} = 14x100µF CERAMIC + 6x470µF POSCAP

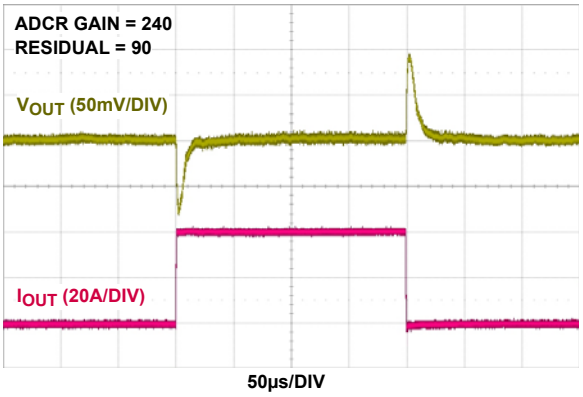


FIGURE 15. $12V_{IN}$ TO $1V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 571kHz, C_{OUT} = 10x100µF CERAMIC + 4x470µF POSCAP

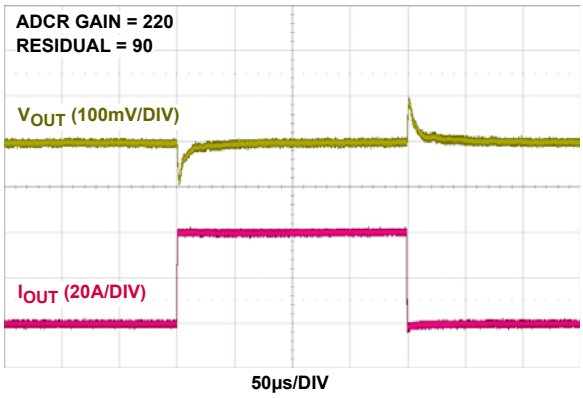


FIGURE 16. $12V_{IN}$ TO $1.5V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 571kHz, C_{OUT} = 10x100µF CERAMIC + 4x470µF POSCAP

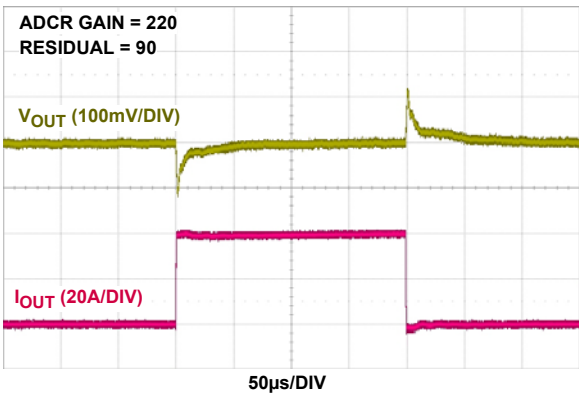


FIGURE 17. $12V_{IN}$ TO $2.5V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 800kHz, C_{OUT} = 6x100µF CERAMIC + 3x470µF POSCAP

Typical Performance Curves (Continued)

Derating Curves

All of the following curves were plotted at T_J = +120°C.

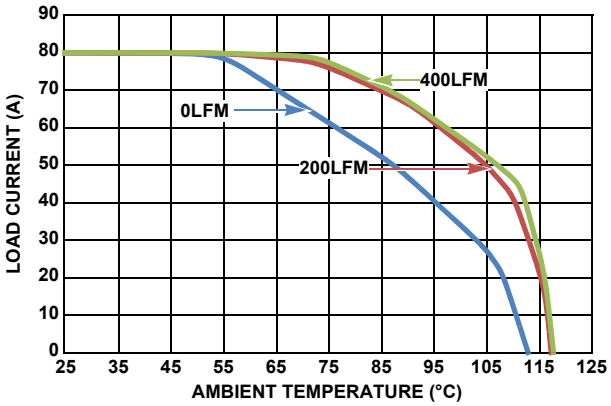


FIGURE 18. $5V_{IN}$ TO $1V_{OUT}$, f_{SW} = 300kHz

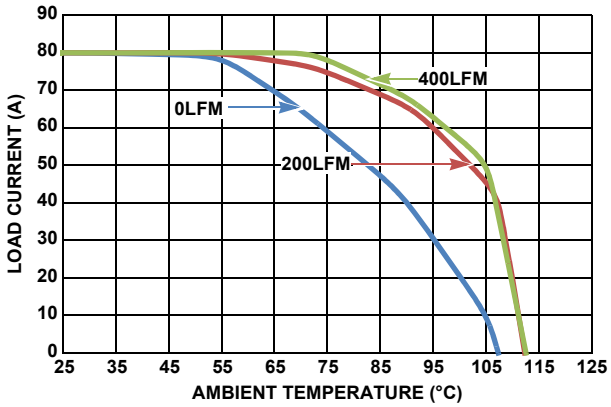


FIGURE 19. $12V_{IN}$ TO $1V_{OUT}$, f_{SW} = 300kHz

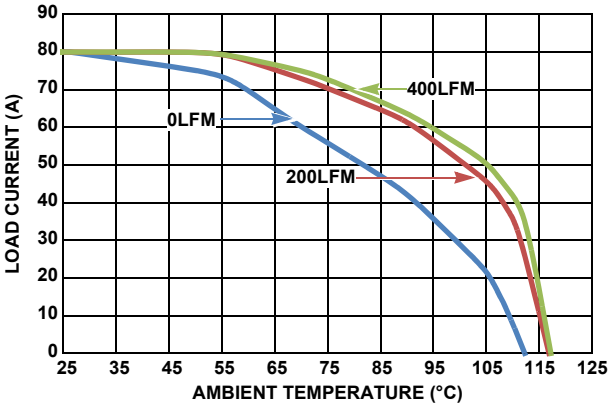


FIGURE 20. $5V_{IN}$ TO $1.5V_{OUT}$, f_{SW} = 300kHz

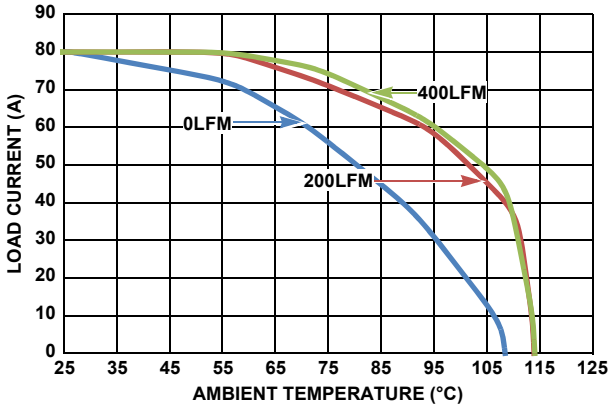


FIGURE 21. $12V_{IN}$ TO $1.5V_{OUT}$, f_{SW} = 364kHz

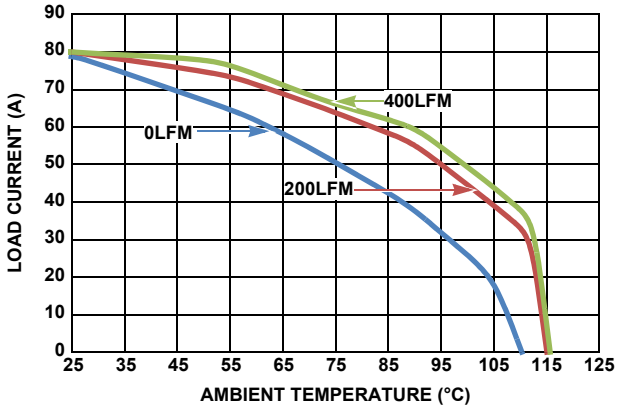


FIGURE 22. $5V_{IN}$ TO $2.5V_{OUT}$, f_{SW} = 364kHz

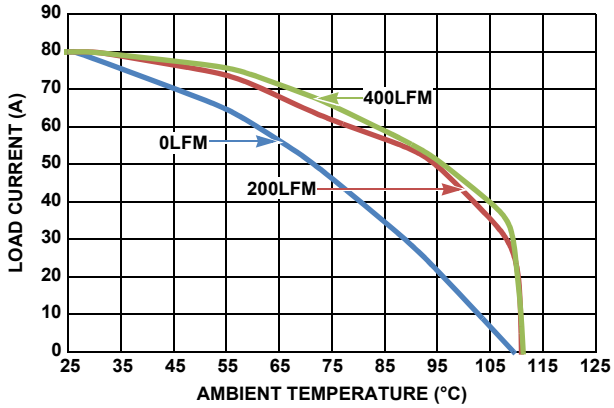


FIGURE 23. $12V_{IN}$ TO $2.5V_{OUT}$, f_{SW} = 533kHz

Functional Description

SMBus Communications

The ISL8273M provides a PMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ISL8273M can be used with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The ISL8273M accepts most standard PMBus commands. When configuring the device using PMBus commands, it is recommended that the enable pin is tied to SGND.

The SMBus device address is the only parameter that must be set by the external pins. All other device parameters can be set using PMBus commands.

The ISL8273M can operate without the PMBus in pin-strap mode with configurations programmed by pin-strap resistors, such as output voltage, switching frequency, device SMBus address, input UVLO, soft-start/stop, and current sharing. Note: pin-strap resistors with 1% tolerance or better should be used for all the pin-strap settings.

Output Voltage Selection

The output voltage can be set to a voltage between 0.6V and 2.5V if the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET pin is used to set the output voltage to levels as shown in Table 3. The R_{SET} resistor is placed between the VSET pin and SGND. A standard 1% resistor is required.

TABLE 3. OUTPUT VOLTAGE RESISTOR SETTINGS

V_{OUT} (V)	R_{SET} (kΩ)
0.60	10
0.65	11
0.70	12.1
0.72	121 (available with FC04 firmware only)
0.75	13.3
0.80	14.7
0.85	16.2
0.88	133 (available with FC04 firmware only)
0.90	17.8
0.92	147 (available with FC04 firmware only)
0.95	19.6
1.00	21.5, or connect to SGND
1.05	23.7
1.10	26.1
1.15	28.7

TABLE 3. OUTPUT VOLTAGE RESISTOR SETTINGS (Continued)

V_{OUT} (V)	R_{SET} (kΩ)
1.20	31.6, or Open
1.25	34.8
1.30	38.3
1.40	42.2
1.50	46.4
1.60	51.1
1.70	56.2
1.80	61.9
1.90	68.1
2.00	75
2.10	82.5
2.20	90.9
2.30	100
2.50	110, or connect to V25

The output voltage can also be set to any value between 0.6V and 2.5V using the PMBus command VOUT_COMMAND. This device supports dynamic voltage scaling, by allowing change to the output voltage set point during regulation. The voltage transition rate is specified by the PMBus command VOUT_TRANSITION_RATE.

By default, V_{OUT_MAX} is set to 110% of V_{OUT} set by the pin-strap resistor, which can be changed to any value up to 2.75V by the PMBus command VOUT_MAX.

Soft-Start, Stop Delay, and Ramp Times

The ISL8273M follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. When this process is completed, the device is ready to accept commands from the PMBus interface and the module is ready to be enabled. If the module is to be synchronized to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ISL8273M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp-up time can be programmed to custom values using the PMBus commands TON_DELAY and TON_RISE. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set

to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 1ms to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay and ramp down time for soft-stop/off can be programmed using the PMBus commands TOFF_DELAY and TOFF_FALL. In addition, the module can be configured as “immediate off” using the command ON_OFF_CONFIG, such that the internal MOSFETs are turned off immediately after the delay time expires.

In current sharing mode, in which multiple ISL8273M modules are connected in parallel, ASCR is required to be disabled for the ramp-up with the USER_CONFIG command. Therefore, the soft-start rise time is not equal to TON_RISE. It can be calculated approximately by Equation 1.

$$\text{Rise Time (ms)} \approx \frac{\text{TON\_RISE}}{V_{IN} \times f_{SW}} \times 330\text{kHz} \times 12\text{V} \quad \text{(EQ. 1)}$$

Also in current sharing mode, ASCR will be enabled automatically upon power-good assertion after the ramp completes. To avoid premature ASCR turn on, it is recommended to increase POWER_GOOD_DELAY if the rise time exceeds 10ms. In addition, only “immediate off” is supported for current sharing.

In current sharing mode, if module self enable is used (VIN power-up), a minimum TON_DELAY of 15ms is recommended.

The SS/UVLO pin can be used to program the soft-start/stop delay time and ramp time to some typical values as shown in Table 4.

TABLE 4. SOFT-START/STOP RESISTOR SETTINGS

DELAY TIME (ms)	RAMP TIME (ms)	R_{SET} (kΩ)
5	2	19.6, or connect to SGND
10	2	21.5
5	5	23.7, or Open
10	5	26.1
20	5	28.7
5	10	31.6
10	10	34.8, or connect to V25
20	10	38.3
5	2	42.2
10	2	46.4
5	5	51.1
10	5	56.2
20	5	61.9
5	10	68.1
10	10	75
20	10	82.5

Power-Good

The ISL8273M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. This limit can be changed using the PMBus command POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the ISL8273M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A PG delay can be programmed using the PMBus command POWER_GOOD_DELAY.

Switching Frequency and PLL

The device’s switching frequency is set from 296kHz to 1067kHz using the pin-strap method (for stand-alone noncurrent sharing module only) as shown in Table 5, or by using the PMBus command FREQUENCY_SWITCH. The ISL8273M incorporates an internal Phase-locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. It is recommended that when using an external clock, the same frequency should be set in the FREQUENCY_SWITCH command. If the external clock is lost, the module will automatically switch to the internal clock. When using the internal oscillator, the SYNC pin can be configured as a clock source and as external sync to other modules. Refer to the SYNC_CONFIG command on page 49 for more information.

TABLE 5. SWITCHING FREQUENCY RESISTOR SETTINGS

f_{SW} (kHz)	R_{SET} (kΩ)
296	14.7, or connect to SGND
320	16.2
364	17.8
400	19.6
421	21.5, or Open
471	23.7
533	26.1
571	28.7
615	31.6, or connect to V25
727	34.8
800	38.3
842	42.2
889	46.4
1067	51.1

Loop Compensation

The module loop response is programmable using the PMBus command ASCR_CONFIG or by using the pin-strap method (ASCR pin) according to Table 6. The ISL8273M uses the ChargeMode control algorithm that responds to the output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

TABLE 6. ASCR RESISTOR SETTINGS

ASCR GAIN	ASCR RESIDUAL	R_{SET} (kΩ)
80	90	10
120	90	11, or connect to SGND
160	90	12.1
200	90	13.3, or Open
240	90	14.7
280	90	16.2
320	90	17.8
360	90	19.6
400	90	21.5
450	90	23.7
500	90	26.1
550	90	28.7
600	90	31.6
700	90	34.8
800	90	38.3
80	100	42.2
120	100	46.4
160	100	51.1
200	100	56.2
240	100	61.9
280	100	68.1
320	100	75
360	100	82.5
400	100	90.9
450	100	100
500	100	110, or connect to V25
550	100	121
600	100	133
700	100	147
800	100	162

Input Undervoltage Lockout (UVLO)

The input Undervoltage Lockout (UVLO) prevents the ISL8273M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.18V and 16V by using the PMBus command VIN_UV_FAULT_LIMIT. Using the pin-strap method (SS/UVLO pin) as shown in Table 7 allows to set the V_{UVLO} to two typical values.

A fault response to an input undervoltage fault can be programmed by the PMBus command VIN_UV_FAULT_RESPONSE. If the input undervoltage fault retry is enabled, the module will shut down immediately when the input voltage falls below V_{UVLO} and then continuously checks the input voltage after a retry delay time, which can be configured from 35ms to 280ms. If the input voltage rises above the input undervoltage warning level, the module will restart. The input undervoltage warning is $1.05*V_{UVLO}$ by default and can be programmed by the PMBus command VIN_UV_WARN_LIMIT. Note that fault retry is not supported in current sharing configuration.

TABLE 7. UVLO RESISTOR SETTINGS

UVLO (V)	R_{SET} (kΩ)
4.5	Open
4.5	Connect to V25
4.5	Connect to SGND
4.5	19.6, 21.5, 23.7, 26.1, 28.7, 31.6, 34.8, 38.3
10.8	42.2, 46.4, 51.1, 56.2, 61.9, 68.1, 75, 82.5

SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between pins SA and SGND. Table 8 lists the available module addresses.

TABLE 8. SMBus ADDRESS RESISTOR SELECTION

R_{SA} (kΩ)	SMBus ADDRESS
10	19h
11	1Ah
12.1	1Bh
13.3	1Ch
14.7	1Dh
16.2	1Eh
17.8	1Fh
19.6	20h
21.5	21h
23.7	22h
26.1	23h
28.7	24h
31.6	25h
34.8, or connect to SGND	26h
38.3	27h
42.2, or Open	28h
46.4	29h
51.1	2Ah

TABLE 8. SMBus ADDRESS RESISTOR SELECTION (Continued)

R_{SA} (kΩ)	SMBus ADDRESS
56.2	2Bh
61.9	2Ch
68.1	2Dh
75	2Eh
82.5	2Fh
90.9	30h
100	31h
110	32h
121	33h
133	34h
147	35h
162	36h
178	37h

Output Overvoltage Protection

The ISL8273M offers an internal output overvoltage protection circuit that can protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at pins VSENP, VSENN) to a threshold set to 15% higher than the target output voltage (default setting). The fault threshold can be programmed to a desired level by the PMBus command VOUT_OV_FAULT_LIMIT. If the VSENP - VSENN voltage exceeds this threshold, the module will initiate an immediate shutdown without retry. Continuous retry can be enabled using the PMBus command VOUT_OV_FAULT_RESPONSE. The retry delay time can be configured from 35ms to 280ms. Note that fault retry is not supported in current sharing configuration.

Internal to the module, two 100Ω resistors are populated from V_{OUT} to VSENP and SGND to VSENN to protect the module from overvoltage conditions in case of open at the voltage sensing pins and differential remote sense traces due to assembly error. As long as differential remote sense traces have low resistance, V_{OUT} regulation accuracy is not compromised.

Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ISL8273M provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage. However, the total time elapsed from when the delay period expires to when the output reaches its target value will match the preconfigured ramp time (see Figure 24).

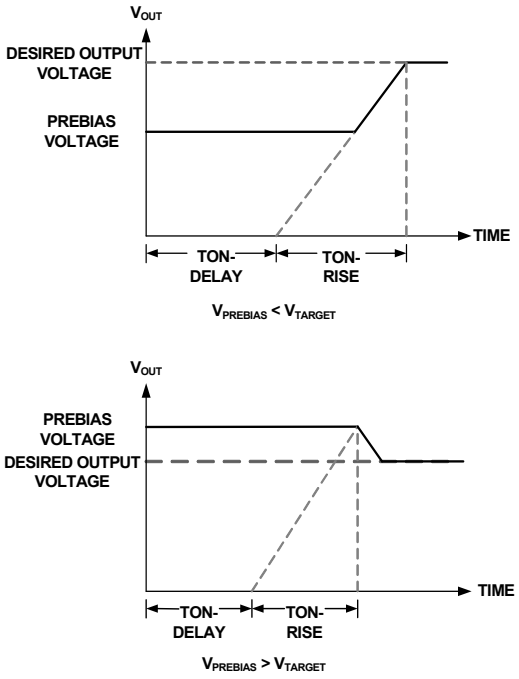


FIGURE 24. OUTPUT RESPONSES TO PREBIAS VOLTAGES

If a prebias voltage is higher than the target voltage after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage. Thus, both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

When the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition. The device then responds based on the output overvoltage fault response setting programmed by the PMBus command VOUT_OV_FAULT_RESPONSE.

Output Overcurrent Protection

The ISL8273M is protected from damage if the output is shorted to ground or if an overload condition is imposed on the output. The average output overcurrent fault threshold can be programmed by the PMBus command IOUT_OC_FAULT_LIMIT. The module automatically programs the peak inductor current fault threshold by calculating inductor ripple current based on input voltage, switching frequency, and VOUT_COMMAND. When the peak inductor current crosses the peak inductor current fault threshold for three successive switching cycles, the module will initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown without retry. A continuous retry can be enabled using the PMBus command MFR_IOUT_OC_FAULT_RESPONSE. Note that fault retry is not supported in the current sharing configuration.

Thermal Overload Protection

The ISL8273M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The factory default temperature limit is set to +125°C. The temperature limit can be changed using the PMBus command OT_FAULT_LIMIT.

The default response from an over-temperature fault is an immediate shutdown without retry. Retry settings can be programmed using the PMBus command OT_FAULT_RESPONSE. Hysteresis is implemented with the over-temperature fault retry. If a retry is enabled, the module will shut down immediately upon an over-temperature fault event and then continuously checks the temperature after a retry delay time, which can be configured from 35ms to 280ms. If the temperature falls below the over-temperature warning level, the module will restart. The over-temperature warning is +105°C by default and programmable using the PMBus command OT_WARN_LIMIT. Note that fault retry is not supported in the current sharing configuration.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil's digital power modules and digital controllers. The DDC bus provides the communication channel between devices for features such as current sharing, sequencing, and fault spreading. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus to guarantee the rise time as shown in Equation 2:

$$\text{Rise Time} = R_{PU} * C_{LOAD} < 1\mu s \quad \text{(EQ. 2)}$$

Where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor can be tied to an external 3.3V or 5V supply as long as this voltage is present before or during the device power-up. In principle, each device connected to the DDC bus represents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance.

Active Current Sharing

Multiple ISL8273M modules can be used in parallel to increase the output current capability of a single power rail. By connecting the DDC and SYNC pins of each module together and configuring the modules as a current sharing rail, the units will share the current equally within a few percent.

Figure 25 illustrates a typical connection for two modules.

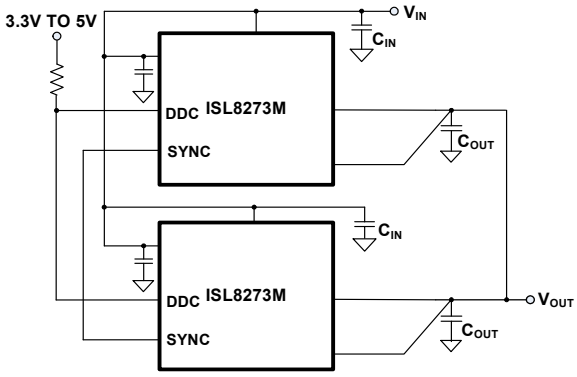


FIGURE 25. CURRENT SHARING GROUP

The ISL8273M uses a DDC bus based digital current sharing technique to balance the steady-state module output current by aligning the load lines of member modules to a reference module.

When multiple ISL8273M modules are connected for current sharing, a non-zero active droop resistance must be set to add artificial resistance in the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to the power train components and PCB layout. The active droop resistance can be programmed using the PMBus command VOUT_DROOP based on Equation 3. Typically, a higher droop value offers a more accurate dynamic current sharing at the expense of the output load regulation. 1% droop at full load will be a good trade-off between output load regulation and dynamic current sharing.

$$\frac{V_{OUT}}{I_{LOAD(MAX)}} \times 0.005 \leq \text{Droop} \leq \frac{V_{OUT}}{I_{LOAD(MAX)}} \times 0.015 \quad \text{(EQ. 3)}$$

At system start-up, the module with the lowest device position as selected in the DDC_CONFIG is defined as the reference module. The remaining modules are members. The reference module broadcasts its current over the DDC bus. The members use the reference current information to trim their voltages (V_{MEMBER}) to balance the current loading of each module in the system.

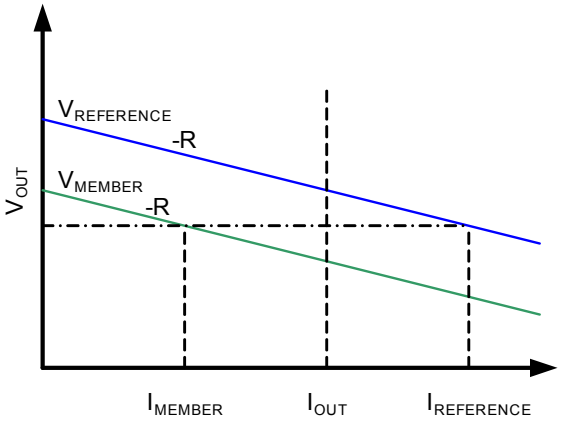


FIGURE 26. ACTIVE CURRENT SHARING

Figure 26 shows that for load lines with identical slopes, the member voltage is increased towards the reference voltage, which closes the gap between the inductor currents.

The relation between reference and member currents and voltage is given by Equation 4:

$$V_{MEMBER} = V_{OUT} + R \times (I_{REFERENCE} - I_{MEMBER}) \quad \text{(EQ. 4)}$$

where *R* is the value of the droop resistance.

The DDC_CONFIG command configures the module for active current sharing. The default setting is a stand-alone noncurrent sharing module.

For the fault configuration, it is required to enable the fault spreading mode in the current sharing rail with the PMBus command DDC_GROUP. Broadcast operation must be enabled using the DDC_GROUP command to allow start-up/shutdown and margining operations. It is optional to enable the V_{OUT} broadcast in the DDC_GROUP command to allow V_{OUT} set point to change dynamically during operation.

In multiple-module current sharing configuration, it is required to synchronize all modules to the same switching clock by tying the SYNC pins together. The clock source can be selected either from one module or from an external clock using the SYNC_CONFIG command. The phase offset of current sharing modules is automatically set according to the device positions and number of devices specified in the DDC_CONFIG command.

The pin-strap method is offered for the current sharing configuration with the CS pin. Table 9 lists the current sharing pin-strap settings.

TABLE 9. CURRENT SHARING RESISTOR SETTINGS

CLOCK CONFIGURATION	DEVICE POSITION NUMBER OF DEVICES	DROOP (mV/A)	R_{SET} (kΩ)
Output internal	1-2	0.07	10
External	2-2	0.07	11
Output internal	1-2	0.1	12.1
External	2-2	0.1	13.3
Output internal	1-2	0.13	14.7
External	2-2	0.13	16.2
Output internal	1-2	0.17	17.8
External	2-2	0.17	19.6
Output internal	1-2	0.21	21.5
External	2-2	0.21	23.7
Output internal	1-3	0.05	26.1
External	2-3	0.05	28.7
External	3-3	0.05	31.6
Output internal	1-3	0.07	34.8
External	2-3	0.07	38.3
External	3-3	0.07	42.2
Output internal	1-3	0.09	46.4
External	2-3	0.09	51.1
External	3-3	0.09	56.2
Output internal	1-3	0.11	61.9
External	2-3	0.11	68.1
External	3-3	0.11	75
Output internal	1-3	0.14	82.5
External	2-3	0.14	90.9
External	3-3	0.14	100
Output internal	1-4	0.07	110 (available with FC03 and FC04 firmware only)
External	2-4	0.07	121 (available with FC03 and FC04 firmware only)
External	3-4	0.07	133 (available with FC03 and FC04 firmware only)
External	4-4	0.07	147 (available with FC03 and FC04 firmware only)
Internal only	1-1	0	Connect to SGND (for immediate off)
Internal only	1-1	0	OPEN (for soft-off)

NOTE: Fault retry is not supported in the current sharing configuration.

Phase Spreading

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device, so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset of each device can also be set to any value between 0° and 360° in 22.5° increments with the PMBus command INTERLEAVE. By default, the internal two phases of the module maintain a phase difference of 180°.

Fault Spreading

Digital-DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group using the PMBus command DDC_GROUP. When a nondestructive fault occurs, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shut down simultaneously if configured to do so.

Note that fault retry is not supported in multiple modules with fault spreading enabled, such as current sharing configuration.

Output Sequencing

A group of Digital-DC modules or devices can be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors (FPGAs and ASICs)

that require one supply to reach its operating voltage before another supply reaching it to avoid latch-up. Multidevice sequencing can be achieved by configuring each device with the PMBus command SEQUENCE. Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that follows the sequence.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. The enable must be driven low to initiate a sequenced turnoff of the group. It is recommended to enable fault spreading with the PMBus command DDC_GROUP within a sequencing group.

Monitoring with SMBus

The ISL8273M can monitor a wide variety of different system parameters using the PMBus commands:

- READ_VIN
- READ_VOUT
- READ_IOUT
- READ_INTERNAL_TEMP
- READ_DUTY_CYCLE
- READ_FREQEUNCY
- READ_VMON

Snapshot Parameter Capture

The ISL8273M offers a special feature to capture parametric data and fault status following a fault. Detailed description is provided in the "PMBus Commands Description" on page 28 under PMBus command SNAPSHOT and SNAPSHOT_CONTROL.

Nonvolatile Memory

The ISL8273M stores user configurations in the internal nonvolatile memory. Integrated security measures ensure that the user can only restore the module to a level that has been made available to them. During the initialization process, the ISL8273M checks for stored values contained in its internal nonvolatile memory.

Modules are shipped with factory defaults configuration and most settings can be overwritten by PMBus Commands and can be stored in nonvolatile memory by the PMBus command STORE_USER_ALL.

Layout Guide

To achieve stable operation, low losses and good thermal performance some layout considerations are necessary. See Figure 27 for the recommended layout.

- Establish separate SGND and PGND planes, then connect SGND to PGND on a middle layer and underneath PAD6 with a single point connection. For SGND and PGND pin connections, such as small pins H16, J16, M5, and M17..., use multiple vias for each pin to connect to the inner SGND or PGND layer.
- To minimize high frequency noise, place enough ceramic capacitors between VIN and PGND and VOUT and PGND. Place bypass capacitors between VDD, VDRV, and the ground plane, as close to the module as possible. It is critical to place the output ceramic capacitors close to the VOUT pads and in the direction of the load current path to create a low impedance path for the high frequency inductor ripple current.
- Use large copper areas for the power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. It is recommended to enlarge PAD11 and 15 and place more vias on them. The ceramic capacitors CIN can be placed on the bottom layer under these two pads.
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation and place the two traces in parallel. Route a trace from VSENN and VSENP to the point of load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENN, VSENP sensing lines near the SW pins.
- PAD14 and 16 (SW1 and SW2) are noisy pads, but they are beneficial for thermal dissipation. If the noise issue is critical for the application, it is recommended to use only the top layer for the SW pads. For better thermal performance, use multiple vias on these pads to connect into the SW inner and bottom layers. However, caution must be taken when placing a limited area of SW planes in any layer. The SW planes should avoid the sensing signals and should be surrounded by the PGND layer to avoid the noise coupling.
- For pins SWD1 (L3) and SWD2 (P10), it is recommended to connect to the related SW1 and SW2 pads with short loop wires. The wire width should be more than 20mils.

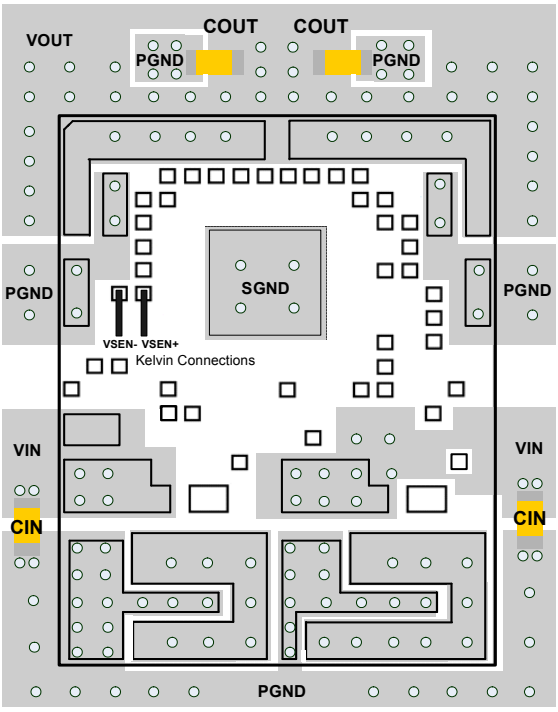


FIGURE 27. RECOMMENDED LAYOUT

Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +120°C. The derating curves are derived based on tests of the ISL8273MEVAL1Z evaluation board, which is an 8-layer board 4.7x4.8inch in size with 2oz Cu on all layers and multiple via interconnects. In the actual application, other heat sources and design margins should be considered.

Package Description

The structure of the ISL8273M belongs to the High Density Array no-lead package (HDA). This kind of package has advantages such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8273M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8273M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly is overmolded with a polymer mold compound to protect these devices.

The package outline and typical Printed Circuit Board (PCB) layout pattern design and typical stencil pattern design are shown on pages 55, 56, and 57. The module has a small size of 18mmx23mmx7.5mm.

PCB Layout Pattern Design

The bottom of the ISL8273M is a leadframe footprint, which is attached to the PCB by a surface mounting process. The PCB layout pattern is shown on page 57 through 59. The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 oz. of copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as the number of vias is increased. Use as many vias as practical for the thermal land size and your board design rules will allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. Stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the "Package Outline Drawing" section starting on page 53. A typical solder stencil pattern is shown starting on page 55. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick like paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch HDA.

Reflow Parameters

Due to the low mount height of the HDA, "No-Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. A nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 28 is provided as a guideline, which can be customized for varying manufacturing practices and applications.

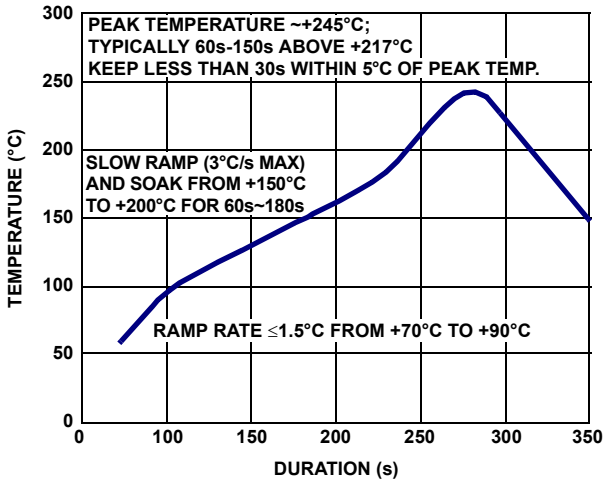


FIGURE 28. TYPICAL REFLOW PROFILE

PMBus Command Summary

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
01h	OPERATION	Sets Enable, Disable, and V_{OUT} Margin modes.	R/W BYTE	BIT			28
02h	ON_OFF_CONFIG	Configures the EN pin and PMBus commands to turn the unit ON/OFF	R/W BYTE	BIT	16h	Hardware Enable, Soft Off	28
03h	CLEAR_FAULTS	Clears fault indications.	SEND BYTE				29
15h	STORE_USER_ALL	Stores all PMBus values written since last restore at user level.	SEND BYTE				29
16h	RESTORE_USER_ALL	Restores PMBus settings that were stored using STORE_USER_ALL.	SEND BYTE				29
20h	VOUT_MODE	Preset to defined data format of V_{OUT} commands.	READ BYTE	BIT	13h	Linear Mode, Exponent = -13	29
21h	VOUT_COMMAND	Sets the nominal value of the output voltage.	R/W WORD	L16u		Pin-strap	29
23h	VOUT_CAL_OFFSET	Applies a fixed offset voltage to the VOUT_COMMAND.	R/W WORD	L16s	0000h	0V	30
24h	VOUT_MAX	Sets the maximum possible value of V_{OUT}. 110% of pin-strap V_{OUT}.	R/W WORD	L16u		1.1*V_{OUT} Pin-strap	30
25h	VOUT_MARGIN_HIGH	Sets the value of the V_{OUT} during a margin high.	R/W WORD	L16u		1.05*V_{OUT} Pin-strap	30
26h	VOUT_MARGIN_LOW	Sets the value of the V_{OUT} during a margin low.	R/W WORD	L16u		0.95*V_{OUT} Pin-strap	30
27h	VOUT_TRANSITION_RATE	Sets the transition rate during margin or other change of V_{OUT}.	R/W WORD	L11	BA00h	1V/ms	30
28h	VOUT_DROOP	Sets the loadline (V/I Slope) resistance for the rail.	R/W WORD	L11		Pin-strap	31
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W WORD	L11		Pin-strap	31
37h	INTERLEAVE	Configures a phase offset between devices sharing a SYNC clock.	R/W WORD	BIT	0000h		31
38h	IOUT_CAL_GAIN	Sense resistance for inductor DCR current sensing.	R/W WORD	L11	B370h	0.86mΩ	31
39h	IOUT_CAL_OFFSET	Sets the current-sense offset.	R/W WORD	L11	0000h	0A	31
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W WORD	L16u		1.15*V_{OUT} Pin-strap	32
41h	VOUT_OV_FAULT_RESPONSE	Configures the V_{OUT} overvoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	32
42h	VOUT_OV_WARN_LIMIT	Sets the V_{OUT} overvoltage warn threshold.	R/W WORD	L16u		1.10*V_{OUT} Pin-strap	32
43h	VOUT_UV_WARN_LIMIT	Sets the V_{OUT} undervoltage warn threshold.	R/W WORD	L16u		0.9*V_{OUT} Pin-strap	32
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W WORD	L16u		0.85*V_{OUT} Pin-strap	32
45h	VOUT_UV_FAULT_RESPONSE	Configures the V_{OUT} undervoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	33
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold.	R/W WORD	L11	EAD0h	90A	33

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
4Ah	IOUT_OC_WARN_LIMIT	Sets the I_{OUT} average overcurrent warning threshold. Available only with FC03 and FC04 firmware	R/W WORD	L11		0.9 * IOUT_OC_FAULT_LIMIT	33
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold.	R/W WORD	L11	E4E0h	-50A	33
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W WORD	L11	EBE8h	+125°C	34
50h	OT_FAULT_RESPONSE	Configures the over-temperature fault response.	R/W BYTE	BIT	80h	Disable and No Retry	34
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit.	R/W WORD	L11	EB48h	+105°C	34
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit.	R/W WORD	L11	DC40h	-30°C	34
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W WORD	L11	E580h	-40°C	35
54h	UT_FAULT_RESPONSE	Configures the under-temperature fault response.	R/W BYTE	BIT	80h	Disable and No Retry	35
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W WORD	L11	D380h	14V	35
56h	VIN_OV_FAULT_RESPONSE	Configures the V_{IN} overvoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	36
57h	VIN_OV_WARN_LIMIT	Sets the input overvoltage warning limit.	R/W WORD	L11	D353h	13.3V	36
58h	VIN_UV_WARN_LIMIT	Sets the input undervoltage warning limit.	R/W WORD	L11		1.05*V_{IN} UV Fault Limit	36
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W WORD	L11		Pin-strap	36
5Ah	VIN_UV_FAULT_RESPONSE	Configures the V_{IN} undervoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	37
5Eh	POWER_GOOD_ON	Sets the voltage threshold for Power-good indication.	R/W WORD	L16u		0.9*V_{OUT} Pin-strap	37
60h	TON_DELAY	Sets the delay time from ENABLE to start of V_{OUT} rise.	R/W WORD	L11		Pin-strap	37
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W WORD	L11		Pin-strap	37
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall.	R/W WORD	L11		Pin-strap	38
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.	R/W WORD	L11		Pin-strap	38
78h	STATUS_BYTE	Returns an abbreviated status for fast reads.	READ BYTE	BIT	00h	No Faults	38
79h	STATUS_WORD	Returns information with a summary of the unit's fault condition.	READ WORD	BIT	0000h	No Faults	39
7Ah	STATUS_VOUT	Returns the V_{OUT} specific status.	READ BYTE	BIT	00h	No Faults	40
7Bh	STATUS_IOUT	Returns the I_{OUT} specific status.	READ BYTE	BIT	00h	No Faults	40
7Ch	STATUS_INPUT	Returns specific status specific to the input.	READ BYTE	BIT	00h	No Faults	40

PMBus Command Summary (Continued)

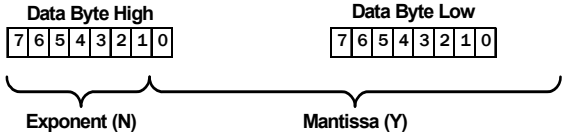
COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
7Dh	STATUS_TEMP	Returns the temperature specific status.	READ BYTE	BIT	00h	No Faults	41
7Eh	STATUS_CML	Returns the communication, logic and memory specific status.	READ BYTE	BIT	00h	No Faults	41
80h	STATUS_MFR_SPECIFIC	Returns the VMON and external sync clock specific status.	READ BYTE	BIT	00h	No Faults	41
88h	READ_VIN	Returns the input voltage reading.	READ WORD	L11			42
8Bh	READ_VOUT	Returns the output voltage reading.	READ WORD	L16u			42
8Ch	READ_IOUT	Returns the output current reading.	READ WORD	L11			42
8Dh	READ_INTERNAL_TEMP	Returns the temperature reading internal to the device.	READ WORD	L11			42
94h	READ_DUTY_CYCLE	Returns the duty cycle reading during the ENABLE state.	READ WORD	L11			42
95h	READ_FREQUENCY	Returns the measured operating switch frequency.	READ WORD	L11			42
96h	READ_IOUT_0	Returns phase 1 current reading.	READ WORD	L11			42
97h	READ_IOUT_1	Returns phase 2 current reading.	READ WORD	L11			43
99h	MFR_ID	Sets a user defined identification.	R/W BLOCK	ASC		Null	43
9Ah	MFR_MODEL	Sets a user defined model.	R/W BLOCK	ASC		Null	43
9Bh	MFR_REVISION	Sets a user defined revision.	R/W BLOCK	ASC		Null	43
9Ch	MFR_LOCATION	Sets a user defined location identifier.	R/W BLOCK	ASC		Null	43
9Dh	MFR_DATE	Sets a user defined date.	R/W BLOCK	ASC		Null	44
9Eh	MFR_SERIAL	Sets a user defined serialized identifier.	R/W BLOCK	ASC		Null	44
A8H	LEGACY_FAULT_GROUP	Sets rail IDs of legacy devices for fault spreading	R/W BLOCK	BIT	00000000h	No rail ID specified	44
B0h	USER_DATA_00	Sets a user defined data.	R/W BLOCK	ASC		Null	44
D0h	ISENSE_CONFIG	Configures ISENSE related features.	R/W BYTE	BIT	06h	256ns Blanking Time, High Range	45
D1h	USER_CONFIG	Configures several user-level features.	R/W BYTE	BIT		Pin-strap (ASCR on/off for start-up)	45
D3h	DDC_CONFIG	Configures the DDC bus.	R/W WORD	BIT		Pin-strap (set based on PMBus address and CS)	46
D4h	POWER_GOOD_DELAY	Sets the delay between V_{OUT} > PG threshold and asserting the PG pin.	R/W WORD	L11	C300h	3ms	46
DFh	ASCR_CONFIG	Configures ASCR control loop.	R/W BLOCK	CUS		Pin-strap	46
E0h	SEQUENCE	Identifies the Rail DDC ID to perform multi-rail sequencing.	R/W WORD	BIT	0000h	Prequel and Sequel Disabled	47
E2h	DDC_GROUP	Sets rail DDC IDs to obey faults and margining spreading information.	R/W BLOCK	BIT		Pin-strap (set based on CS)	47
E4h	DEVICE_ID	Returns the 16-byte (character) device identifier string.	READ BLOCK	ASC		Reads Device Version	48
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W BYTE	BIT	80h	Disable and No Retry	48

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W BYTE	BIT	80h	Disable and No Retry	48
E9h	SYNC_CONFIG	Configures the SYNC pin.	R/W BYTE	BIT		Pin-strap (set based on CS)	49
EAh	SNAPSHOT	Returns 32-byte read-back of parametric and status values.	READ BLOCK	BIT			49
EBh	BLANK_PARAMS	Returns recently changed parameter values.	READ BLOCK	BIT	FF...FFh		49
F3h	SNAPSHOT_CONTROL	Snapshot feature control command.	R/W BYTE	BIT			50
F4h	RESTORE_FACTORY	Restores device to the factory default values.	SEND BYTE				50
F5h	MFR_VMON_OV_FAULT_LIMIT	Returns the VMON overvoltage threshold.	READ WORD	L11	CB00h	6V	50
F6h	MFR_VMON_UV_FAULT_LIMIT	Returns the VMON undervoltage threshold.	READ WORD	L11	CA00h	4V	50
F7h	MFR_READ_VMON	Returns the VMON voltage reading.	READ WORD	L11			50
F8h	VMON_OV_FAULT_RESPONSE	Returns the VMON overvoltage response.	READ BYTE	BIT	80h	Disable and No Retry	51
F9h	VMON_UV_FAULT_RESPONSE	Returns the VMON undervoltage response.	READ BYTE	BIT	80h	Disable and No Retry	51

PMBus Data Formats

Linear-11 (L11)
The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X).



The relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)
The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Linear-16 Signed (L16s)
The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X).
The relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)
An explanation of the Bit Field for each command is provided in "PMBus Commands Description" on page 28.

Custom (CUS)
An explanation of the Custom data format for each command is provided in "PMBus Commands Description" on page 28. A combination of Bit Field and integer is a common type of Custom data format.

ASCII (ASC)
A variable length string of text characters using the ASCII data format.

PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and ASCCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_USER_ALL, and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Summary

All commands can be read at any time.

Always disable the device when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To ensure a change to a device setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable.

PMBus Commands Description

OPERATION (01h)

Definition: Sets the Enable, Disable, and V_{OUT} Margin settings. Data values of OPERATION that force margin high or low take effect only when the MGN pin is left open (that is, in the NOMINAL margin state).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value:

Units: N/A

SETTINGS	ACTIONS
04h	Immediate off (no sequencing)
44h	Soft off (with sequencing)
84h	On - Nominal
94h	On - Margin low
A4h	On - Margin high

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 16h (Device starts from ENABLE pin with soft-off)

Units: N/A

SETTINGS	ACTIONS
16h	Device starts from ENABLE pin with soft off.
17h	Device starts from ENABLE pin with immediate off.
1Ah	Device starts from OPERATION command with soft off.
1Bh	Device starts from OPERATION command with immediate off.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

Reference: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings. Fixed with linear mode with default exponent (N) = -13

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 13h (Linear Mode, N = -13)

Units: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than VOUT_MAX.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit.

Data Length in Bytes: 2

Data Format: L16s

Type: R/W

Default Value: 0000h

Units: Volts

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. Default value can be changed using PMBus.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10xVOUT_COMMAND pin-strap setting

Units: Volts

Range: 0V to 5.5V

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This command loads the unit with the voltage to which the output is to be changed when the OPERATION command or MGN pin is set to “Margin High”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default value: 1.05 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the V_{OUT} during a margin low. This command loads the unit with the voltage to which the output is to be changed when the OPERATION command or MGN pin is set to “Margin Low”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default value: 0.95 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_TRANSITION_RATE (27h)

Definition: Sets the rate at which the output should change voltage when the device receives the VOUT_COMMAND or an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default value: BA00h (1V/ms)

Units: V/ms

Range: 0.1 to 4V/ms

VOUT_DROOP (28h)

Definition: Sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A, at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with adaptive voltage positioning schemes or multi-module current sharing. In current sharing configuration, VOUT_DROOP set in each module stands for the droop seen by the load.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default value: Pin-strap setting

Units: mV/A

Range: 0 to 40mV/A

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. The initial default value is defined by a pin-strap, and this value can be overridden by writing this command from the PMBus. If an external SYNC is used, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: kHz

Range: 300kHz to 1066kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: 0000h

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15:4	Reserved	0	Reserved
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group.

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: B370h (0.86mΩ)

Units: mΩ

IOUT_CAL_OFFSET (39h)

Definition: Nulls any offsets in the output current sensing circuit for each phase and compensates for delayed measurements of current ramp due to I_{SENSE} blanking time.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: 0000h (0A)

Units: A

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.15xVOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response. Note that the device cannot be set to ignore this fault mode.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms

VOUT_OV_WARN_LIMIT (42h)

Definition: Sets the V_{OUT} overvoltage warning threshold. The power-good signal is pulled low when output voltage goes higher than this threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10xVOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_WARN_LIMIT (43h)

Definition: Sets the V_{OUT} undervoltage warning threshold. The power-good signal is pulled low when the output voltage goes lower than this threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.90xVOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.85xVOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. The device will automatically calculate peak inductor overcurrent fault limit for each phase based on the equation: $I_{OUT(PEAK\ OC\ LIMIT)} = (0.5*IOUT\_OC\_FAULT\_LIMIT+0.5*I_{RIPPLE(P-P)})*125\%$. A hard bound of 60A is applied to the peak overcurrent fault limit per phase.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EAD0h (90A)

Units: A

Range: -100A to 100A

IOUT_OC_WARN_LIMIT (4Ah)

Definition: Sets the I_{OUT} average overcurrent warning threshold. This command is available only with the FC03 and FC04 firmware.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: 0.90 * IOUT_OC_FAULT_LIMIT

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} average undercurrent fault threshold. The device will automatically calculate the valley inductor undercurrent fault limit for each phase based on the equation: $I_{OUT(VALLEY\ UC\ LIMIT)} = (0.5*IOUT\_UC\_FAULT\_LIMIT-0.5*I_{RIPPLE(P-P)})*125\%$. A hard bound of -55A is applied to the valley undercurrent fault limit per phase.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E4E0h (-50A)

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below the limit specified in OT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EBE8h (+125˚C)

Units: Celsius

Range: 0°C to +175°C

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device on what action to take in response to an over-temperature fault.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Fault Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

OT_WARN_LIMIT (51h)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB48h (+105°C)

Units: Celsius

Range: 0°C to +175°C

UT_WARN_LIMIT (52h)

Definition: Sets the temperature at which the device should indicate an under-temperature warning alarm. In response to the UT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: DC40h (-30°C)

Units: Celsius

Range: -55°C to +25°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault. Note that the temperature must rise above the limit specified in UT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E580h (-40°C)

Units: Celsius

Range: -55°C to +25°C

UT_FAULT_RESPONSE (54h)

Definition: Configures the under-temperature fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D380h (14V)

Units: V

Range: 0V to 16V

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the VIN overvoltage warning threshold. In response to the OV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Protectable: Yes

Default Value: D353h (13.3V)

Units: V

Range: 0V to 16V

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the VIN undervoltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: 1.05 x VIN_UV_FAULT_LIMIT pin-strap setting

Units: V

Range: 0V to 12V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: V

Range: 0V to 12V

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for Power-good indication. Power-good asserts with a delay specified in POWER_GOOD_DELAY after the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_WARN_LIMIT. It is recommended to set POWER_GOOD_ON higher than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9xVOUT_COMMAND pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0 to 256ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY. In multi-module current sharing configuration where ASCR is disabled for start up, the rise time of V_{OUT} can be approximately calculated by Equation 1.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0 to 200ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.
Data Length in Bytes: 2
Data Format: L11
Type: R/W
Default Value: Pin-strap setting
Units: ms
Range: 0 to 256ms

TOFF_FALL (65h)

Definition: Sets the soft-off fall time for V_{OUT} after DISABLE and TOFF_DELAY.
Data Length in Bytes: 2
Data Format: L11
Type: R/W
Default Value: Pin-strap setting
Units: ms
Range: 0 to 200ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.
Data Length in Bytes: 1
Data Format: BIT
Type: Read-only
Default Value: 00h
Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in bits 7:1 has occurred.

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read-only

Default Value: 0000h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT/POUT	An output current or output power fault or warning has occurred.
13	INPUT	An input voltage, input current, or input power fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	FANS	A fan or airflow fault or warning has occurred.
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in bits 7:1 has occurred.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Indicates an output overvoltage warning.
5	VOUT_UV_WARNING	Indicates an output undervoltage warning.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	An output overcurrent and low voltage fault has occurred.
5	IOUT_OC_WARNING	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	N/A	These bits are not used.

STATUS_INPUT (7Ch)

Definition: Returns the input voltage and input current status information.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	N/A	These bits are not used.

STATUS_TEMP (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

BIT NUMBER	MEANING
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	Packet error was detected in the PMBus command.
4:2	Not used
1	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults. VMON OV/UV warnings are set at ±10% of the VMON_FAULT commands.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default value: 00h

Units: N/A

BIT NUMBER	FIELD NAME	MEANING
7:6	Reserved	
5	VMON UV Warning	For FC01 firmware: the voltage on the VMON pin has dropped below 4V. For FC03 and FC04 firmware: the voltage on the VMON pin has dropped below 4.4V.
4	VMON OV Warning	For FC01 firmware: the voltage on the VMON pin has risen above 6V. For FC03 firmware: the voltage on the VMON pin has risen above 5.6V. For FC04 firmware: the voltage on the VMON pin has risen above 5.9V.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Reserved	
1	VMON UV Fault	The voltage on the VMON pin has dropped below the level set by VMON_UV_FAULT_LIMIT.
0	VMON OV Fault	The voltage on the VMON pin has risen above the level set by VMON_OV_FAULT_LIMIT.

READ_VIN (88h)

Definition: Returns the input voltage reading.
Data Length in Bytes: 2
Data Format: L11
Type: Read-only
Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.
Data Length in Bytes: 2
Data Format: L16u
Type: Read-only
Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.
Data Length in Bytes: 2
Data Format: L11
Type: Read-only
Default Value: N/A
Units: A

READ_INTERNAL_TEMP (8Dh)

Definition: Returns the controller junction temperature reading from internal temperature sensor. Note that the junction temperature of the power stage in the module may be higher than the READ_INTERNAL_TEMP command value, and the temperature difference depends on the operating condition. In some cases, the power stage junction temperature can be 30°C higher than the READ_INTERNAL_TEMP command value.
Data Length in Bytes: 2
Data Format: L11
Type: Read-only
Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Units: %

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Units: kHz

READ_IOUT_0 (96h)

Definition: Returns the Phase 1 current reading.
Data Length in Bytes: 2
Data Format: L11
Type: Read-only
Default Value: N/A
Units: A

READ_IOUT_1 (97h)

Definition: Returns the Phase 2 current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Default Value: N/A

Units: A

MFR_ID (99h)

Definition: Sets user defined identification. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, and perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_MODEL (9Ah)

Definition: Sets a user defined model. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, and perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_REVISION (9Bh)

Definition: Sets a user defined revision. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, and perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_LOCATION (9Ch)

Definition: Sets a user defined location identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, and perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_DATE (9Dh)

Definition: Sets a user defined date. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, and perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

Reference: N/A

MFR_SERIAL (9Eh)

Definition: Sets a user defined serialized identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, and perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

LEGACY_FAULT_GROUP (A8h)

Definition: Sets which rail DDC IDs should be listened to for fault spreading with legacy devices. The data sent is a 4-byte, 32-bit, bit vector where every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device will respond upon receiving a fault spreading event. In this vector, Bit 0 of byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with DDC ID 31.

Data Length in Bytes: 4

Data Format: BIT

Type: Block R/W

Default Value: 00000000h (No rail ID specified)

USER_DATA_00 (B0h)

Definition: Sets a user defined data. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, and perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

ISENSE_CONFIG (D0h)

Definition: Configures current sense circuitry.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 06h (256ns current sense blanking time, current sense high range)

Units: N/A

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7:4	Reserved	0000		
3:2	Current Sense Blanking Time	00	192ns	Sets the blanking time current sense blanking time.
		01	256ns	
		10	412ns	
		11	640ns	
1:0	Current Sense Range	00	Low Range	±25mV
		01	Mid Range	±35mV
		10	High Range	±50mV
		11	Not Used	

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command overrides the pin-strap settings.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: Pin-strap setting for ASCR on for Start up; ramp-up and ramp-down minimum duty cycle 0.39%; minimum duty cycle control enabled; PG is open-drain output.

Units: N/A

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7	ASCR on for Start up	0	Disabled	ASCR is disabled for start up. Use this for current sharing mode.
		1	Enabled	ASCR is enabled for start up. Use this for stand alone mode.
6:5	Reserved	0		Reserved
4:3	Ramp-up and Ramp-down Minimum Duty Cycle	00	0.39%	Sets the minimum duty-cycle during start-up and shutdown ramp.
		01	0.78%	
		10	1.17%	
		11	1.56%	
2	Minimum Duty Cycle Control	0	Disable	Control for minimum duty cycle.
		1	Enable	
1	Power-good Pin Configuration	0	Open Drain	0 = PG is open-drain output.
		1	Push-Pull	1 = PG is push-pull output.
0	Reserved	0		

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing. With pin-strap for stand alone configuration, the DDC rail ID is set according to the SMBus address. With pin-strap for multi-module current sharing, the DDC rail ID is set according to the number of devices. Device position and number of devices in the rail can be programmed as needed.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: Pin-strap setting

Units: N/A

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:13	Device Position	0, 1, 2, 3		Sets the device position in a current sharing rail. 0-Position 1; 1-Position 2; 2-Position 3; 3-Position 4
12:8	Rail ID	0 to 31 (00 to 1Fh)		Configures DDC rail ID
7:4	Reserved	0	Reserved	Reserved
3	Device Internal Phase Difference	0, 1		Sets the internal phase difference of the device. 0-phase difference is 180°; 1-phase difference is 0°.
2:0	Number of Devices in Rail	1, 3, 5, 7		Identifies the number of devices in a current sharing rail. 1-stand-alone; 3-two devices; 5-three devices; 7-four devices

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: C300h, 3ms

Units: ms

Range: 0 to 5s

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR gain is analogous to bandwidth and ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To lower transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but will not affect the peak output voltage deviation. Typical ASCR gain settings range from 50 to 1000, and ASCR residual settings range from 10 to 100.

Data Length in Bytes: 4

Data Format: CUS

Type: R/W

Default Value: Pin-strap setting

BIT	PURPOSE	DATA Format	VALUE	DESCRIPTION
31:25	Unused		0000000h	Unused
24	ASCR Enable	BIT	1	Enable
			0	Disable
23:16	ASCR Residual Setting	Integer		ASCR residual
15:0	ASCR Gain Setting	Integer		ASCR gain

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device will enable its output when its EN or OPERATION enable states, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a Power-good event on the DDC bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a Power-down event on the DDC bus.

The data field is a two-byte value. The most significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: 0000h (Prequel and Sequel disabled)

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail.
		1	Enable	Enable, prequel to this rail is defined by bits 12:8.
14:13	Reserved	0	Reserved	Reserved
12:8	Prequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the prequel rail.
7	Sequel Enable	0	Disable	Disable, no sequel following this rail.
		1	Enable	Enable, sequel to this rail is defined by bits 4:0.
6:5	Reserved	0	Reserved	Reserved
4:0	Sequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the sequel rail.

DDC_GROUP (E2h)

Definition: Configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable.

Data Length in Bytes: 3

Data Format: BIT

Type: Block R/W

Default Value: Pin-strap setting (Ignore BROADCAST VOUT_COMMAND, OPERATION, and fault for stand-alone operation. Enable BROADCAST VOUT_COMMAND, OPERATION, and fault for current sharing)

BITS	PURPOSE	VALUE	DESCRIPTION
23:22	Reserved	0	Reserved
21	BROADCAST_VOUT_COMMAND Response	1	Responds to BROADCAST_VOUT_COMMAND with same Group ID.
		0	Ignores BROADCAST_VOUT_COMMAND.
20:16	BROADCAST_VOUT_COMMAND Group ID	0-31d	Group ID sent as data for broadcast BROADCAST_VOUT_COMMAND events.
15:14	Reserved	0	Reserved
13	BROADCAST_OPERATION Response	1	Responds to BROADCAST_OPERATION with same Group ID.
		0	Ignores BROADCAST_OPERATION.
12:8	BROADCAST_OPERATION Group ID	0-31d	Group ID sent as data for broadcast BROADCAST_OPERATION events.
7:6	Reserved	0	Reserved
5	POWER_FAIL Response	1	Responds to POWER_FAIL events with same Group ID by shutting down immediately.
		0	Responds to POWER_FAIL events with same Group ID with sequenced shutdown.
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events.

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASC

Type: Block Read

Default Value: Part number/Die revision/Firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Reserved	10	
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used.
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

SYNC_CONFIG (E9h)

Definition: Sets options for SYNC output configurations.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: Pin-strap setting

SETTINGS	ACTIONS
00h	Use internal clock. Clock frequency is set by pin-strap or PMBus command.
02h	Use internal clock and output internal clock.
04h	Use external clock.

SNAPSHOT (EAh)

Definition: 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, last updated values are stored to the flash memory. When the SNAPSHOT STATUS bit is set to stored, the device will no longer automatically capture parametric and status values following fault until stored data are erased. Use SNAPSHOT_CONTROL command to erase store data and clear the status bit before next ramp up. Data erase is not allowed when the module is enabled.

Data Length in Bytes: 32

Data Format: Bit field

Type: Block Read

BYTE NUMBER	VALUE	PMBUS COMMAND	FORMAT
31:23	Reserved	Reserved	00h
22	Flash Memory Status Byte FF - Not Stored 00 - Stored	N/A	BIT
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	Reserved	Reserved	00h
11:10	Internal Temperature	READ_INTERNAL_TEMP (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Highest Measured Output Current	N/A	L11
5:4	Output Current	READ_IOUT (8Ch)	L11
3:2	Output Voltage	READ_VOUT (8Bh)	L16u
1:0	Input Voltage	READ_VIN (88h)	L11

BLANK_PARAMS (EBh)

Definition: Returns a 16-byte string indicating which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A one indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Data Length in Bytes: 16

Data Format: BIT

Type: Block Read

Default Value: FF...FFh

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h will cause the device to copy the current Snapshot values from NVRAM to the 32-byte Snapshot command parameter. Writing a 02h will cause the device to write the current Snapshot values to NVRAM, 03h will erase all Snapshot values from NVRAM. Write (02h) and Erase (03h) can be used only when the device is disabled. All other values will be ignored.

Data Length in Bytes: 1

Data Format: Bit field

Type: R/W byte

VALUE	DESCRIPTION
01h	Read Snapshot values from NV RAM
02h	Write Snapshot values to NV RAM
03h	Erase Snapshot values stored in NV RAM.

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Data Length in Bytes: 0

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Reads the VMON OV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CB00h (6V)

Units: V

Range: 4V to 6V

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Reads the VMON UV fault threshold

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CA00h (4V)

Units: V

Range: 4V to 6V

MFR_READ_VMON (F7h)

Definition: Reads the VMON voltage.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: N/A

Units: V

Range: 4V to 6V

VMON_OV_FAULT_RESPONSE (F8h)

Definition: Reads the VMON OV fault response
Data Length in Bytes: 1
Data Format: BIT
Type: Read only
Default Value: 80h (Disable and no retry)
Units: N/A

VMON_UV_FAULT_RESPONSE (F9h)

Definition: Reads the VMON UV fault response, which is a direct copy of VIN_UV_FAULT_RESPONSE
Data Length in Bytes: 1
Data Format: BIT
Type: Read only
Default Value: 80h (Disable and no retry)
Units: V

Datasheet Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Visit the website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Nov 9, 2017	FN8704.4	- Added ISL8273MDIRZ to Ordering Information on page 3. - Added FC04 to firmware revision graphic on page 3. - Updated Pin Configuration graphic on page 3. - Updated Table 3 on page 16 with FC04-specific values. - Updated Table 9 on page 21 with information about FC03 and FC04. - Updated IOUT_OC_WARN_LIMIT (4Ah) descriptions on pages 25 and 33. - Updated STATUS_MFR_SPECIFIC description on page 41. - Updated READ_INTERNAL_TEMP description on page 42. - Added FC04 to Firmware Revision History on page 53.
May 9, 2017	FN8704.3	- Updated the Ordering Information table on page 3 by adding part number ISL8273MCIRZ. - Added a nomenclature guide on page 3. - Added Notes 1 and 2 on page 3. - Removed STORE_DEFAULT_ALL and RESTORE_DEFAULT_ALL commands from PMBus guidelines - Added and edited descriptions which pertain to changes made in FC03 firmware from FC01/FC02 firmware 1) Added command IOUT_OC_WARN_LIMIT 2) Added to Table 9 Current Sharing Resistor Settings based on FC03 firmware changes 3) Updated description for PMBus command DDC_CONFIG(D3h) and description for Phase Spreading. - Added in SMBus Communications the requirement for pin-strap resistor to have 1% tolerance or better - Updated Table 1 ISL8273M design guide matrix and output voltage response for the condition of VIN=5V, VOUT=1V, FREQ=300kHz -Updated the Firmware Revision History section. -POD Y58.18x23 updated from rev 1 to rev 3. Changes since rev 1: 1) Pages 1 and 2 of POD Y58.18x23 remain unchanged for this update. 2) Delete remaining pages 3-5 of existing POD and replace with new pages 3-12. New drawings - 2 drawings per page - POD is now 7 pages. 3) On -page 2, In "SIZE DETAILS FOR THE 16 EXPOSED PADS" (BOTTOM VIEW) changed dimension 8.40 (2X) to 8.30 (2x) and 8.00 (2x) to 1.00 (2X).
March 16, 2016	FN8704.2	Added “PMBus Use Guidelines” on page 28. Updated POD Y58.18x23 to the latest revision changes are as follows: -Detail A on page 1: Added Reference Radius for rounded corners on small I/O pads.
September 10, 2015	FN8704.1	-Updated text on page 1. -Added a paragraph under “Soft-Start, Stop Delay, and Ramp Times” on page 16 to explain the internal start-up procedure after power is applied to the VDD pin. -Updated command description for VOUT_COMMAND, “This command cannot set a value higher than VOUT_MAX.” -Updated the range for commands TON_DELAY and TOFF_DELAY on page 38 to “0ms to 256ms”.
June 11, 2015	FN8704.0	Initial Release

Firmware Revision History

TABLE 10. ISL8273M NOMENCLATURE GUIDE

FIRMWARE REVISION CODE	CHANGE DESCRIPTION	NOTE
ISL8273-000-FC04	- Changed VMON OV warning limit to 5.9V - Enhanced current balance between the two internal phases - Added three values for VSET pin-strap: 0.72V, 0.88V, and 0.92V	Recommended for new designs
ISL8273-000-FC03	- Enhanced fault management during start-up. - Enhanced IOUT UC fault management during start-up. - Enhanced PMBus immunity to noise and lockup. - Added IOUT_OC_WARN_LIMIT command. - Added the IOUT_OC_WARNING function bit in the STATUS_IOUT command. - Added paged ISENGain and ISENOffset factors which are storable in default memory. - Added temperature compensation for the paged ISENGain and ISENOffset factors and reduced temperature drift. - Improved intra-device current balance within the two internal phases. - Fixed the synchronization issue during VOUT_COMMAND change on-the-fly in current sharing conditions. - Added more pin-strap resistor settings for CS pin for four-module current sharing conditions. - Added the capability to change the device internal phase difference from 180° to 0° in DDC_CONFIG and optimized module-to-module phase shift in Current Sharing mode. - Changed VMON OV warning limit to 5.6V and VMON UV warning limit to 4.4V	Not recommended for new designs
ISL8273-000-FC02	Skip	Not recommended for new designs
ISL8273-000-FC01	Initial Release	Not recommended for new designs

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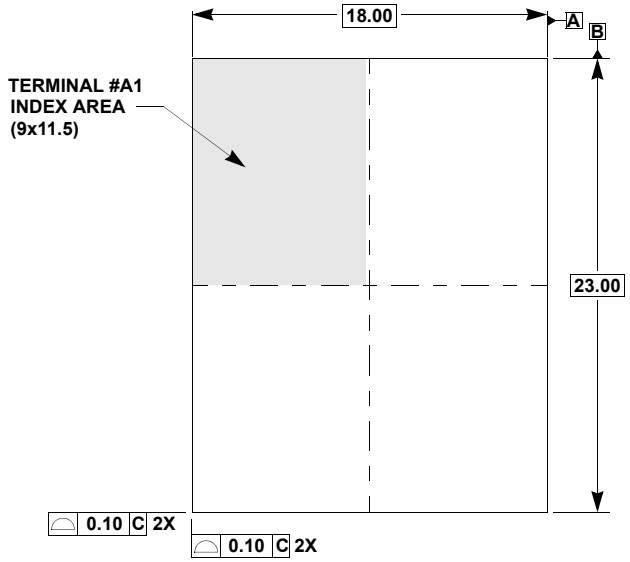
Package Outline Drawing

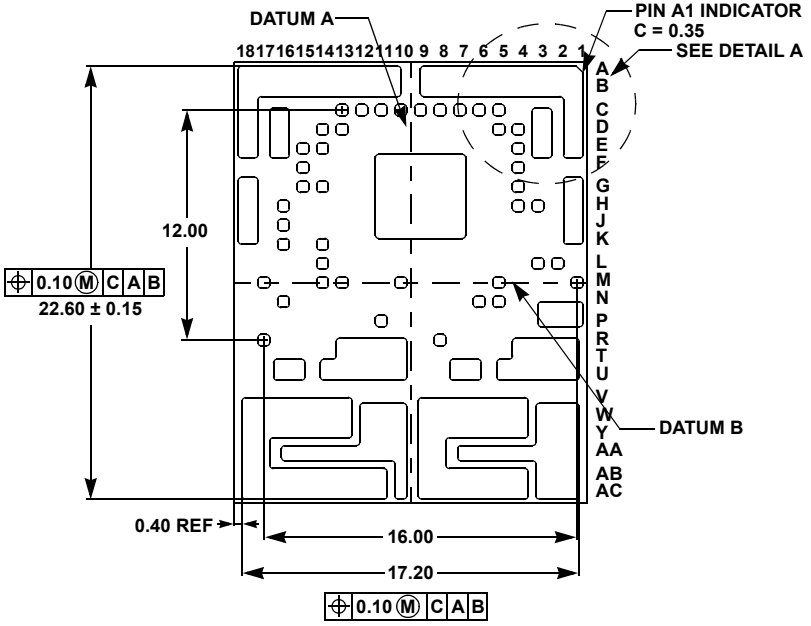
Y58.18x23

58 I/O 18mmx23mmx7.5mm CUSTOM HDA MODULE
Rev 3, 12/16

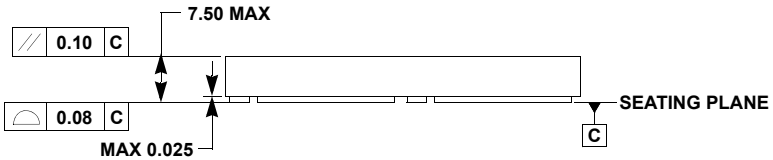
For the most recent package outline drawing, see Y58.18x23.



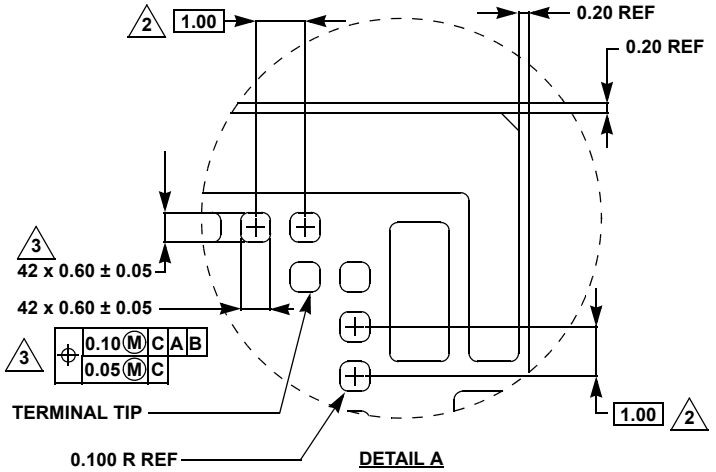
TOP VIEW



BOTTOM VIEW



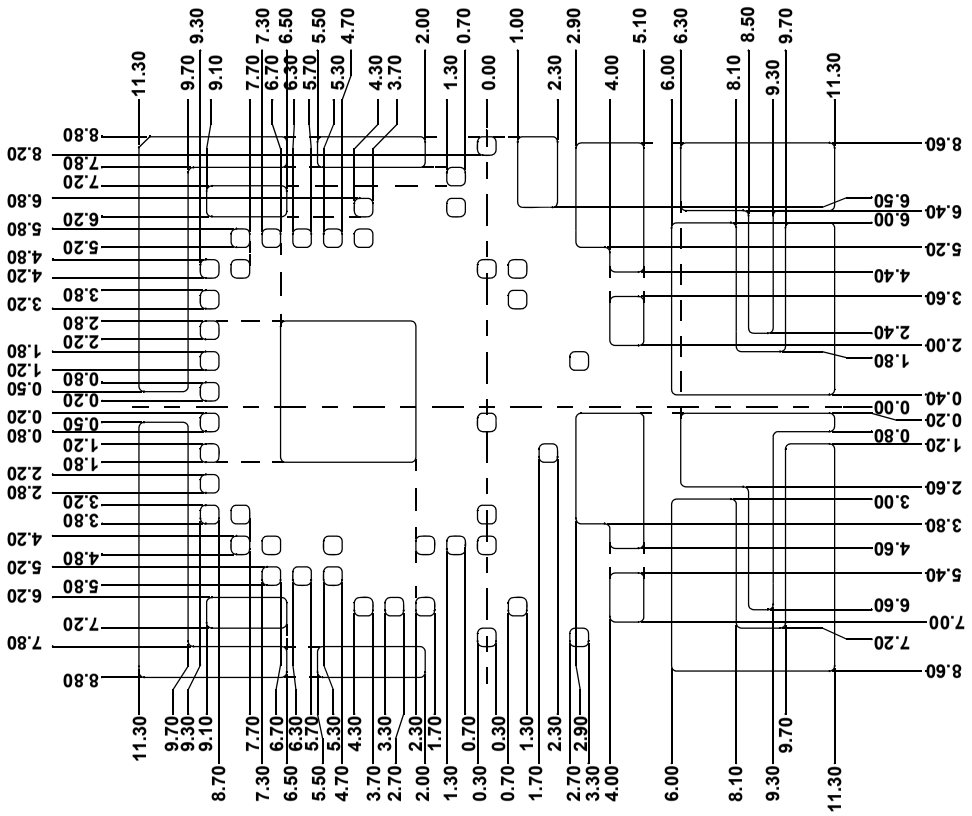
SIDE VIEW



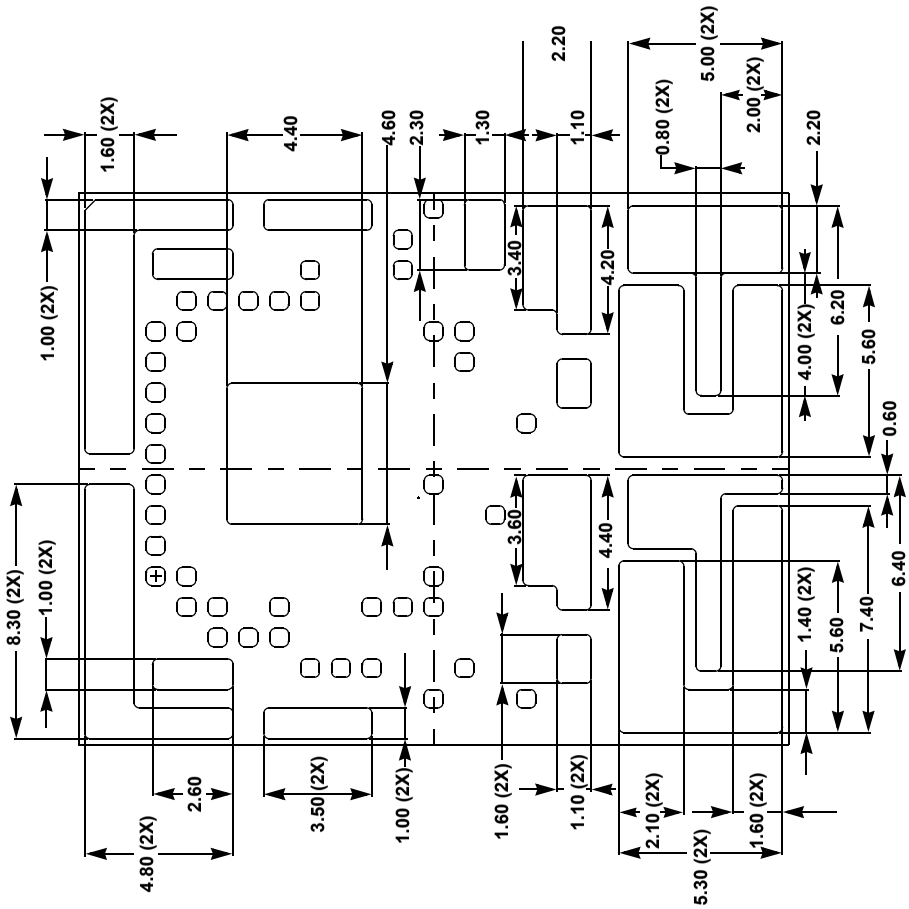
DETAIL A

NOTES:

1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 42 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension on page 3 is ±0.1mm.

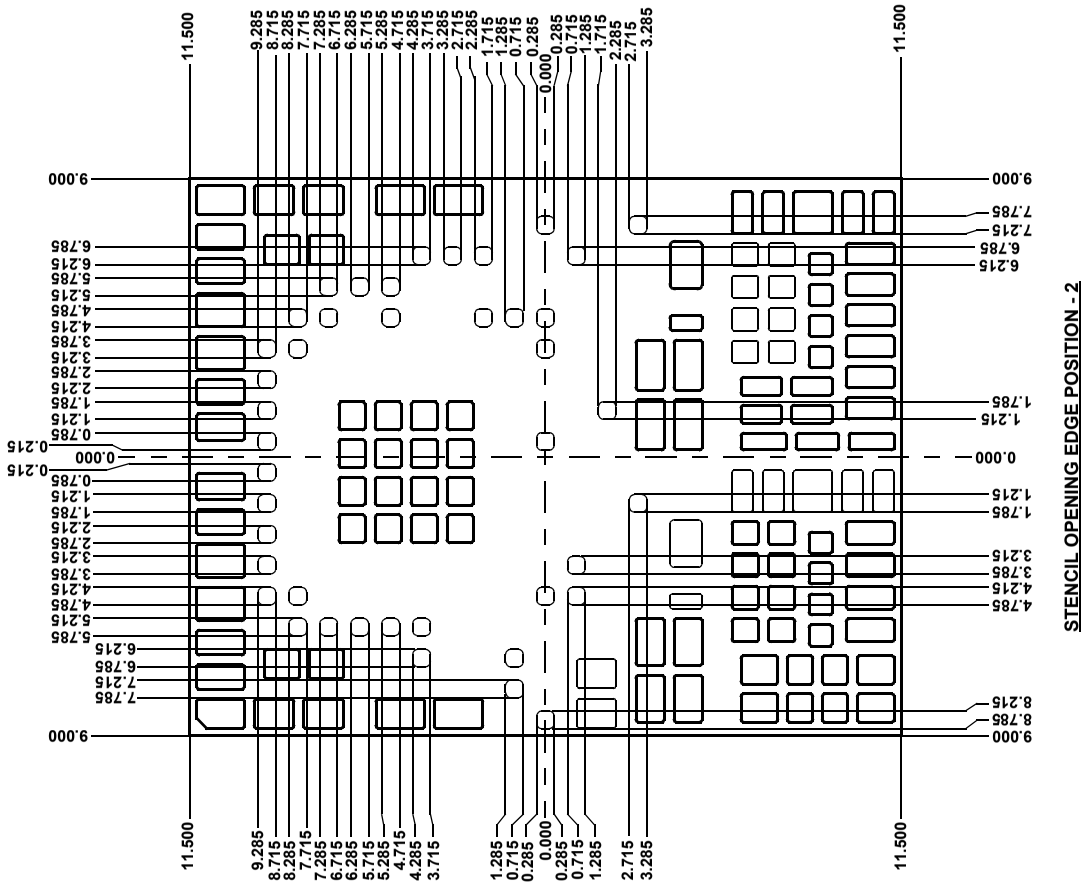


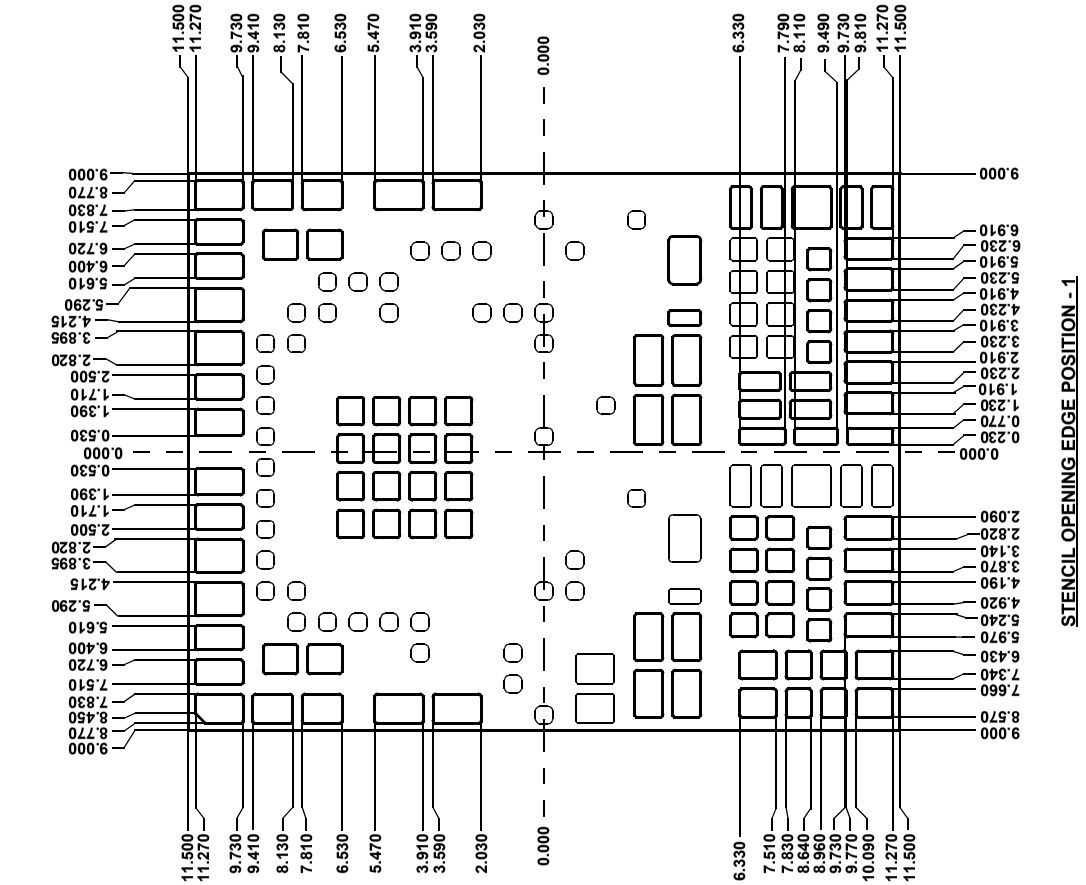
TERMINAL AND PAD EDGE DETAILS

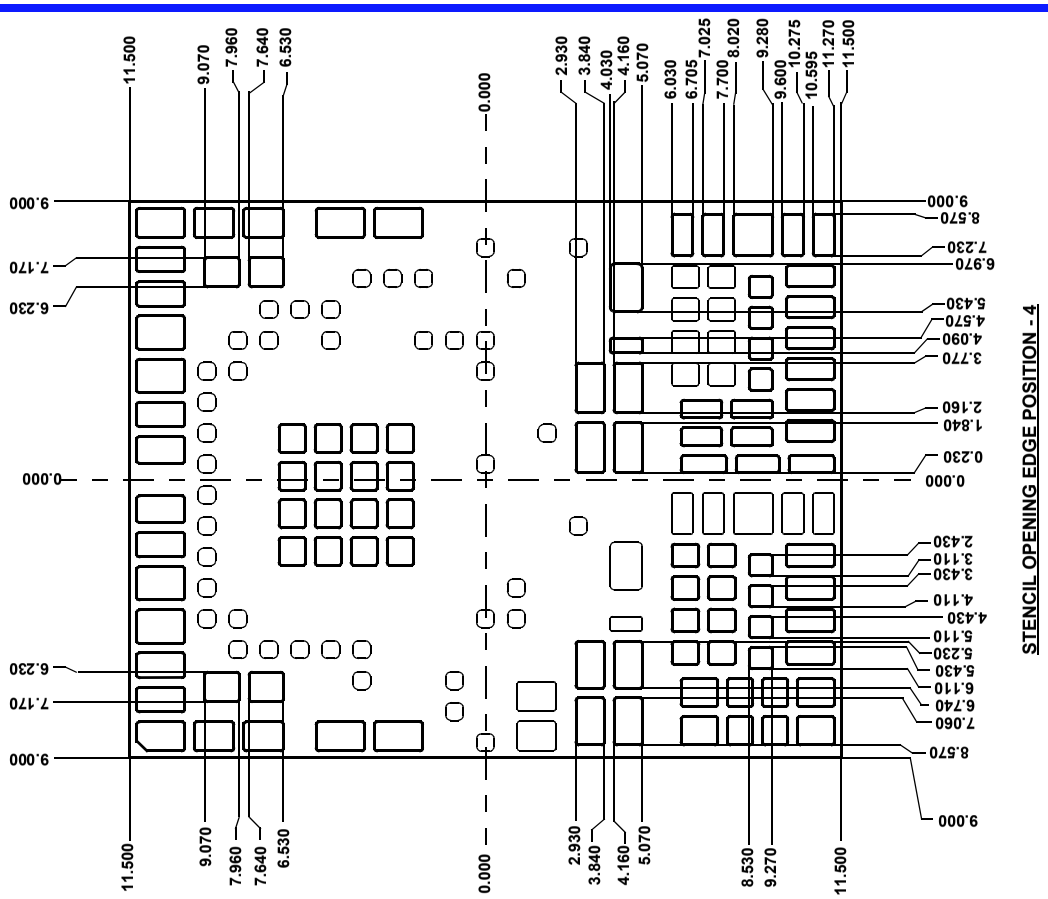


BOTTOM VIEW

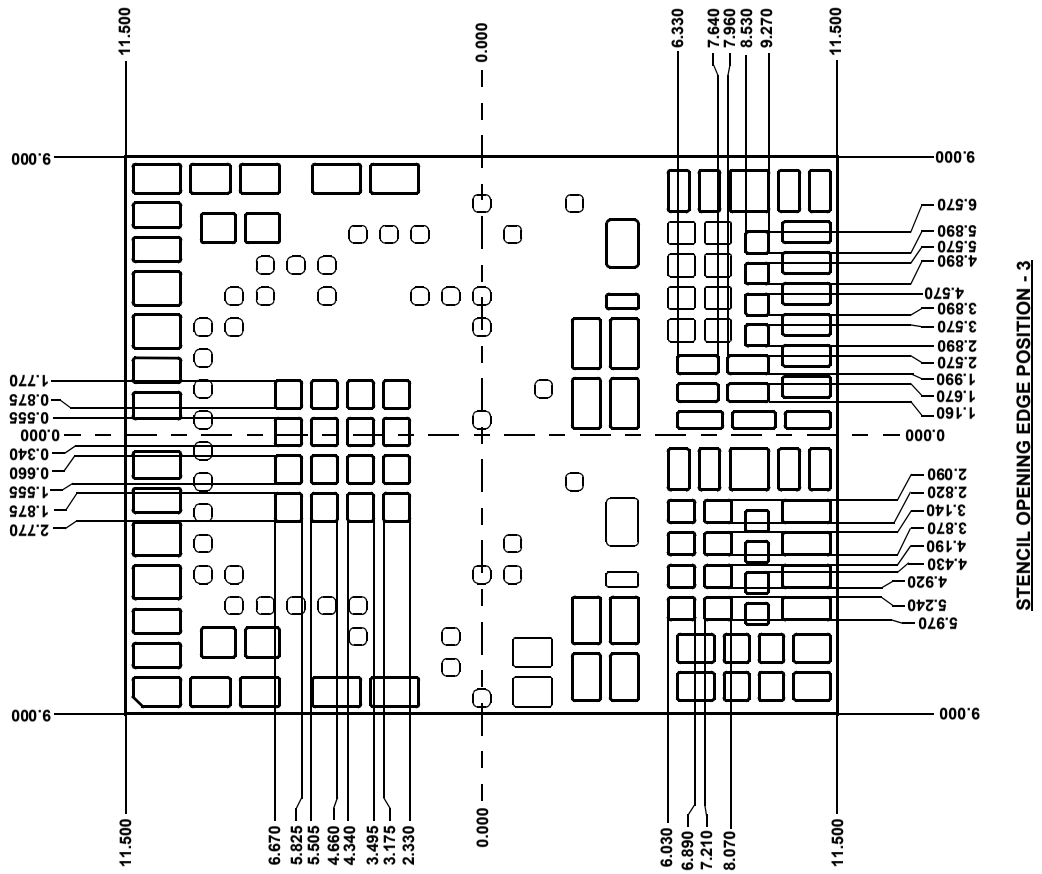
SIZE DETAILS FOR THE 16 EXPOSED PADS


STENCIL OPENING EDGE POSITION - 2

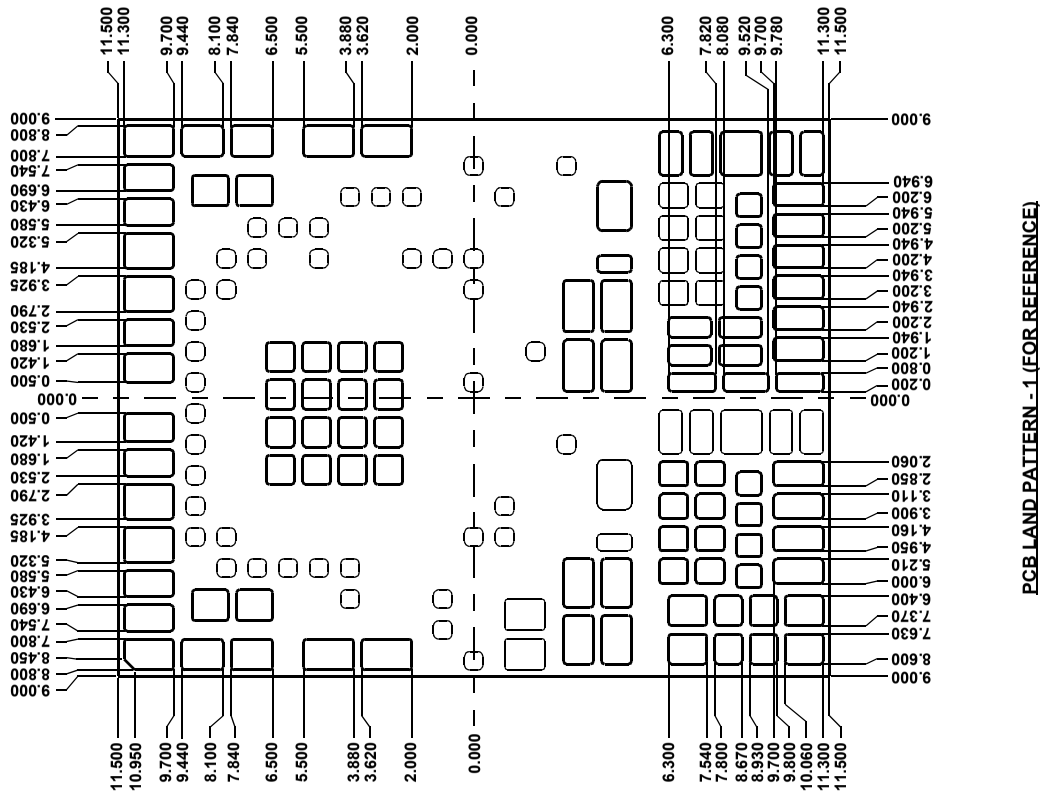

STENCIL OPENING EDGE POSITION - 1



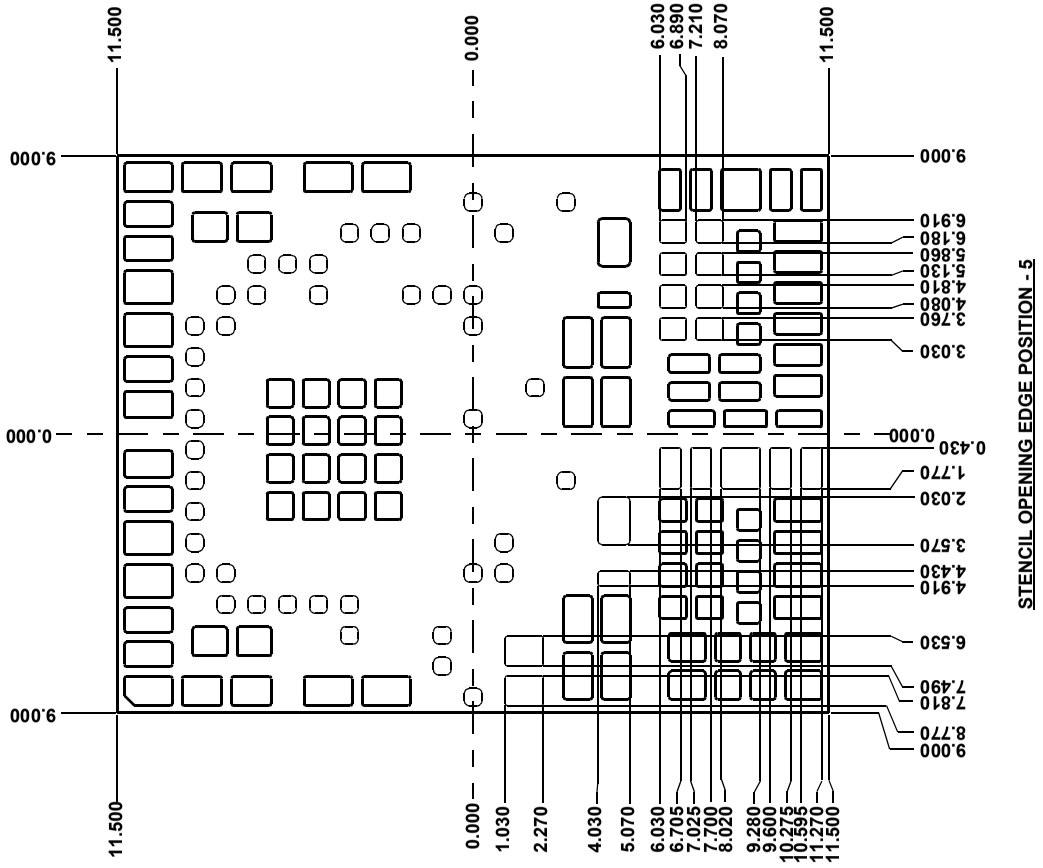
STENCIL OPENING EDGE POSITION - 4



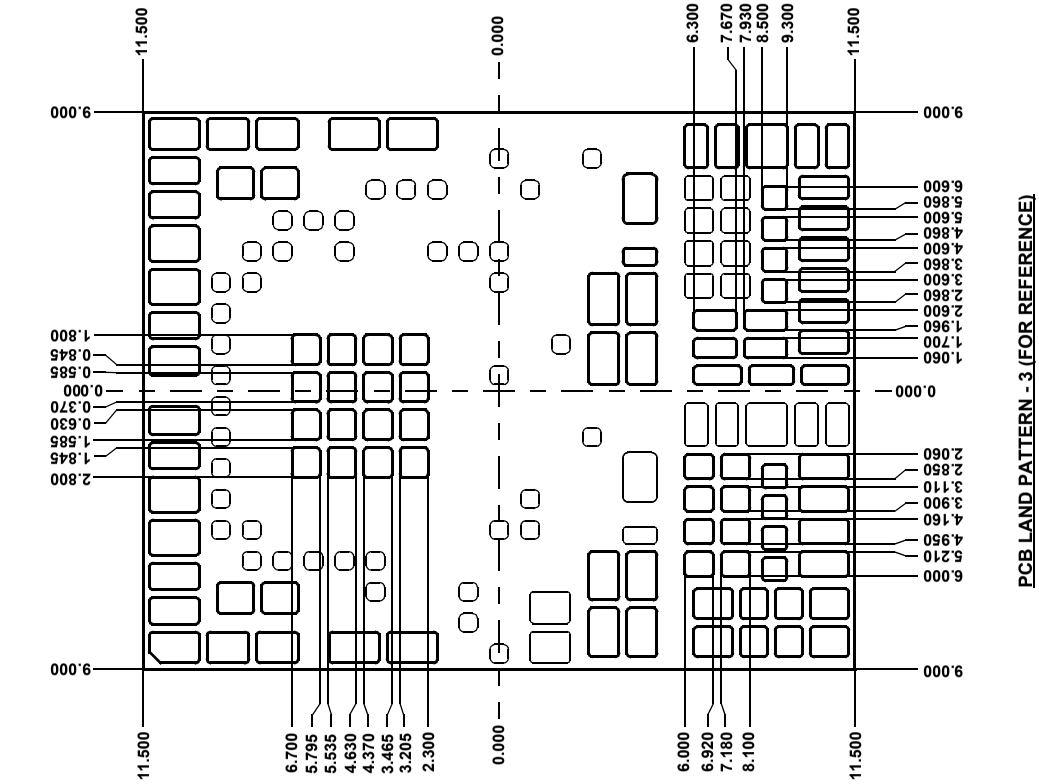
STENCIL OPENING EDGE POSITION - 3



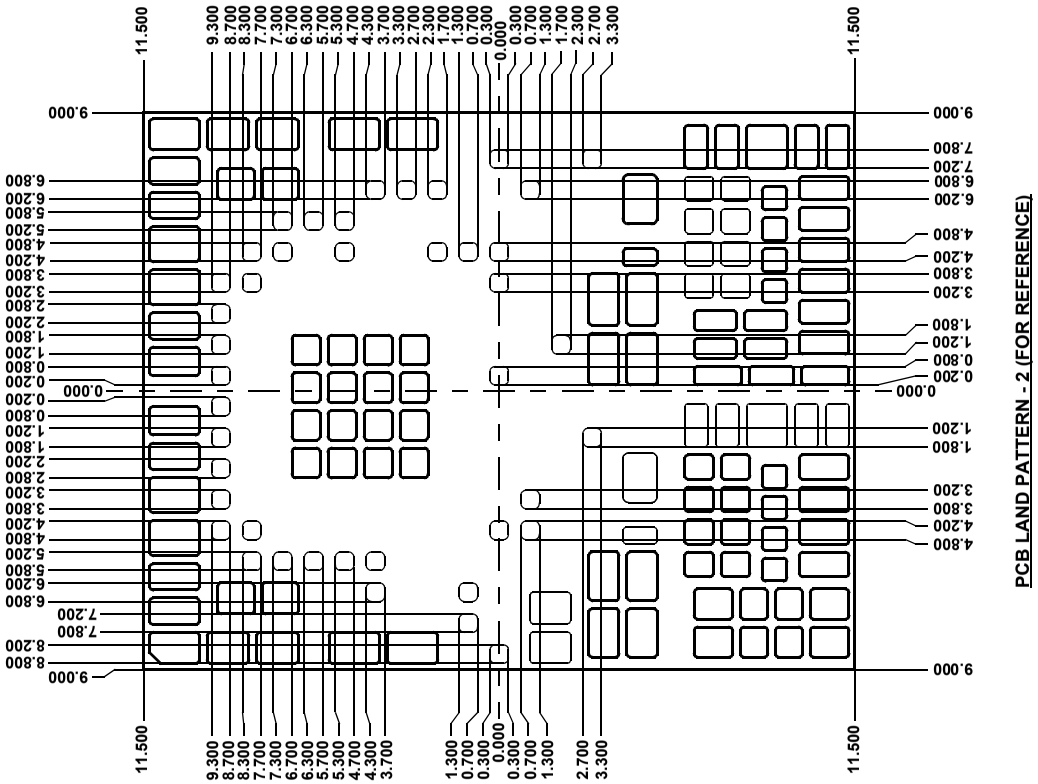
PCB LAND PATTERN - 1 (FOR REFERENCE)



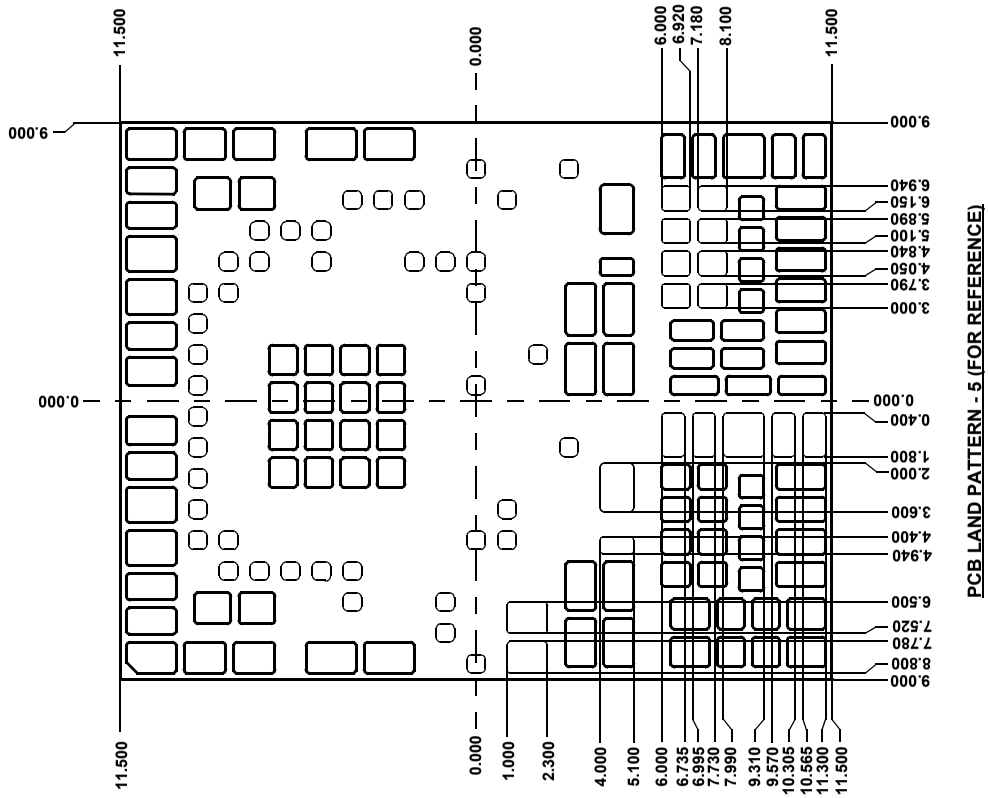
STENCIL OPENING EDGE POSITION - 5



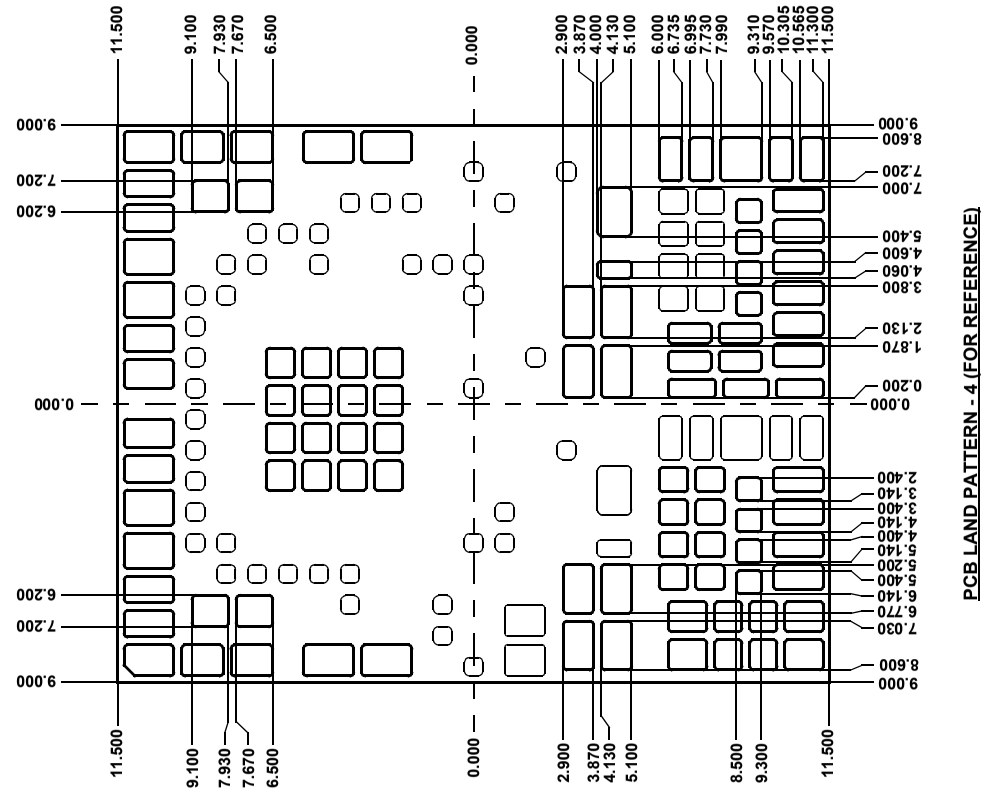
PCB LAND PATTERN - 3 (FOR REFERENCE)



PCB LAND PATTERN - 2 (FOR REFERENCE)



PCB LAND PATTERN - 5 (FOR REFERENCE)



PCB LAND PATTERN - 4 (FOR REFERENCE)