SOC Octal Wide Voltage PMU/Load

ISL55185

The ISL55185 is a highly integrated System-on-a-Chip pin electronics solution incorporating 8 independent channels of:

- PMU
- Active load
- External force/external sense

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.

Applications

- Automated test equipment
- Instrumentation
- ASIC verifiers

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Features

- Per channel active load
  - 24mA maximum current
  - MI capability
  - Independent source and sink current levels
  - Extremely low HiZ leakage over a 32V range
  - 32V Input compliance/28V Output forcing range
  - Extremely low input leakage over a 32V range
- Per channel PMU
  - FV/MI/MV
  - 5 current ranges (24mA, 4mA, 400µA, 40µA, 4µA)
  - FV current clamps
  - 32V Input compliance/28V output forcing range
  - Extremely low input leakage over a 32V range
- Monitor
  - Differential per channel monitor with HiZ
  - Differential central monitor with HiZ
- External force/sense per channel
- 3-bit serial port
- On-chip DAC to generate DC levels
  - 4 DC levels per channel (16 bits/level)
  - On-chip offset and gain correction per level
- Package/power dissipation
  - Pb-free (RoHs Compliant)
  - 128 Lead, 14mm x 20mm LQFP w/Heat Slug
  - Pdq ≤ 250mW/channel; Pdq ≤ 2W/chip

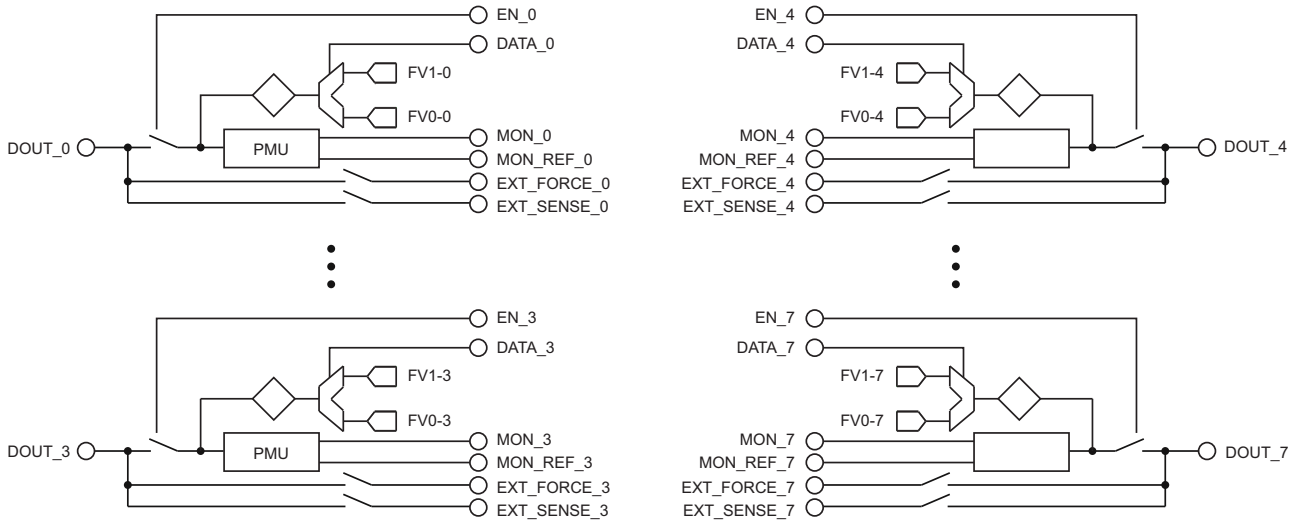

FIGURE 1. BLOCK DIAGRAM

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Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
99, 100 3, 2 128, 1 102	EXT_FORCE_0, EXT_SENSE_0 MON_0, MON_REF_0 DATA_0, EN_0 DOUT_0	Channel 0 External Force and Sense. Channel 0 differential monitor output pins. Channel 0 real time control inputs. Channel 0 I/O pin.
94, 95 8, 7 5, 6 97	EXT_FORCE_1, EXT_SENSE_1 MON_1, MON_REF_1 DATA_1, EN_1 DOUT_1	Channel 1 External Force and Sense. Channel 1 differential monitor output pins. Channel 1 real time control inputs. Channel 1 I/O pin.
89, 90 13, 12 10, 11 92	EXT_FORCE_2, EXT_SENSE_2 MON_2, MON_REF_2 DATA_2, EN_2 DOUT_2	Channel 2 External Force and Sense. Channel 2 differential monitor output pins. Channel 2 real time control inputs. Channel 2 I/O pin.
84, 85 18, 17 15, 16 87	EXT_FORCE_3, EXT_SENSE_3 MON_3, MON_REF_3 DATA_3, EN_3 DOUT_3	Channel 3 External Force and Sense. Channel 3 differential monitor output pins. Channel 3 real time control inputs. Channel 3 I/O pin.
79, 80 23, 22 20, 21 82	EXT_FORCE_4, EXT_SENSE_4 MON_4, MON_REF_4 DATA_4, EN_4 DOUT_4	Channel 4 External Force and Sense. Channel 4 differential monitor output pins. Channel 4 real time control inputs. Channel 4 I/O pin.
74, 75 28, 27 25, 26 77	EXT_FORCE_5, EXT_SENSE_5 MON_5, MON_REF_5 DATA_5, EN_5 DOUT_5	Channel 5 External Force and Sense. Channel 5 differential monitor output pins. Channel 5 real time control inputs. Channel 5 I/O pin.
69, 70 33, 32 30, 31 72	EXT_FORCE_6, EXT_SENSE_6 MON_6, MON_REF_6 DATA_6, EN_6 DOUT_6	Channel 6 External Force and Sense. Channel 6 differential monitor output pins. Channel 6 real time control inputs. Channel 6 I/O pin.
64, 65 38, 37 35, 36 67	EXT_FORCE_7, EXT_SENSE_7 MON_7, MON_REF_7 DATA_7, EN_7 DOUT_7	Channel 7 External Force and Sense. Channel 7 differential monitor output pins. Channel 7 real time control inputs. Channel 7 I/O pin.
Central Resource Pins		
116	TEST_IN	Analog input used to bypass the DAC for test purposes.
44, 113	V_REF, R_EXT	External precision voltage and resistance reference.
45	DUT_GND	Analog voltage input used to track ground at the DUT.
123, 122, 121, 120	DG_A, DG_B, DG_C, DG_D	Optional DUT_GND inputs.
109, 108	TEMP_N, TEMP_P	Terminals of an on-chip thermal diode.
115, 114	MONITOR, MON_REF	Central monitor differential analog output.
CPU Interface		
55, 54, 56, 57	CK, SDIO, STB, RESET	3 bit serial port (Clock, Data and Strobe) and Reset.
External Monitor Control		
51	EXT_MON_OE	External Monitor output enable control.
49, 48, 47	EXT_MON_SEL_<2:0>	External Monitor selection control bits.
Temperature Monitor		
112	TJ	On-chip die temperature monitor output.
52	EXT_TJ_OE	External TJ monitor enable.

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Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
Power Supplies		
62, 63, 68, 73, 78, 83, 88, 93, 98, 103, 104, 105	VCC	Analog positive power supply.
60, 61, 66, 71, 76, 81, 86, 91, 96, 101, 106, 107	VEE	Analog negative power supply.
40, 41, 50, 58, 111, 118, 126, 127	VDD	Digital power supply.
4, 9, 14, 19, 24, 29, 34, 39, 42, 43, 53, 59, 110, 117, 124, 125	GND	Digital ground.

Pin Configuration

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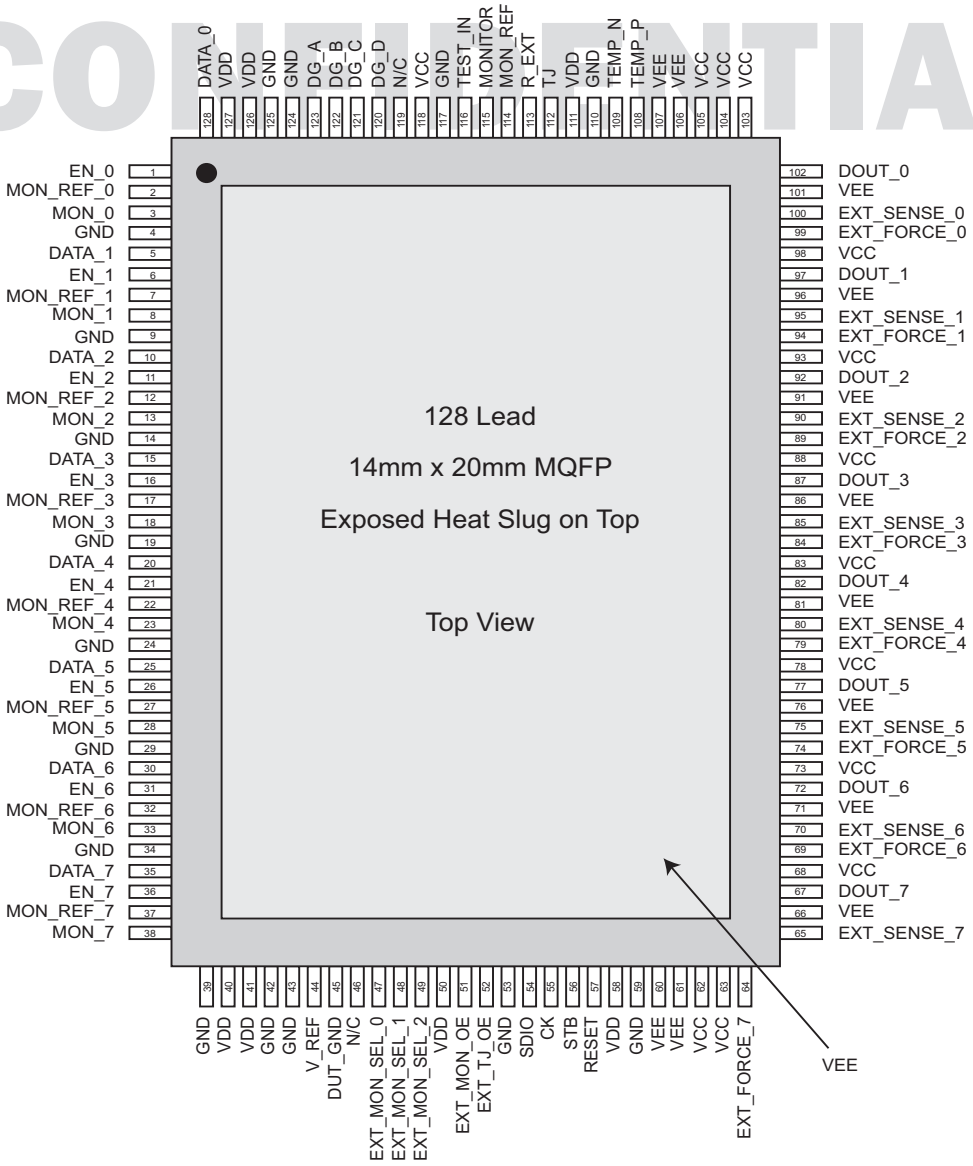

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	VDD – 0.5		+32	V
VEE	–22		+0.5	V
VDD	+0.5		+5	V
VCC – VEE	0		+34	V
Output Voltage				
FORCE, SENSE	VEE – 0.5		VCC + 0.5	V
Output Currents				
COMP_A, COMP_B	–80		+20	mA
SDIO	–10		20	mA
External References				
V_REF	GND – 0.4		VDD + 0.4	V
EXT_SENSE	VEE – 0.4		VCC + 0.4	V
EXT_FORCE	VEE – 0.4		VCC + 0.4	V
Thermal Information				
Typical Thermal Resistance θJA (Note 1)		32		°C/W
Typical Thermal Resistance θJC (Note 2)		0.9		°C/W
Junction Temperature	55		150	°C

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CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θJA is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. For θJC, the “case temp” location is taken at the package top center.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	+10		+29	V
VEE	–20		–3	V
VDD	+3.25		+3.45	V
GND		0		V
VCC – VEE	+13		+33	V
Digital Inputs				
CK, SDIO, STB, RESET	GND		VDD	V
PPMU Levels				
FV-0#, FV1-#	VEE + 2		VCC – 2	V
External References				
V_REF	+2.99		+3.01	V
R_EXT		10		KΩ
EXT_SENSE	VEE		VCC	V
EXT_FORCE	VEE		VCC	V
Miscellaneous				
Junction Temperature	+25		100	°C
CPU Port CK Frequency	10		25	MHz
Capacitive Load at DOUT_#		1		nF

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DC Electrical Specifications

For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications - Power Supplies

VCC = +29V, VEE = –4V, VDD = +3.45V, V_REF = +3V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	Pd (Typ)
No Load							**2.75W/Chip**
11010	ICC	Note 1	50	80	115	mA	2,320mW
11020	IEE	Note 1	50	80	115	mA	320mW
11030	IDD	Note 1	18	30	43	mA	106mW
+3.0mA Load/Channel							**3.39W/Chip**
11110	ICC	Note 2	75	100	140	mA	2,900mW
11120	IEE	Note 2	60	90	125	mA	360mW
11130	IDD	Note 2	22	40	47	mA	132mW
+10mA Load/Channel							**5.69W/Chip**
11210	ICC	Note 3	135	170	210	mA	4,930mW
11220	IEE	Note 3	120	155	200	mA	620mW
11230	IDD	Note 3	25	43	50	mA	142mW

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NOTES:

1. All channels tested simultaneously. FV = +10V; Isource/Isink = 0mA (uncalibrated); No external load.
2. All channels tested simultaneously. FV = +10V; Isource/Isink = 3mA (uncalibrated); No external load
3. All channels tested simultaneously. FV = +10V; Isource/Isink = 10mA (uncalibrated); No external load

DC Electrical Specifications - CPU Port

VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SDIO, CK, STB, RESET						
17100	VIH		2.0			V
17110	VIL				0.8	V
17120	Iin Input Leakage Current	Tested at +3V	–100	0	+100	nA
17200	VOH (SDIO Only)	Output Current = 4mA	2.4			V
17210	VOL (SDIO Only)	Input Current = 4mA			0.8	V

DC Electrical Specifications - Digital Inputs

VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DATA, EN, EXT_MON_OE, EXT_MON_SEL<2:0>, EXT_TJ_OE						
13260	VIH		2.0			V
13261	VIL				0.8	V
13262	Iin (Input Leakage Current) (HiZ)	Tested at +3V	–100	0	+100	nA

DC Electrical Specifications - Analog Pins

VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
10999	V_REF Input Current @ 3V		–100	0	+100	nA
10998	DUT_GND, DG_A(B)(C)(D) Input Current	Tested at 0V, –2.5V, +4V	–100	0	+100	nA
14741	DUT_GND, DG_A(B)(C)(D) Error	FV = +3V measured through the monitor. DUT_GND, DG_A(B)(C)(D) = ±300mV	–5		+5	mV
	TEST_IN Input Current	Tested at (VCC+VEE)/2, VEE, VCC		±20		nA
13262	TJ Input Leakage (HiZ)	Tested at +3V	–100		+100	nA
	TJ Maximum Output Current	Limits established by characterization and are not production tested.		1		mA
	TJ(V)/VDD Sensitivity	Limits established by characterization and are not production tested.		1.25		mV/mV

DC Electrical Specifications - Level DAC Calibration

All DC tests are performed after the DAC is first calibrated. The upper 5 bits of the DAC are calibrated in the sequence D11 to D15. The DAC Cal bits are adjusted to make the major carries as small as possible.. VCC = +28.9V, VEE = -3.9V, VDD = 3.25V, V_REF = +3V, GND = 0V.

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SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
16510	D15 Step Error	(DAC @ 8000 – DAC @ 7FFF) – DAC LSB; Code 8000 – Code 7FFF – LSB; VR1	–5		+5	mV
16520	D14 Step Error	(DAC @ 7000 – DAC @ 3000) – DAC LSB; Code 4000 – Code 3FFF – LSB; VR1	–5		+5	mV
16530	D13 Step Error	(DAC @ 7000 – DAC @ 5000) – DAC LSB; Code 6000 – Code 5FFF – LSB; VR1	–5		+5	mV
16540	D12 Step Error	(DAC @ 7000 – DAC @6000)) – DAC LSB;Code 7000 – Code 6FFF – LSB; VR1	–5		+5	mV
16550	D11 Step Error	(DAC @ 7800 – DAC @ 7000)) – DAC LSB; Code 7800 – Code 77FF – LSB; VR1	–5		+5	mV

DAC

There are 3 on-chip internal DACs per channel used for DC Level, DC Level Offset Correction, and DC Level Gain Correction. DAC testing is performed post-DAC Calibration. These on-chip DACs are not used off-chip explicitly as stand-alone outputs. Rather, they are internal resources that are used by every functional block. The DACs are tested many times over by the DC tests for driver, comparator and PMU. However, the DACs are specifically tested independently from all other functional blocks to verify basic functionality.

DC Electrical Specifications - DAC

VCC = +28.9V, VEE = -3.9V, VDD = +3.25V, V_REF = +3V, GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Level DAC Test						
16100	Span	Notes 4, 5 and 7	7.6	8.2	8.6	V
16110	Linearity Error	Notes 4, 5 and 6	–5	0	+5	mV
16120	Bit Test Error	Notes 4, 5 and 8	–5	0	+5	mV
16190	Droop Test	Note 9	–300		+300	µV/ms
16400	DAC Noise	Note 10			+1.0	mV
Offset DAC Test						
16200	+Adjustment Range	Notes 4, 11 and 12	+4.5	+5.2	+6.0	% of Span
16210	–Adjustment Range	Notes 4, 11 and 12	–4.5	–5.2	–6.0	% of Span
16220	Linearity Error	Notes 4, 6and 11	–5	0	+5	mV
16230	Bit Test Error	Notes 4, 8 and 11	–5	0	+5	mV
Gain DAC Test						
16300	+Adjustment Range	Notes 4 and 13	1.07	1.125	1.15	V/V
16310	–Adjustment Range	Notes 4 and 13	0.850	0.875	.922	V/V
16320	Linearity Error	Notes 4, 6 and 13	–3	0	+3	mV/V
16330	Bit Test Error	Notes 4, 8 and 13	–3	0	+3	mV/V
Vmid DAC Test						
16800	Linearity Error	Notes 4 and 14	–10	0	+10	mV

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NOTES:

4. DAC tests performed using the PMU in FV mode and the MONITOR output VR1.
5. Offset and Gain DACs both programmed to mid-scale (Code 7FFF).
6. Linearity Test: 17 equal spaced codes relative to a straight line determined by 3/17 and 15/17 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF, 4FFFF, 5FFFF, 6FFFF, 7FFFF, 8FFFF, AFFFF, BFFFF. CFFF, **DFFF**, EFFF, FFFF.
7. Span = DAC(FFFF) - DAC (0000).
8. Bit Test - Walking 1 and walking 0 to determine bit weight: 1's: 8000, 4000, 2000, 100, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001; 0's: 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE.
9. CPU CK turned off. 66ms delay between measurements. Each DC level on the chip checked one at a time.
10. FV = 0, VR2, Measured at FORCE_0, RMS measurement.
11. Level and gain DACs both programmed to mid-scale (Code 7FFF).
12. Code 0000, FFFF relative to mid-scale (7FFF).
13. Level DAC = FFFF, Offset DAC = 7FFF.
14. Linearity Test - 16 codes relative to a straight line determined by 2/16 and 13/16 measurement points: 0000, 0001, **0010**, 0011 ... 1100, **1101**, 1110, 1111. DAC Code = 7FFF, FV Mode

Force Voltage

CHANNEL CONFIGURATION

1. Feedback# = DOUT_#
2. Isource-#/Isink-# = 15.6mA
3. Load-BP# = 0

The sequence of events performed for FV testing is:

1. Program VF#
2. Force current at DOUT_#
3. Measure the voltage at DOUT_# using MV.

FV TESTS

1. VR0-VR3 tested in IR3
2. VR3 tested in all current ranges , VEE

DC Electrical Specifications– Force Voltage

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV (Post Calibration)						
14200	Output Force Error	Note 15, VR0, (Table 1, TPFV0)	–5		+5	mV
14201	Output Force Error	Note 15, VR1, (Table 1, TPFV1)	–10		+10	mV
14202	Output Force Error	Note 15 VR2, (Table 1, TPFV2)	–20		+20	mV
14203	Output Force Error	Note 15, VR3, (Table 1, TPFV3A)	–30		+30	mV
14213	Output Force Error	Note 15, VR3, (Table 1, TPFV3B)	–50		+50	mV
	FV Temperature Coefficient	Notes 16,17, 22; VR3.		<800		µV/°C
	Short Circuit Output Current	Notes 16, 18, 22		48		mA
HIZ Leakage						
14090	DOUT_# HiZ	Notes 16, 19	–20		+20	nA
14091	DOUT_# HiZ	Notes 16, 20	–30		+30	nA
10997	EXT_FORCE_#, EXT_SENSE_#, HiZ	Notes 16, 19	–20		+20	nA
10996	EXT_FORCE_#, EXT_SENSE_#, HiZ	Notes 16, 20	–20		+20	nA
Capacitance						
	DOUT_# Capacitance	Note 22		110		pF
	EXT_FORCE_# Capacitance	Note 22		5		pF
	EXT_SENSE_# Capacitance	Note 22		5		pF

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NOTES:

15. VCC = +28.9V, VEE = -3.9V, VDD = +3.25V, V_REF = +3V, GND = 0V.
16. VCC = +29V, VEE = -4, VDD = +3.3V, V_REF = +3V, GND = 0V.
17. FV = 25V
18. FV = +10V. Bypass mode. Isource = Isink = 0. External PMU = 0V.
19. Tested at (VCC + VEE)/2.
20. Tested at VCC, VEE.
21. Tested at VCC – 1V, VEE + 1V.
22. Limits established by characterization and are not production tested.

TABLE 1. FV

RANGE	CAL POINTS	LIMITS	FV TEST POINTS
VR0 IR3	0V/0µA +3V/0µA	TPFV0 TPFV0 TPFV0	–.5V/0µA +1.5V/0µA +3.5V/0µA
VR1 IR3	0V/0µA +5V/0µA	TPFV1 TPFV1 TPFV1	–1V/0µA +3V/0µA +7V/0µA
VR2 IR3	0V/0µA +10V/0µA	TPFV2 TPFV2 TPFV2	–2V/0µA +6V/0µA +14V/0µA
VR3 IR0 – IR3	0V/0µA +20V/0µA	TPFV3A TPFV3A TPFV3A TPFV3A TPFV3A	+12.5V/–Imax +12.5V/–50% Imax +12.5V/0µA +12.5V/+50% Imax +12.5V/+Imax
VR3 IR4	0V/0µA +20V/0µA	TPFV3B TPFV3B TPFV3B TPFV3A TPFV3A TPFV3B	–2V/–3mA –1.5V/–5mA 0V/–12mA +12.5V/–10mA +12.5V/+10mA +25V/+10mA

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DC Electrical Specifications - Measure Current

VCC = +28.9V, VEE = -3.9V, VDD = +3.25V, V_REF = +3V, GND = 0V.

Channel Configuration:

1. Feedback# = DOUT_#
2. Isource-#/Isink-# = 15.6mA
3. Mon-Scale# = 1.0V, Mon-shift# = 0V

The sequence of events performed for MI testing is:

1. Program VF#
2. Force current at DOUT_#
3. Measure the voltage at MON_#.

FI Tests:

1. MI tested in VR3, IR0 – IR4
2. MI uses 2-Pt software cal

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MI (Post Calibration)						
14100	Measure Current Error	IR0, MI test points, TPMI (Note 24, Table 2)	–24		+24	nA
14101	Measure Current Error	IR1, MI test points, TPMI (Note 24, Table 2)	–240		+240	nA
14102	Measure Current Error	IR2, MI test points, TPMI (Note 24, Table 2)	–2.4		+2.4	µA
14103	Measure Current Error	IR3, MI test points,TPMI (Note 24, Table 2)	–8		+8	µA
14104	Measure Current Error	IR4, MI test points, TPMI (Note 24, Table 2)	–80		+80	µA
14104	Measure Current Error	IR4, MI test points,TPMI-B(Note 24, Table 2)	–200		+200	µA
	MI Temperature Coefficient	IR0, Note 23		<0.02		%Imax/°C
	MI Temperature Coefficient	IR1, Note 23		<0.02		%Imax/°C
	MI Temperature Coefficient	IR2, Note 23		<0.01		%Imax/°C
	MI Temperature Coefficient	IR3, Note 23		<0.01		%Imax/°C
	MI Temperature Coefficient	IR4, Note 23		<0.01		%Imax/°C

NOTES:

23. Limits established by characterization and are not production tested.
24. 4-point software calibration for MI CMRR

TABLE 2.

RANGE	CAL POINTS	TPMI	TPMI-B
IR0 – IR3	+12.5V/.8 • Imax +12.5V/–.8 • Imax	+12.5V/–Imax +12.5V/–50% Imax +12.5V/0µA +12.5V/+50% Imax +12.5V/+Imax	
IR4	+12.5V/+10mA +12.5V/–10mA	+12.5V/–10mA +12.5V/0mA +12.5V/+10mA	–2V/–3mA –1.5V/–5mA 0V/–12mA +25V/+10mA

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DC Electrical Specifications - Measure Voltage (Per Channel Monitor)

VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, GND = 0V.

The sequence of events performed for testing the MONITOR is:

1. Program FV to the desired voltage (in VR3 IR4, Iload = 0
2. Measure the voltage at DOUT_#
3. Mon-Scale#=1, Mon-Shift#=0V
4. Measure the voltage at MONITOR
5. Calculate the difference to determine the error.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MON_#, MON_REF_#						
19112	MON_# Output Impedance	Tested at +5V, Iout = 0mA/+4mA and 0mA/–4mA		100	250	Ω
14721	MON_# Voltage Error		–5		+5	mV
14710	MON_# HiZ Leakage Current	Tested at VEE + 1V (VCC + VEE)/2, VCC – 1V	–20		+20	nA
	Short Circuit Output Current	Monitor @ +10V/0V. External PMU @ 0V/+10V, Note 25		15		mA
	MON_# Temperature Coefficient	DOUT# Input = 25V, Mon-Scale#=0.5, Mon-Shift#=0V, Note 25		<200		µV/°C
	MONITOR, MON_# Capacitance	Note 25		5		pF

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NOTES:

25. Limits established by characterization and are not production tested.

TABLE 3.

MV TESTING	MV CAL POINTS	MV TEST POINTS
IR4	0V/0µA +20V/0µA	–2.5V/0µA +12V/0µA +27V/0µA

DC Electrical Characteristics- Active Load

Channel Configuration:

1. Feedback# = Tight
2. Load-BP# = 0
3. IR4
4. Tester PMU configured in FV/MI Mode

LEVEL	FV	TESTER PMU
SRC	12.5V	9.5V
SNK	12.5V	15.5V

The sequence of events performed for SRC/SNK Testing is:

1. Program FV#
2. Set Tester PMU voltage
3. Measure the current using Tester PMU

TABLE 4. SRC/SNK Test Points

CAL POINTS	TEST POINTS
5.2mA/13.0mA	2.6mA, 5.2mA, 7.8mA, 10.4mA, 13.0mA, 15.6mA

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source and Sink Currents						
	Post-Cal Error	Note 26		1.5		mA
Tempco						
	Source Temperature Coefficient	Notes 27, 28		2		µA/°C
	Sink Temperature Coefficient	Notes 27, 28		8		µA/°C
IL_Adjust						
12000	IL-Adjust#<2:0> = 001	Note 26		0.9 • Nominal	0.94 • Nominal	mA
12001	IL-Adjust#<2:0> = 010	Note 26	1.06 • Nominal	1.1 • Nominal		mA
12002	IL-Adjust#<2:0> = 101	Note 26		0.8 • Nominal	0.86 • Nominal	mA
12003	IL-Adjust#<2:0> = 110	Note 26	1.14 • Nominal	1.2 • Nominal		mA

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NOTES:

26. VCC = +28.9V, VEE = –3.9V, VDD = +3.25V, V_REF = 3V, DUT_GND = 0V.
27. VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, DUT_GND = 0V
28. Limits established by characterization and are not production tested.

DC Electrical Specifications - Resistance Values

VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sense Resistors						
19000	IR0			250		kΩ
19010	IR1			25		kΩ
19020	IR2			2.5		kΩ
19030	IR3			250		Ω
19040	IR4			25		Ω
On-Chip FET Switches						
19109	Load-BP#			30		Ω
19102	Tj Connect Switch			180		Ω
19111	Con-D-ES#			1200		Ω
19110	Con-D-EF#			150		Ω
19104	Con-MI0#			650		Ω
19105	Con-MI1#			650		Ω
19106	Con-MI2#			300		Ω
19107	Con-MI3#			65		Ω
19108	Con-MI4#			15		Ω

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DC Electrical Specifications - Central Monitor

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MONITOR, MON_REF						
14710	MONITOR HiZ Leakage Current	Tested at MONITOR = VCC, (VCC+VEE)/2, VEE; Note 33	–20	0	+20	nA
19100	MONITOR Output Impedance	Tested @ +5V, Iout = 0µA/ +100µA and 0µA/–100µA/ Note 34		150	300	Ω
14720	MONITOR Voltage Error	Note 35	–5		+5	mV
	Short Circuit Current	Monitor = +10V/0V. External PMU = 0V/+10V; Notes 34 and 36		15		mA
	Monitor Temperature Coefficient	Notes 33 and 35		<+50		µV/°C
14715	MON_REF Hi-Z Leakage	Tested @ MON_REF = –2.5V, 0V, +4.5V; Note 33	–20		+20	nA
19101	MON_REF Output Impedance	Tested @ 0V; 0mA/+4mA; 0mA/–4mA; Note 34		200	350	Ω

NOTES:

29. VCC = +29V, VEE = –4V, VDD = +3.45V, V_REF = +3V, DUT_GND = 0V
30. VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, DUT_GND = 0V
31. VCC = +28.9V, VEE = –3.9V, VDD = +3.25V, V_REF = +3V, DUT_GND = 0V
32. Limits established by characterization and are not production tested.

DC Electrical Specifications - Per Channel Monitor Scaling

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Monitor Scaling DAC						
16730	Error @ Mon-Scale#<2:0> = 000	Notes 37 and 38	–100		+100	mV
16730	Error @ Mon-Scale#<2:0> = 001	Notes 37 and 38	–50		+50	mV
16730	Error @ Mon-Scale#<2:0> = 010	Notes 37 and 38	–50		+50	mV
16730	Error @ Mon-Scale#<2:0> = 011	Notes 37 and 38	–10		+10	mV
16730	Error @ Mon-Scale#<2:0> = 100	Notes 37 and 38	–10		+10	mV
16730	Error @ Mon-Scale#<2:0> = 101	Notes 37 and 38	–10		+10	mV
16730	Error @ Mon-Scale#<2:0> = 110	Notes 37 and 38	–10		+10	mV
16730	Error @ Mon-Scale#<2:0> = 111	Notes 37 and 38	–10		+10	mV
Monitor Shiftng DAC						
16600	Linearity Error	Notes 30 and 40	–50		+50	mV
16610	Offset	Notes 30 and 40	–250		+250	mV
16620	Gain	Notes 30 and 40	0.49	0.50	0.51	mV/Code

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NOTES:

33. VCC = +28.9V, VEE = –3.9V, VDD = +3.25V, V_REF = +3V, DUT_GND = 0V
34. 2-point calibration by forcing DOUT_# to 0V/+16V. Error vs. theoretical gain relative to Mon-Scale# = 1.0 (Code 100). FV mode, VR1, FV = +1V. Mon-Shift# = 0V.
35. VCC = +16V, VEE = –16V, VDD = +3.3V, V_REF = +3V, DUT_GND = 0V
36. 16 codes tested relative to a line dtermined by the 2/16 and 13/16 measurement point. FV mode, FR1, DAC Code = 7FFF. Mon-Scale# = 0.

AC Characteristics

For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications - CPU Port

VCC = +28.9V, VEE = –3.9V, VDD = +3.25V, V_REF = +3V, GND = 0V.
Limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Set-Up Time						
27100	SDIO to rising CK		10			ns
27110	STB to rising CK		10			ns
Hold Time						
27120	SDIO to rising CK		10			ns
27130	STB to rising CK		10			ns
27140	CK Minimum Pulse Width High		18			ns
27150	CK Minimum Pulse Width Low		15			ns
27160	CK Period		40		100	ns
Propagation Delay						
27180	Rising CK to SDIO Out				12	ns
27170	Reset Minimum Pulse Width		100			ns

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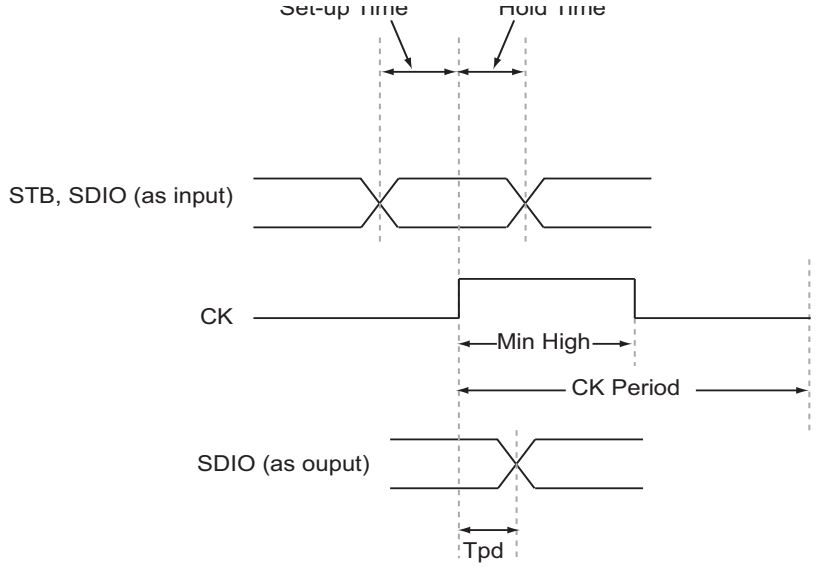

FIGURE 2. AC SPECS CPU PORT

AC Electrical Specifications - PPMU

VCC = +29V, VEE = –4V, VDD = +3.3V, V_REF = +3V, GND = 0V.
Limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV Settling Time						
	IR0	Note 1		1500		µs
	IR1	Note 1		180		µs
	IR2	Note 1		80		µs
	IR3	Note 1		80		µs
	IR4	Note 1		80		µs
	IR4	Note 2		20		µs
MV Settling Time						
		Note 3		0.6		µs
		Note 4		2		µs

NOTES:

1. VR3, FV = 0V to 25V swing. Cload = 1nF, all IR, Isource#/Isink# = Max Code, Sel-FB = DOUT.
2. VR3, FV = 0V to 1V swing. Cload = 1nF, IR4, Isource#/Isink# = MaxCode, Sel-FB = DOUT.
3. PMU in HiZ. External PulseGen = 0V to 1V swing. Mon-Scale# = 1.0, Mon-Shift# = 0V.
4. PMU in HiZ. External PulseGen = 0V to 10V swing. Mon-Scale# = 1.0, Mon-Shift# = 0V.

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Chip Overview

ISL55185 is a highly integrated System-on-a-Chip pin electronics solution incorporating 8 independent channels of:

- PMU
- Active Load
- External Force/External Sense

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.

CPU Control

All configuration set up as well as the writing to and reading back of the internal registers are controlled through the 3 bit serial data CPU port. The CPU port is typically used to set up the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the datasheet, lists all programmable control signals and their addresses. This chart shows how to program each internal signal.

Real Time Control

Real time control is accomplished via the DATA_#,EN_#, EXT_MON_OE and EXT_MON_SEL pins. Real time observation is accomplished via the per channel monitor pins MON_# and MON_REF#, as well as the central MONITOR and MON_REF.

Analog References

All on-chip analog levels are related to off-chip precision voltage and resistance references:

- V_REF
- R_EXT

These external references are used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, part to part, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the datasheet or in any circuit diagram, use the following naming conventions:

1. all capital letters (i.e. MON_0, CK, SDIO)
2. underscores for clarity (i.e. DOUT_0)
3. shown next to an I/O circle in any schematic.

CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

1. the first letter in a word is always a capital letter
2. subsequent letters within the same word are small
3. dashes (but never an underscore) for clarity
4. NOT shown with an I/O circle in any schematic.

Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.

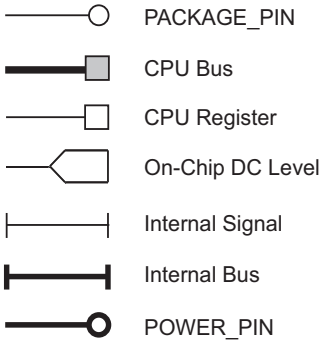

FIGURE 3. CPU NOMENCLATURE

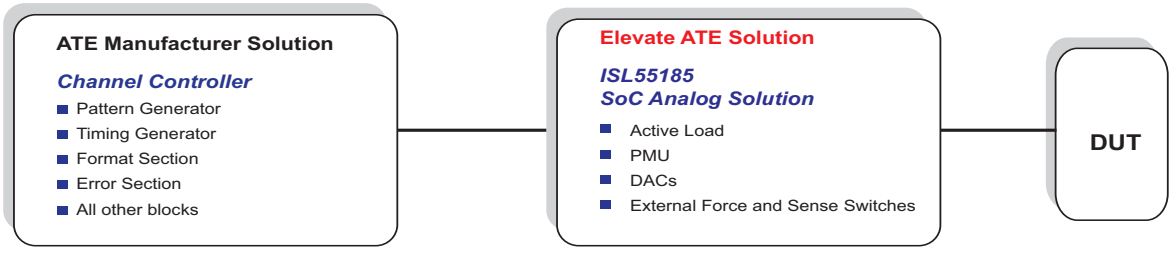

FIGURE 4. Elevate Semiconductor ATE SOLUTION

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Block Diagrams

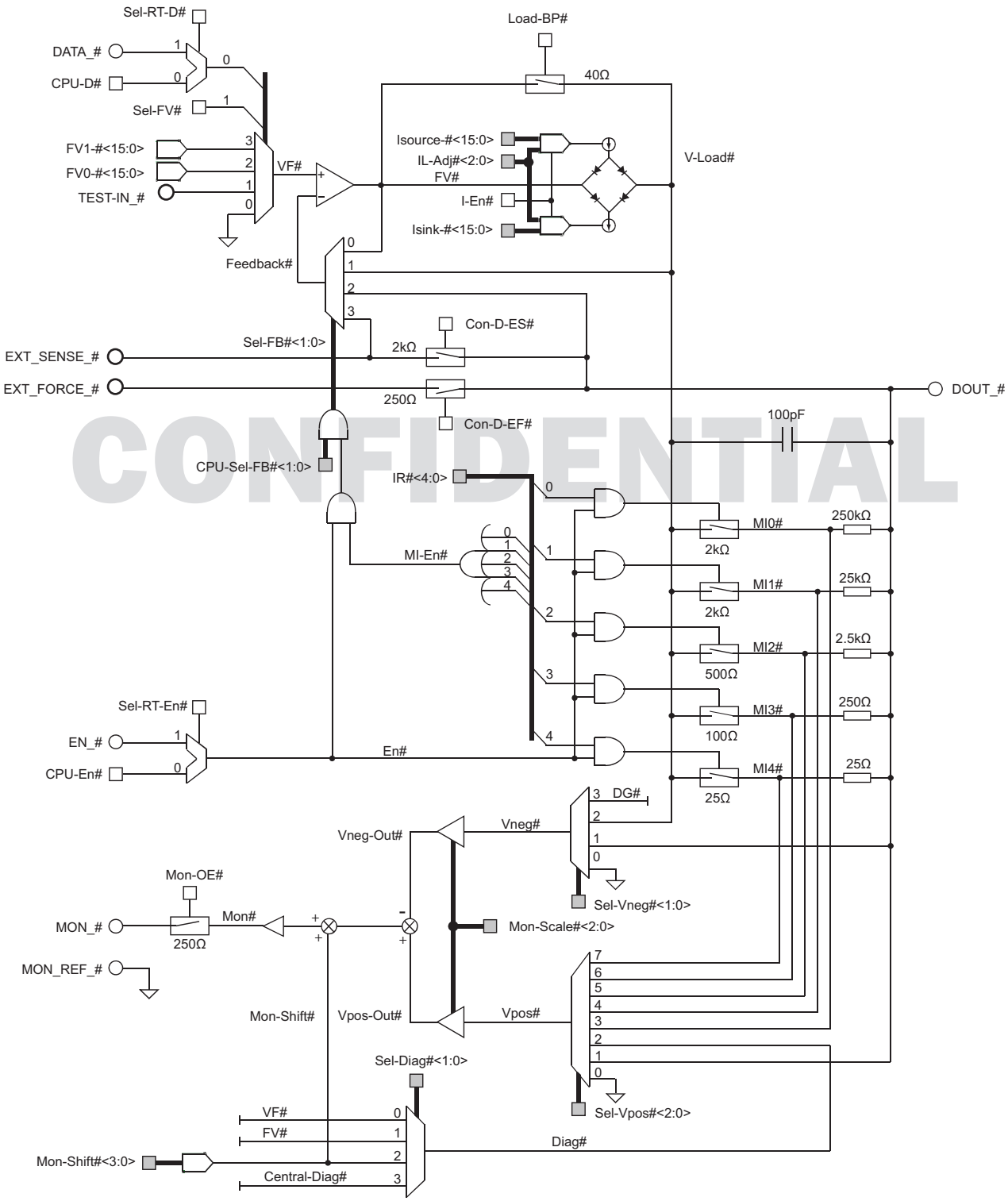

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FIGURE 5. PER CHANNEL DIAGRAM

Block Diagrams (Continued)

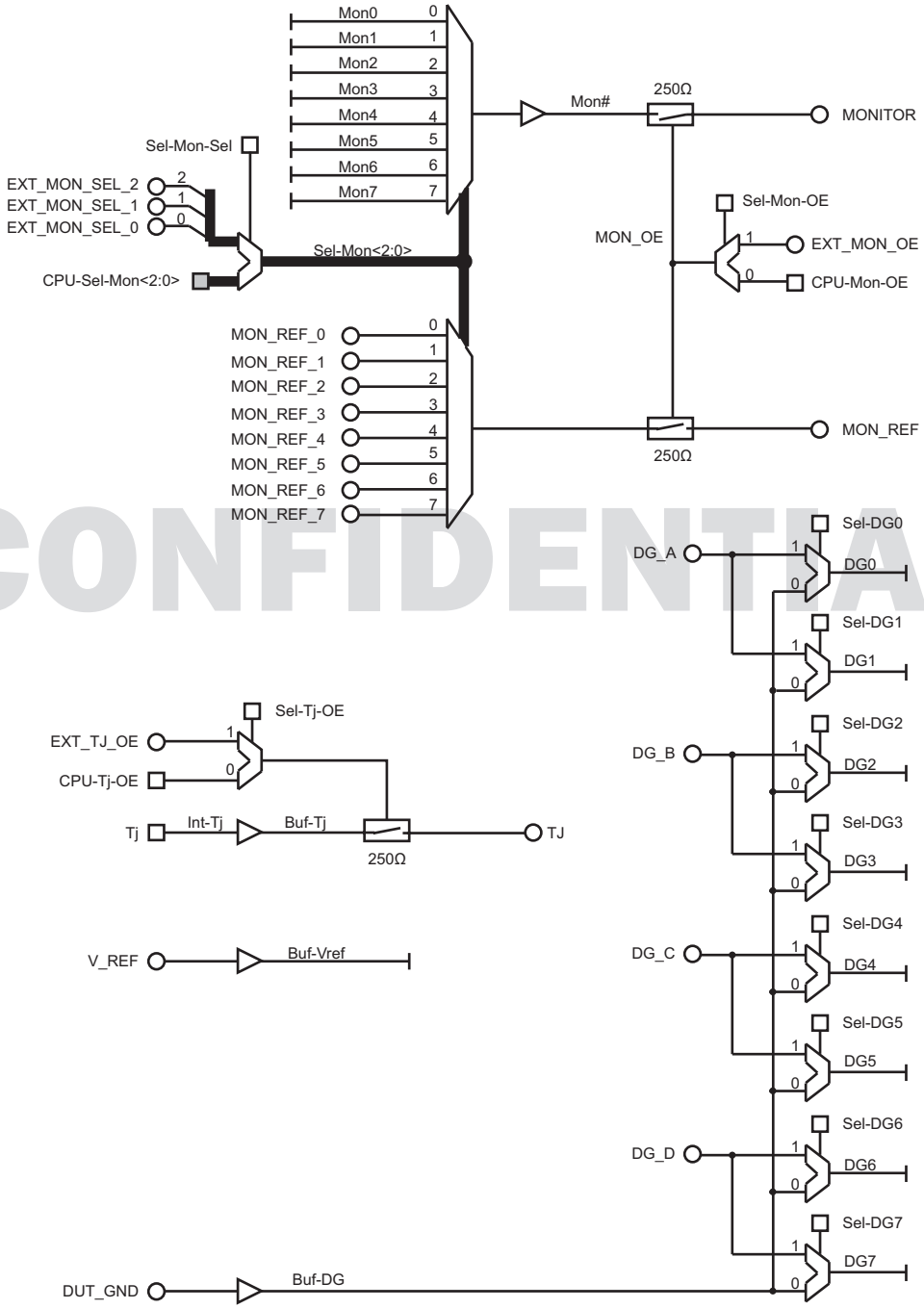

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FIGURE 6. CENTRAL RESOURCES

Overview

Each channel has an independent PMU with the ability to:

- Force Voltage
- Measure Current
- Measure Voltage.

FV

There are two static levels capable of providing the forcing voltage. The selection between these levels may be under CPU or external real time control.

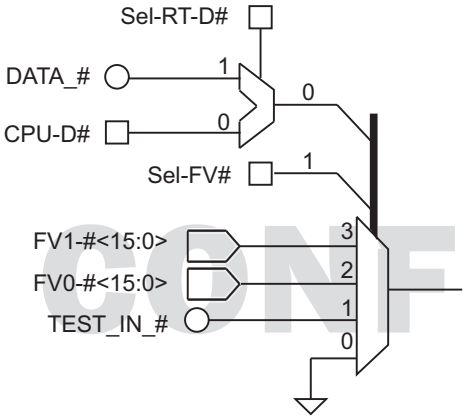

FIGURE 7.

TABLE 5.

SEL-RT-D#	Sel-FV#	CPU-D#	DATA_#	VF_#
0	0	0	X	GND
0	0	1	X	TEST_IN
0	1	0	X	FV0-#
0	1	1	X	FV1-#
1	0	X	0	GND
1	0	X	1	TEST_IN
1	1	X	0	FV0-#
1	1	X	1	FV1-#

Feedback Options

Several nodes may be selected for the feedback voltage to the forcing op amp.

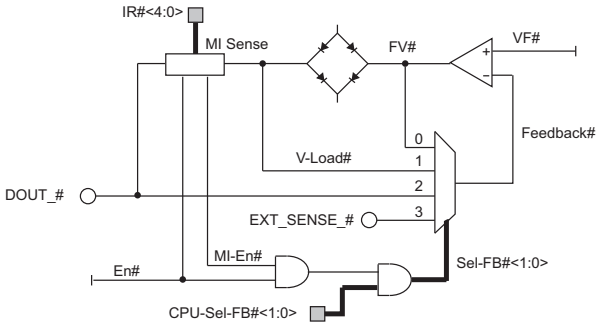

FIGURE 8. FEEDBACK OPTIONS

TABLE 6.

SEL-FB#<1:0>	FEEDBACK#
00	FV#
01	V-Load#
10	DOUT_#
11	EXT_SENSE#

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However, if the part is placed into a HiZ state, the forcing op will automatically go into a tight loop configuration to guarantee that the op amp does not go open loop.

TABLE 7.

EN#	MI_EN#	SEL-FB#<1:0>
0	X	00
X	0	00
1	1	CPU-Sel-FB#<1:0>

The default condition upon power-up and reset is:

- HiZ
- tight loop configuration

Current Clamps

The independent source and sink load currents act as a current limit on the PMU in when forcing a voltage and the bypass switch open.

MI

When measuring current the CPU port may select the desired current range. Each range may be independently activated or disabled allowing for a wide variety of make/break combinations when changing modes and current ranges.

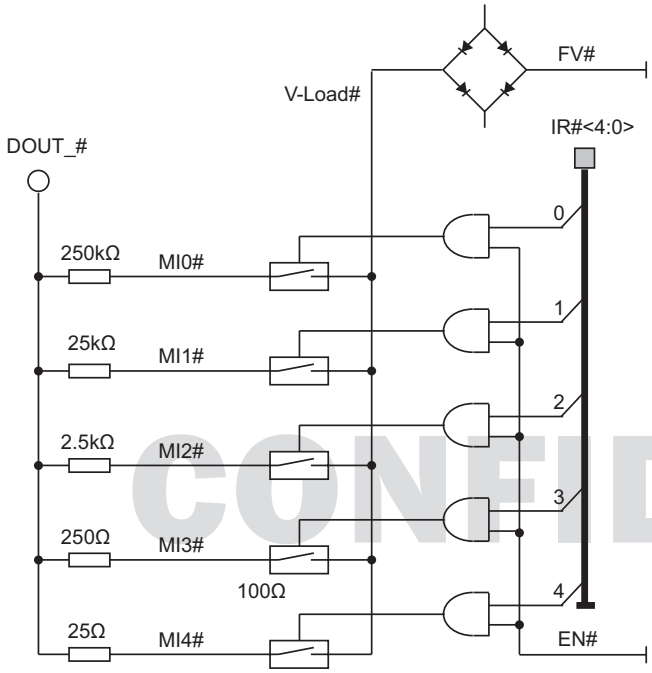

FIGURE 9. MEASURING CURRENT (I)

TABLE 8.

I RANGE	IR#<4:0>	IMAX	RSENSE
N/A	00000	MI in HiZ	N/A
IR0	00001	4µA	250kΩ
IR1	00010	40µA	25kΩ
IR2	00100	400µA	2.5kΩ
IR3	01000	4mA	250Ω
IR4	10000	24mA	25Ω

The Imax of a current range is defined at the current that creates a 1V drop across the sense resistors. There is no hard limit within the part in that currents that exceed Imax will simply continue to generate a larger sense voltage. IR4 supports an Imax of 24mA even though a 1V drop across the sense resistor corresponds to 40mA.

Measurement Unit

The per-channel measurement unit has the ability to measure either voltage or current. A positive and negative input to the instrumentation amplifier is selected by the CPU port. These inputs are then combined, scaled, shifted and buffered before driving the per-channel differential monitor.

TABLE 9.

SEL-VNEG#<1:0>	VNEG#
00	GND
01	DOUT_#
10	V-Load#
11	Buf-DG
SEL-VPOS#<2:0>	**VPOS#**
000	GND
001	DOUT_#
010	Diag#
011	MI0#
100	MI1#
101	MI2#
110	M13#
111	M14#

Measurement Unit Configuration

The selection of the two inputs to the instrumentation amplifier determines the mode of the PMU and what parameter is being measured.

TABLE 10.

VPOS#	VNEG#	MODE	IRANGE
DOUT_#	DUT_GND	MV	X
MI0#	DOUT_#	MI	VIR0
MI1#	DOUT_#	MI	VIR1
MI2#	DOUT_#	MI	VIR2
MI3#	DOUT_#	MI	VIR3
MI4#	DOUT_#	MI	VIR4

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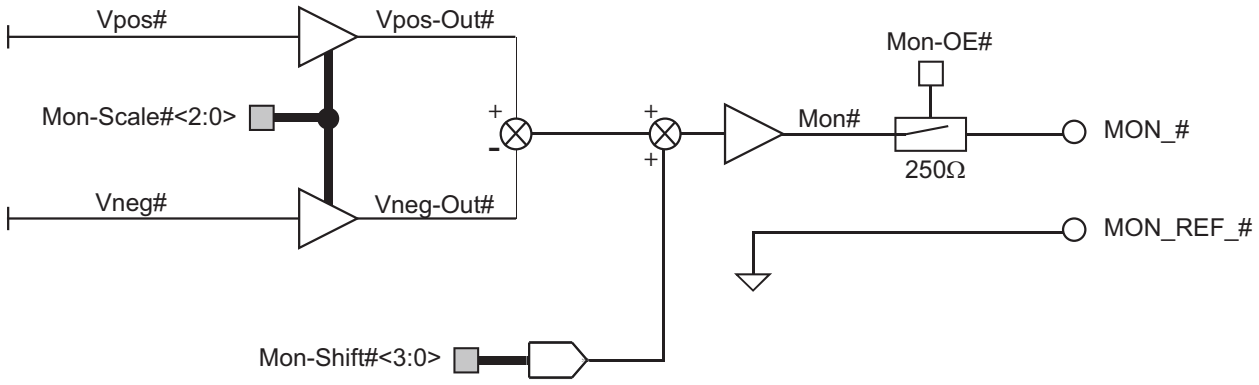

FIGURE 10. SCALING AND SHIFTING

Scaling and Shifting

Once the differential inputs are selected, they are combined, scaled and shifted before driving an output buffer.

MON_# = ((Vpos# - Vneg#) o Mon-Scale#) + Mon-shift#

MON_REF# = GND

SCALING

The CPU port selects the voltage gain of the instrumentation amplifier.

TABLE 11.

MON-SCALE#<2:0>	SCALE FACTOR
000	0.0625 (1/16)
001	0.125 (1/8)
010	0.25 (1/4)
011	0.5 (1/2)
100	1.0
101	2.0
110	4.0
111	8.0

SHIFTING

Once gained up or down, the CPU can then shift the resulting signal more positive or more negative using the Mon-Shift# DAC.

TABLE 12.

MON-SHIFT#<3:0>	MON-SHIFT#
0000	–5V
0001	–4.5
•	•
1010	0V
•	•
1110	+2V
1111	+2.5V

Scaling and shifting allows a wide variety of measurements to connect directly with an off-chip ADC without requiring any external circuitry. In addition, the output signal may be optimized to use the entire ADC input range in order to maximize the DC accuracy of the measurement.

To prevent damage to the ADC in cases where the monitor voltage exceeds the input compliance of the ADC, the monitor output current is limited at ~15mA.

Output High Impedance

The per-channel monitor output may be placed in a HiZ state by the CPU port.

TABLE 13.

MONOE#	MON_# OUTPUT STATE
0	HiZ
1	Active

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Active Load

Overview

Each channel supports an independent active load with the following characteristics:

- MI capability
- Independent source and sink currents
- 2 independent commutating voltages
- HiZ capability.

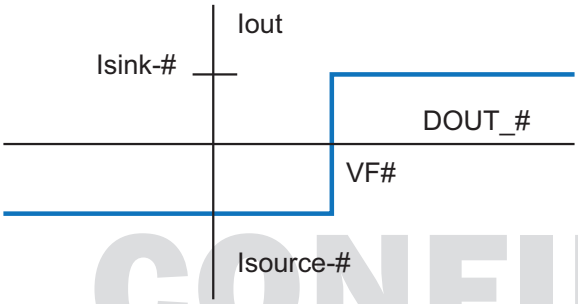

FIGURE 11. ACTIVE LOAD OVERVIEW

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Source/Sink Currents

The source and sink currents are established by independent on-chip 16-bit DACs.

The source and sink currents can be adjusted slightly upward or downward.

TABLE 14.

ISOURCE-#<15:0> ISINK-#<15:0>	ISOURCE ISINK	RESOLUTION
0000	0mA	
FFFF	26mA	397nA

TABLE 15.

IL_ADJ#<2:0>	IMAX
000	Nominal
001	0.9 • Nominal
010	1.1 • Nominal
011	Reserved
100	Reserved
101	0.8 • Nominal
110	1.2 • Nominal
111	Reserved

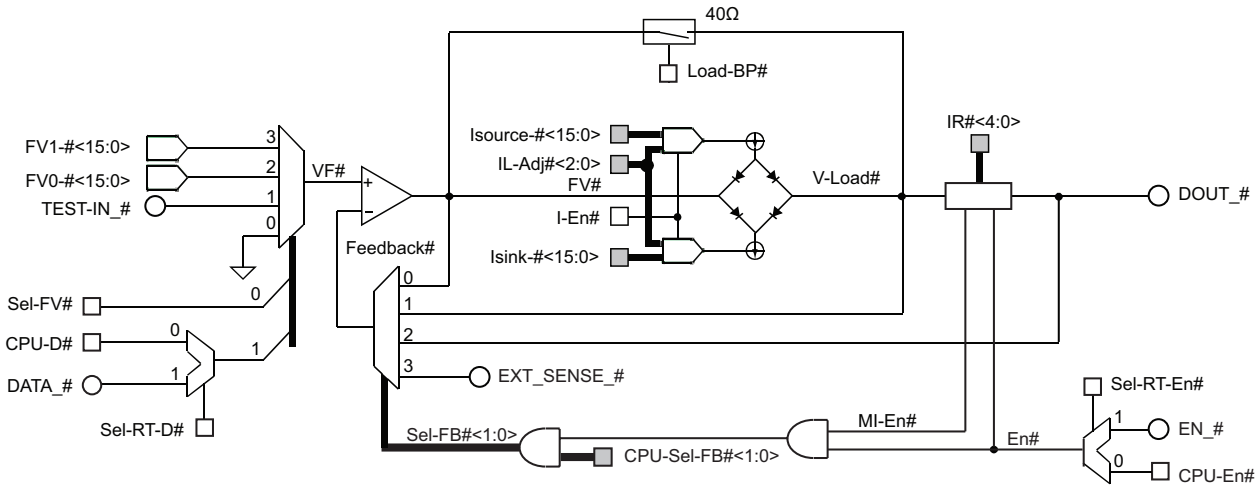

FIGURE 12.

Load Current Enable

The CPU port can override the programmed values of the source and sink currents and set them to 0. The default state upon power up is "disabled", or 0 current flow.

TABLE 16.

I-EN#	SOURCE CURRENT	SINK CURRENT
0	0	0
1	I-Source#<15:0>	I-Sink#<15:0>

HiZ

The active load may be placed into a HiZ condition where it supports extremely low leakage currents as long as the output pin is within the positive and negative analog supply rails.

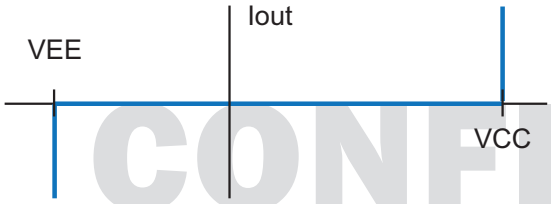

FIGURE 13. ACTIVE LOAD HIZ

HiZ may be controlled by the CPU port or the real time input EN_#.

TABLE 17.

SEL-RT-EN#	CPU-En#	EN_#	LOAD @ DOUT_#
0	0	X	HiZ
0	1	X	Active
1	X	0	HiZ
1	X	1	Active

Commutating Voltage

There are two independent on-chip commutating voltage that may be selected by either the CPU port or an external real-time input.

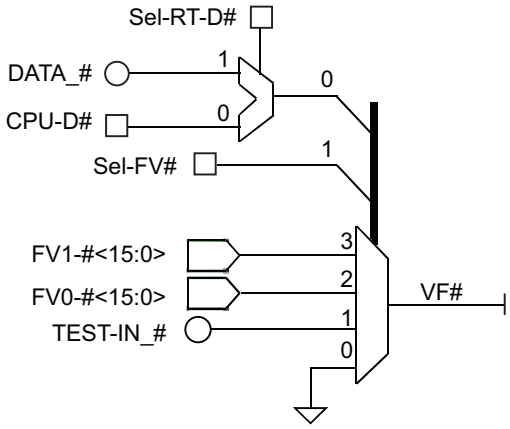

FIGURE 14. COMMUTATING VOLTAGE

TABLE 18.

SEL-RT-D#	SEL-FV#	CPU-D#	DATA_#	VF_#
0	0	0	X	GND
0	0	1	X	TEST-IN
0	1	0	X	FV0-#
0	1	1	X	FV1-#
1	0	X	0	GND
1	0	X	1	TEST_IN
1	1	X	0	FV0-#
1	1	X	1	FV1-#

Load Configuration

For normal active load operation the following conditions should be established:

1. tight loop configuration (CPU-Sel-FB#<1:0> = 00)
2. select the desired current range (typically IR4).

Resistive Load

With the bridge bypassed and the source and sink currents programmed to 0mA, the load is configured as a resistive load.

The voltage of the resistive load is the input voltage to the forcing op amp. The resistance is the series resistance of the MI sense resistor, the on resistance of the MI switch and the on resistance of the bypass switch.

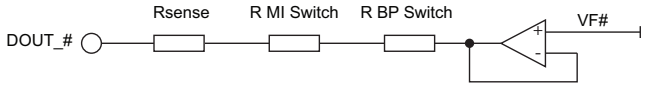

FIGURE 15. RESISTIVE LOAD

Load Bypass

The diode bridge of the active load may be bypassed by a transmission gate.

In bypass mode, current flow is limited to ~32mA. This limit is not programmable nor may it be disabled.

TABLE 19.

LOAD-BP#	FV# to V-LOAD#
0	Bridge not bypassed
1	Bridge bypassed

Hybrid Mode

With the bypass switch connected and the source and sink currents programmed to a non-zero value the load continues to act like an active load except that the source and sink currents no longer act as current limits. Additional current may flow from the forcing op amp through the bypass switch.

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Diagnostics

Each channel has a diagnostic mux that provides access to internal nodes that may be brought out on each channel's monitor.

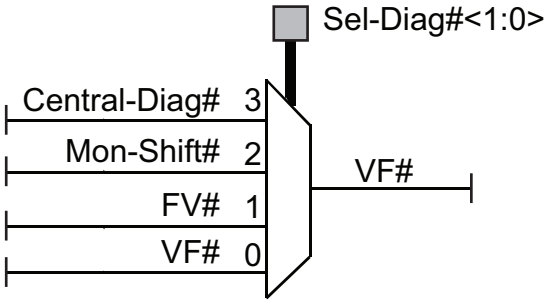

FIGURE 16.

TABLE 20.

SEL-DIAG#<1:0>	DIAG#
00	VF#
01	FV#
10	Mon-Shift#
11	Central-Diag#

Each channel has one diagnostic input reserved for a central resource, and each channel has a resource level as its input.

TABLE 21.

CHANNEL #	CENTRAL-DIAG#
0	Buf-Tj
1	GND
2	Buf-DG
3	Buf-Vref
4	DAC-P
5	DAC-N
6	DAC Test Node 0
7	DAC Test Node1

External Force and Sense

An independent external force and sense path exists for each channel.

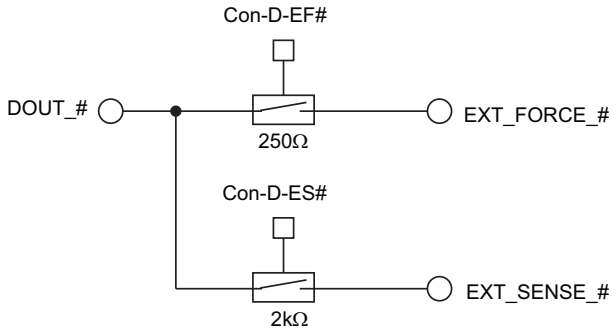

FIGURE 17.

TABLE 22.

Con-D-EF#	DOUT_# to EXT_FORCE_#
0	Disconnected
1	Connected

Con-D-ES#	DOUT_# to EXT_SENSE_#
0	Disconnected
1	Connected

These paths are useful to bypass the PPMU completely and provide direct access to the DUT, which is useful for:

1. Connecting an external PMU to the DUT
2. Direct measurement of the DUT voltage
3. DC calibration.

Central Resources

Central Monitor

There is a central differential monitor that can select any one channel's monitor as its input.

TABLE 23.

SEL-MON<2:0>	MONITOR	MON_REF
#	MON_#	MON_REF#

This selection can be made by the CPU port or by external real-time control.

TABLE 24.

SEL-MON-SEL	SEL-MON<2:0>
0	CPU-Sel-Mon<2:0>
1	EXT_MON_SEL_<2:0>

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HiZ

The central monitor may be placed into a HiZ condition where it supports extremely low leakage currents as long as the output pin is within the positive and negative analog supply rails. HiZ is useful when ganging multiple central monitors across multiple chips together and connecting the outputs to one external ADC.

TABLE 25.

SEL-MON-OE	CPU-MON-OE	EXT_MON_OE	MONITOR
0	0	X	HiZ
0	1	X	Active
1	X	0	HiZ
1	X	1	Active

Monitor Output Current Limiting

The central monitor output is designed to mate directly with an external ADC. To prevent damage to the ADC in cases where the monitor voltage exceeds the input compliance of the ADC, the monitor output current is limited to ~15mA.

Junction Temp Measurement

Temperature Monitor

TJ is an analog voltage output that tracks the junction temperature. TJ may be placed in a high impedance state by either an external pin or by the CPU port.

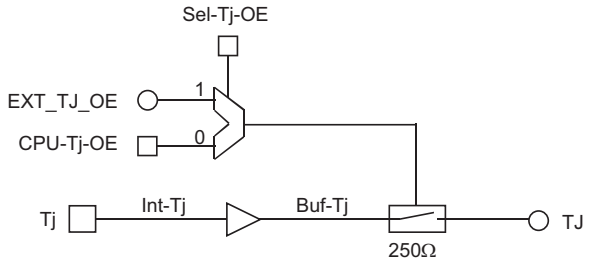

FIGURE 18.

TABLE 26.

Sel-Tj-OE	CPU-Tj-OE	EXT_TJ_OE	TJ
0	0	X	HiZ
0	1	X	V-Temp
1	X	0	HiZ
1	X	1	V-Temp

Equation 1 is used to calculate the junction temperature based on the TJ voltage.

$$T_J(°C) = [T_J(V) \bullet 118] - 113 \quad \text{(EQ. 1)}$$

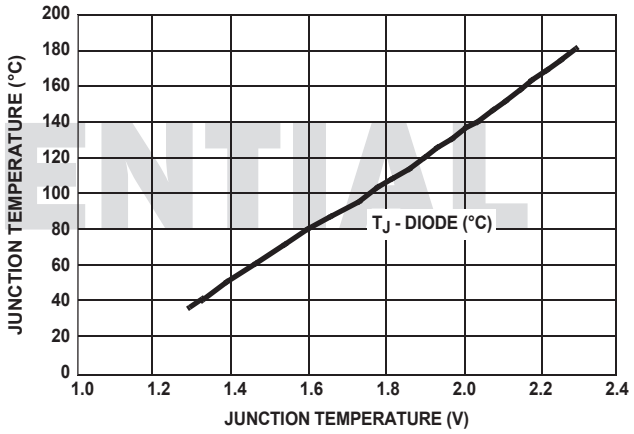

FIGURE 19. THERMAL TRANSFER FUNCTION

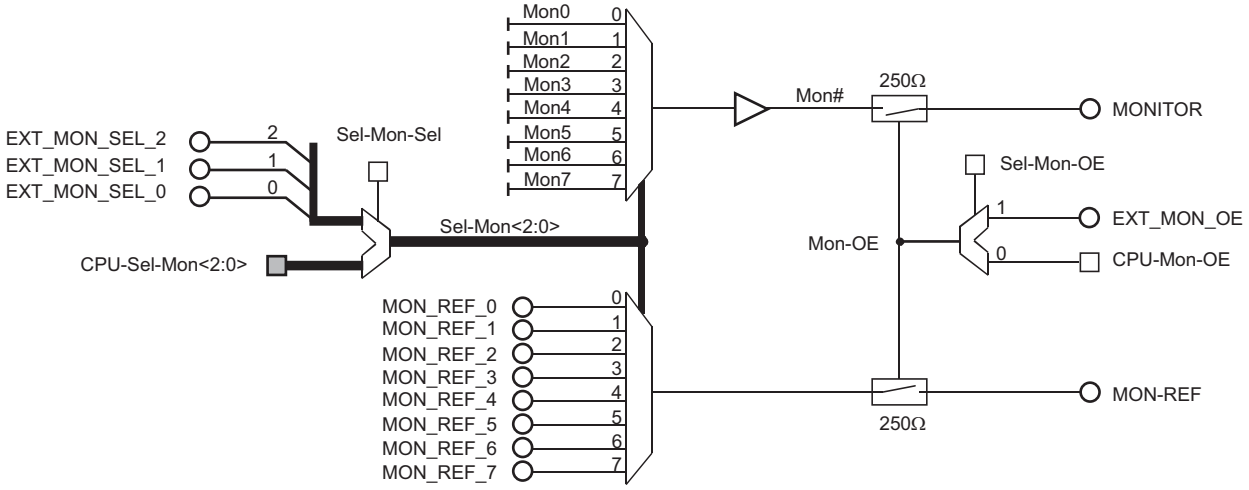

FIGURE 20. CENTRAL MONITOR

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Thermal Diode

A separate thermal diode allows an off-chip temperature sensor to perform continuous real time junction temperature tracking. This diode may be used with all chip power supplies turned off.

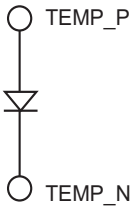

FIGURE 21. THERMAL DIODE

Required Off-Chip Components

A precision reference level is required per chip. However, there may be a need for decoupling capacitors on the power supply pins. The need for decoupling capacitors is dependent upon the particular application, and is therefore system dependent.

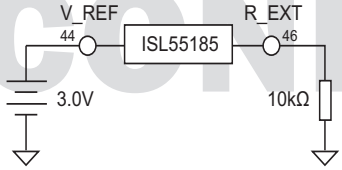

FIGURE 22.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VCC ≥ VDD ≥ VREF ≥ GND
2. VEE ≤ GND

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation.

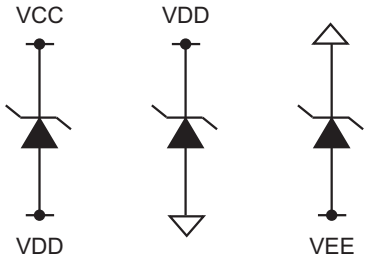

FIGURE 23. POWER SUPPLY SEQUENCE

Power Supply/Analog Voltage Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VCC
3. VDD
4. V_REF

DC Levels

All required DC levels are generated on-chip with a 16-bit DAC that is programmed through the CPU port.

Voltage Level Programming

The CPU port may select 1 of several voltage range options.

The realizable voltage range is restricted by the power supply levels and headroom limitations. If a level is programmed beyond the power supply rails, saturation will occur and the actual DC level will not match the desired programmed level.

TABLE 27.

V-RANGE-SEL#<1:0>	VOLTAGE RANGE	OUTPUT VOLTAGE SWING (FS)	RESOLUTION (LSB)
0	VR0	4V	61µV
1	VR1	8V	122µV
2	VR2	16V	244µV
3	VR3	32V	488µV

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Offset and Gain

Each individual DC level has independent offset and gain correction. These correction values allow the desired output level to be loaded simultaneously across multiple pins without having to correct for per pin errors.

TABLE 28.

OFFSET CODE	OFFSET VALUE	GAIN CODE	GAIN VALUE
0000H	-5.4% of FS	0000H	0.875
7FFFH	0	7FFFH	1.0
FFFFH	+5.4% of FS	FFFFH	1.125

Device Under Test Ground

The actual ground reference level at the DUT may be different than that used by the DAC reference. DUT_GND is a high impedance analog voltage input that provides a means of tracking the destination ground, and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT. DUT_GND is super imposed upon all channels.

The input at DUT_GND should be:

1. filtered for noise
2. stable
3. reflect the actual ground level at the DUT

DUT_GND is NOT added into the DC level when measuring a current by the PMU.

V_REF

V_REF is an analog input voltage that is used to program the on chip DC levels. Any noise or jitter on V_REF will contribute to the noise floor of the chip, and therefore V_REF should be as quiet and stable as possible.

There is one V_REF pin shared by all channels.

V_REF Sensitivity

The previous equations that predict the DAC output assume that V_REF = +3.0V. Any variation in V_REF at the input pin will affect the Level by a 1:1 ratio before being multiplied by the gain.

$$(Level = ProgrammedLevel) \bullet (1 - (V\_REF - 3.0)) \quad \text{(EQ. 2)}$$

Offset adjust has ample range to correct for deviations in V_REF, in addition to any offset requirements. As long as V_REF is held stable after calibration, deviation in V_REF from +3.0V will not affect DC accuracy.

Voltage Range Shifting

While the total output voltage range for each ranges select code is fixed, this range may be shifted more positive or more negative by using the Vmid DAC. Vmid is common for all channels on the chip. Vmid does not affect the DC levels that are used to generate currents.

TABLE 29.

VOLTAGE RANGE	VMID LSB	VMID<3:0>	VMID
VR0	125mV	0000 1111	+125mV +2.0V
VR1	250mV	0000 1111	+250mV +4.0V
VR2	500mV	0000 1111	+500mV +8.0V
VR3	1V	0000 1111	+1V +16V

Voltage Range Table

Several examples of different voltage ranges are shown in Table 30 below. For simplicity, in each example:

Gain Correction = 1.0

Offset Correction = 0.0V

DUT_GND = 0.0V.

Voltage Level Programming

Voltage ranges VR0, VR1, VR2 and VR3 use Equation 3:

$$(VOUT = (Value - Vmid)) \bullet Gain + Offset + Vmid + DUT\_GND \quad \text{(EQ. 3)}$$

Value is described by Equation 4:

$$Value = \left\{\frac{(DACCode)}{2^{(N-1)}}\right\} \bullet FS + Vmin \quad \text{(EQ. 4)}$$

where:

$N = 16; 2^{(N-1)} = 65,535$

and:

Vmin = Vmid - (FS/2).

Voltage Level Reference

All DC voltage levels are referenced to GND.

Current Level Programming

Current levels are programmed using Equations 5 through 9:

$$Imin = 0mA \quad \text{(EQ. 5)}$$

$$Imid = 13mA \quad \text{(EQ. 6)}$$

$$Imax = 26mA \quad \text{(EQ. 7)}$$

$$Idac = 26mA \bullet (DACCode)/(2^{(N-1)}) \quad \text{(EQ. 8)}$$

$$Isource/sink = (Idac - Imid) \bullet Gain + Imid + Offset \quad \text{(EQ. 9)}$$

TABLE 30. EXAMPLES OF Vmid CHANGING THE EFFECTIVE VOLTAGE OUTPUT RANGE

Range	FS	Vmid<3:0>	Vmid Value	DAC Code	Output Voltage	Comments
VR0	4	0000	+0.125V	0000 Hex, FFFF Hex	–1.875V, +2.125V	VR0 shifted – 1.375V
VR0	4	1011	+1.5V	0000 Hex, FFFF Hex	–0.5V, +3.5V	Nominal VR0
VR0	4	1111	+2V	0000 Hex, FFFF Hex	0V, 4V	VR0 shifted +0.5V
VR1	8	1011	+3V	0000 Hex, FFFF Hex	–1V, +7V	Nominal VR1
VR1	8	0011	+1V	0000 Hex, FFFF Hex	–3V, +5V	VR1 shifted –2V
VR1	8	1111	+4V	0000 Hex, FFFF Hex	0V, +8V	VR1 shifted +1V
VR2	16	1011	+6V	0000 Hex, FFFF Hex	–2.0V, +14V	Nominal VR2
VR2	16	1001	+5V	0000 Hex, FFFF Hex	–3V, +13V	VR2 shifted –1V
VR3	32	0000	+1V	0000 Hex, FFFF Hex	–15V, +17V	VR3 shifted down
VR3	32	1111	+16V	0000 Hex, FFFF Hex	0V, +32V	VR3 shifted up

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Voltage Range Options

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in Table 31.

TABLE 31. RANGE DECODE

FUNCTIONAL BLOCK	VR0	VR1	VR2	VR3	RANGE Select Bits <1:0>
PMU, Active Load FV0-#, FV1-#	√	√	√	√	V-Range-Sel#<1:0>
PMU Current Force Isource-#, Isink-#	VIR	VIR	VIR	VIR	N/A

Tracks DUT_GND

Does NOT Track DUT_GND

DC Calibration

The part is designed and tested to meet its DC accuracy specifications after a two-point calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. In general, most calibration points will be at 20% and 80% of the full-scale value for that range. (The actual calibration points are listed separately for each functional block in the DC specification section.)

The test points are broken into two categories:

1. inner test
2. outer test

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

In general, the inner test will be performed against tighter, more accurate limits. But every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration technique.

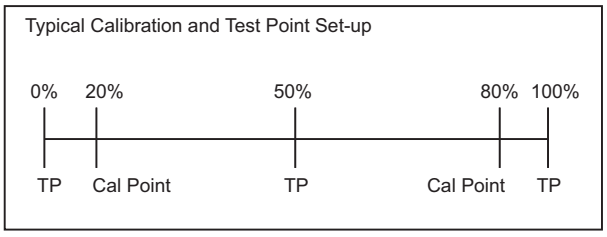

FIGURE 24.

System Level DC Accuracy Limits

Other calibration schemes and techniques, using more or fewer calibration points or different test points, may also be employed. The resulting system level accuracy may be superior or inferior to the part's specified limits, and will be dependent on the details of the particular application.

Calibration Procedure

1. Calibrate the MONITOR
2. Calibrate the DAC using the DAC cal bits
3. Calibrate the offset DAC
4. Calibrate the Gain DAC
5. Calibrate the DC Level

Level Calibration

INITIALIZE

- Select desired voltage range (VR0, VR1, VR2, VR3, VIR)
- Set Gain = 1.0; Offset = 0.0V

MEASURE

- Set Level 1 = Cal Point 1. Measure Output1'
- Set Level 2 = Cal Point 2. Measure Output2'

CALCULATE

- Gain' = (Output2' - Output1') / (Level 2 - Level1)
- Offset' = (Output2' - Vmid) - Gain' • (Level2 - Vmid)

FINISH

- Set Offset = - Offset' / Gain'
- Set Gain = 1.0 / Gain'

DAC Calibration

A 16-bit DAC is used to generate all of the required DC levels. To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction.

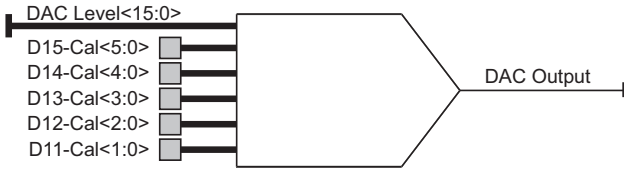

FIGURE 25. DAC CALIBRATION

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TABLE 32. D15 CALIBRATION

D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	D15 ADJUSTMENT
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	–3 LSB
			•			•
1	1	1	1	1	1	–93 LSB

TABLE 33. D14 CALIBRATION

D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	D14 Adjustment
1	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	–3 LSB
		•			•
1	1	1	1	1	–45 LSB

TABLE 34. D13 CALIBRATION

D13-Cal<3>	D13-Cal<2>	D13Cal<1>	D13-Cal<0>	D13 Adjustment
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	–3 LSB
	•			•
1	1	1	1	–21 LSB

TABLE 35. D12 CALIBRATION

D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	D12 Adjustment
0	1	1	+9 LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	–3 LSB
1	1	0	–6 LSB
1	1	1	–9 LSB

TABLE 36. D11 CALIBRATION

D11-Cal<1>	D11-Cal<0>	D11 Adjustment
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
0	1	–3 LSB

TABLE 37. CAL RANGE VS. VOLTAGE RANGE vs DAC BITS

	D15	D14	D13	D12	D11
VR0	5.67mV	2.74mV	1.28mV	549µV	183µV
VR1	11.3mV	5.49mV	2.55mV	1.1mV	366µV
VR2	22.6mV	11mV	5.1mV	2.19mV	732µV
VR3	45.3mV	21.9mV	10.2mV	4.38mV	1.46mV
VR4	30.6mV	43.8mV	20.4mV	8.76mV	2.92mV
VIR	14.2µA	6.87µA	3.2µA	1.37µA	458µA

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CPU Port

All on-chip DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip (typically used for diagnostic purposes.)

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low before another transaction may begin.

Clock Requirements

It is recommended that the CK be running at all times as it refreshes the DC levels throughout the chip. However, the CK may be stopped momentarily in order to make the chip quieter to support extremely accurate low noise measurements. The duration of these measurements should be short enough to minimize any droop on the levels.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached.

The registers in the WE group will be written to if WE = 1. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

WE is read back as a don't care (X) value.

Read vs Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 38.

1st SDIO Bit	CPU TRANSACTION TYPE
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

Unused data bits are read back as a don't care (X) state.

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs. The parallel write is a convenient way to save time when identical information needs to go to all channels.

TABLE 39. PARALLEL WRITE CONTROL

2nd SDIO Bit	CPU TRANSACTION TYPE
0	Data goes to the selected channel
1	Data goes to all channels

Reset

RESET is an external hardware reset signal that places all internal registers into a low state. Reset must be executed after a power up sequence. RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.

RESET is active high.

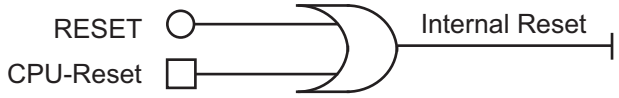

FIGURE 26.

In addition, the CPU port can execute a reset (as a write only transaction.) If the Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one-shot pulse that performs the same function as an external RESET.

Chip ID

Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

PRODUCT-ID<11:0>(D15:D4)	D3:D0
0C0 Hex (192)	Die-Rev<3:0>

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Address Space

Address Description

Information is stored on-chip in two ways:

1. RAM
2. Registers

Each storage mechanism is then broken into two categories:

1. Per-pin resources
2. Central resources

The address space is partitioned into several different segments to clearly mark the resource type and function.

TABLE 40. Address Space

Register Bit	Central Bit	Channel Address							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
Per Pin Resource RAM Storage																
0	0	0	0	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	Channel 0 DC Levels
0	0	0	0	0	0	0	0	0	0	1	A4	A3	A2	A1	A0	Channel 0 DC Level Offset Values
0	0	0	0	0	0	0	0	0	1	0	A4	A3	A2	A1	A0	Channel DC Level Gain Values
0	0	0	0	0	0	0	0	0	1	1	A4	A3	A2	A1	A0	Not Used
•	•				•				•	•			•			•
•	•				•				•	•			•			Channels 1 – 6
•	•				•				•	•			•			•
0	0	0	0	0	0	1	1	1	0	0	A4	A3	A2	A1	A0	Channel 7 DC Levels
0	0	0	0	0	0	1	1	1	0	1	A4	A3	A2	A1	A0	Channel 7 DC Level Offset Values
0	0	0	0	0	0	1	1	1	1	0	A4	A3	A2	A1	A0	Channel 7 DC Level Gain Values
0	0	0	0	0	0	1	1	1	1	1	A4	A3	A2	A1	A0	Not Used
Per Pin Resource Register Storage																
Register Bit	Central Bit	Channel Address							Resource Address							Description
1	0	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 0 Registers
1	0	0	0	0	0	0	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 1 Registers
1	0	0	0	0	0	0	1	0	A6	A5	A4	A3	A2	A1	A0	Channel 2 Registers
1	0	0	0	0	0	0	1	1	A6	A5	A4	A3	A2	A1	A0	Channel 3 Registers
1	0	0	0	0	0	1	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 4 Registers
1	0	0	0	0	0	1	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 5 Registers
1	0	0	0	0	0	1	1	0	A6	A5	A4	A3	A2	A1	A0	Channel 6 Registers
1	0	0	0	0	0	1	1	1	A6	A5	A4	A3	A2	A1	A0	Channel 7 Registers
Central Resource Register Storage																
Register Bit	Central Bit	Channel Address							Resource Address							Description
1	1	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Central Resource Registers

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Protocol Timing Diagram

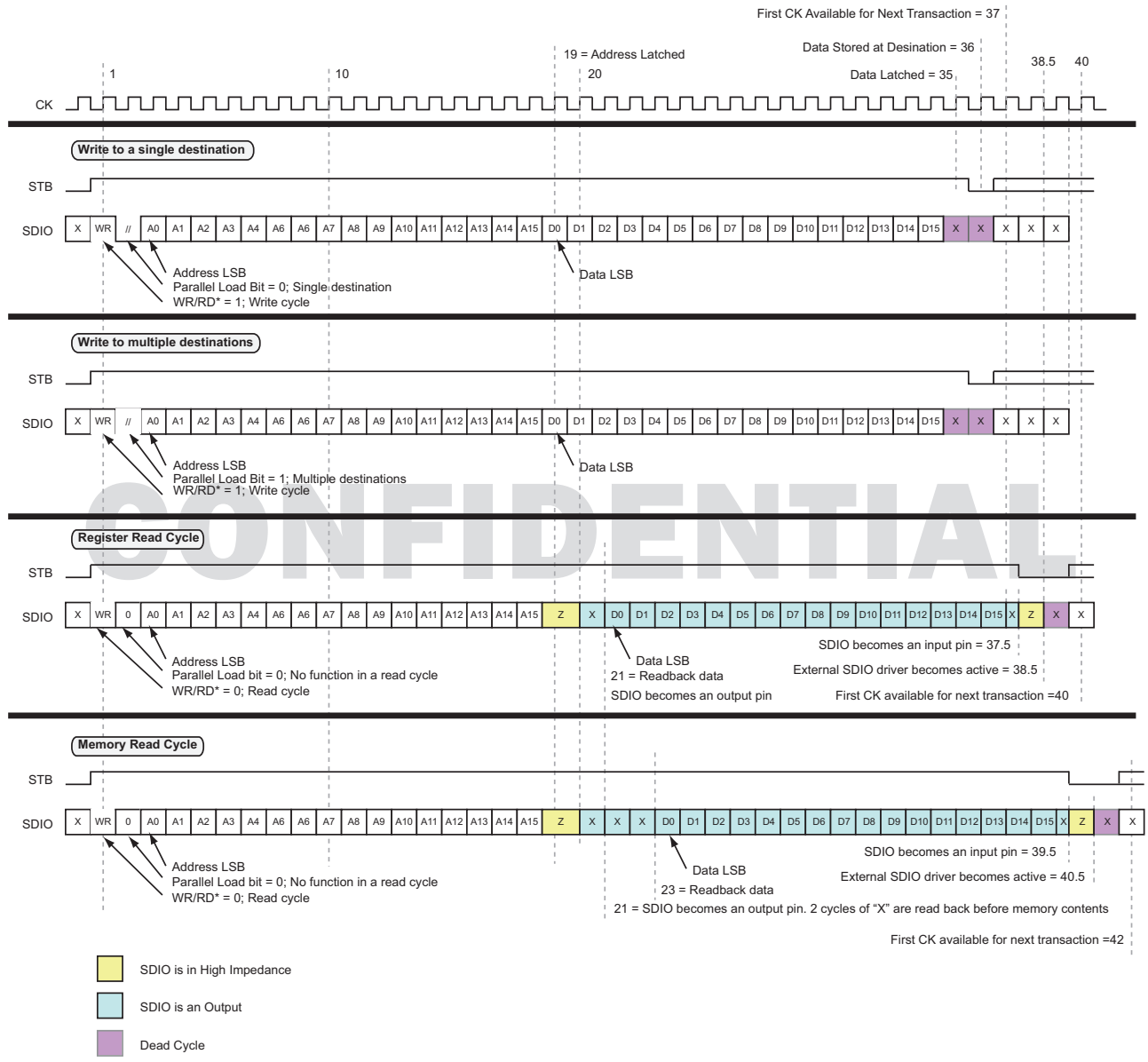

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FIGURE 27.

Per Pin DC Levels

Channel 0-7 RAM Storage (# = Channel Number)																
Register Bit	Central Bit	CHANNEL ADDRESS							DAC Function		RESOURCE ADDRESS					DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	0	0	FV0-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	0	1	FV1-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	1	0	Isource-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	0	0	0	1	1	Isink-#
0	0	0	0	0	0	0 ≤ # ≤ 7			0	0	4 – 31					Not used
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	0	0	FV0-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	0	1	FV1-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	1	0	Isource-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	0	0	0	1	1	Isink-# Offset
0	0	0	0	0	0	0 ≤ # ≤ 7			0	1	4 – 31					Not used
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	0	0	FV0-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	0	1	FV1-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	1	0	Isource-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	0	0	0	1	1	Isink-# Gain
0	0	0	0	0	0	0 ≤ # ≤ 7			1	0	4 – 31					Not used
0	0	0	0	0	0	0 ≤ # ≤ 7			1	1	0 – 31					Not used

NOTE: Do not write to or read from any of the unused locations.

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Per Pin Registers

TABLE 41.

Channel 0 – 7 Control Registers (0 ≤ # ≤ 7)																				
Register Big	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	#	0			WE	Sel-DG#	WE	Sel-RT-En#	CPU-En#	WE	Sel-RT-D#	CPU-D#	Sel-FV#	WE	CPU-Sel-FB#<1>	CPU-Sel-FB#<0>	WE	Load-BP#	Channel Configuration
1	0	#	1								WE	I-En#	WE	Il-Adj#<2>	IL-Adj#<1>	IL-Adj#<0>	WE	V-Range-Sel#<1>	V-Range-Sel#<0>	Range Selection
1	0	#	2											WE	IR#<4>	IR#<3>	IR#<2>	IR#<1>	IR#<0>	MI Range Select
1	0	#	3						WE	Mon-OE#	WE	Mon-Shift#<3>	Mon-Shift#<2>	Mon-Shift#<1>	Mon-Shift#<0>	WE	Mon-Scale#<2>	Mon-Scale#<1>	Mon-Scale#<0>	Per Channel Monitor Scaling and Shifting
1	0	#	4					WE	Sel-Diag#<1>	Sel-Diag#<0>	WE	Not Used	Sel-Vpos#<2>	Sel-Vpos#<1>	Sel-Vpos#<0>	WE	Not Used	Sel-Vneg#<1>	Sel-Vneg#<0>	Per Channel Monitor Source Selection
1	0	#	5														WE	Con-D-EF#	Con-D-ES#	External Force/Sense
1	0	#	6 – 27																	Not Used

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Central Resource Register

Register Big	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	1	0	0					WE	Sel-Tj-OE	CPU-Tj-OE	WE	Sel-Mon-Sel	WE	CPU-Sel-Mon<2>	CPU-Sel-Mon<1>	CPU-Sel-Mon<0>	WE	Sel-Mon-OE	CPU-Mon-OE	Monitor Control/TJ
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPU-Reset
1	1	0	2												WE	Vmid<3>	Vmid<2>	Vmid<1>	Vmid<0>	Vmid
1	1	0	3 – 4																	Not Used
1	1	0	5				WE	D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	WE	D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	Upper DAC Bit Calibration
1	1	0	6					WE	D11-Cal<1>	D11-Cal<0>	WE	D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	WE	D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13 -Cal<0>	Mid DAC Bit Calibration
1	1	0	7 – 126																	Not Used
1	1	0	127	Product-ID<11>	Product-ID<10>	Product-ID<9>	Product-ID<8>	Product-ID<7>	Product-ID<6>	Product-ID<5>	Product-ID<4>	Product-ID<3>	Product-ID<2>	Product-ID<=1>	Product-ID<0>	Die-Rev<3>	Die-Rev<2>	Die-Rev<1>	Die-Rev<0>	Die ID

Write Only

Read Only

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Manufacturing Information

Moisture Sensitivity

ISL55185 is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre-production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

Chip Floor Life ≤ 168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead free or not.

TABLE 42.

PROFILE FEATURE	Sn-Pb EUTECTIC ASSEMBLY	Pb-Free ASSEMBLY
Average ramp up rate (t_L to t_P)	3°C/sec (max)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 100°C 150°C 60s to 120s	 150°C 200°C 60s to 180s
ts max to t_L • Ramp Up Rate		 3°C/sec (max)
Time above • Temperature (T_L) • Time (t_L)	 183°C 60s to 150s	 217°C 60s to 150s
Peak Temperature (T_P)	240°C +0/–5°C	250°C + 0/–5°C
Time within 5°C of actual peak temp (tp)	10s – 30s	20s to 40s
Ramp down rate	6°C/sec (max)	6°C/sec (max)
Time +25°C to peak temperature	6 minutes (max)	8 minutes (max)

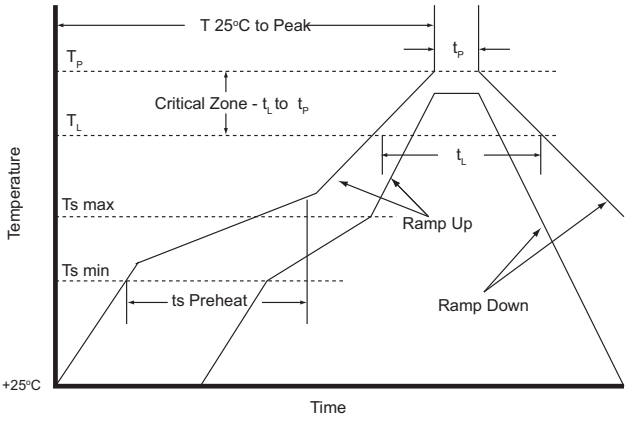

FIGURE 28. TIME vs TEMP

Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows the following equation:

$$T_J = Pd \bullet \theta_{JA} + T_A.$$

T_J = Junction Temperature

Pd = Power Dissipation

θ_{JA} = Thermal Resistance (Junction to Ambient)

T_A = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θ_{JC}) plus the resistance from the case to ambient (θ_{CA}).

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Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall θ_{JA}. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

θ_{CA} is determined by the system environment of the part and is therefore application specific. θ_{JC} is determined by the construction of the part.

ΘJC CALCULATION

θ_{JC} = θ(silicon)

+ θ(die attach)

+ θ(paddle).

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$\theta_{JC} = 0.072°C/W + 0.61°C/W + 0.006°C/W$

$\theta_{JC} = 0.688°C/W$.

The calculation is based upon ideal assumptions and it should be treated as a best-case value.

The thermal resistance of any material is defined by the equation:

θ = (Intrinsic material resistivity) • Thickness/Area

or

θ = Thickness / (Intrinsic material conductivity • Area).

INTRINSIC THERMAL CONDUCTIVITY

Die Attach Thermal Conductivity = 1.4 W/M°K

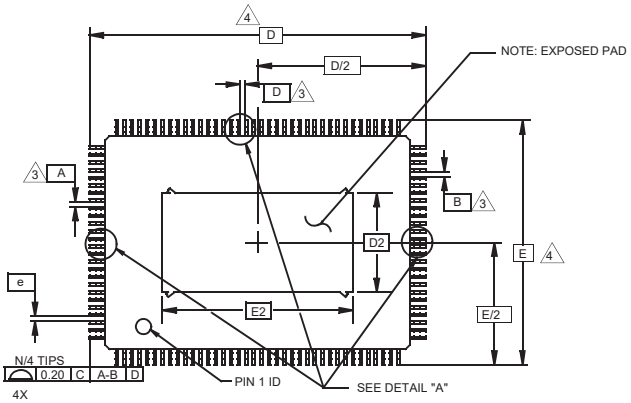
Silicon Thermal Conductivity = 141.2 W/M°K

Paddle Thermal Conductivity = 263 W/M°K

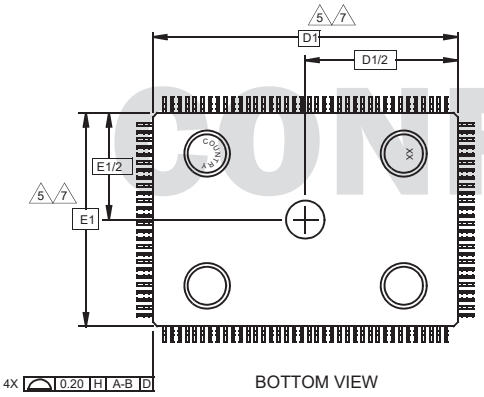
Plastic Thermal Conductivity = 0.88 W/M°K

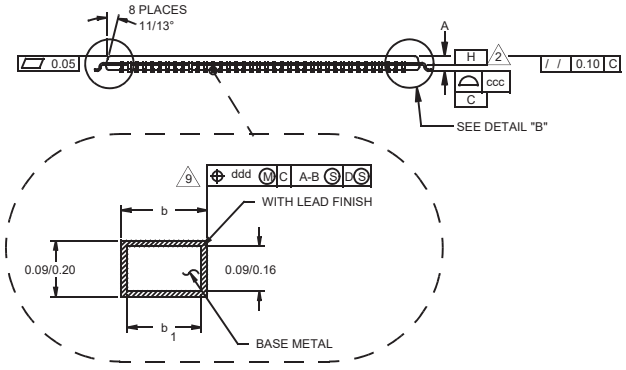
(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of Theta JC through the paddle. The assumption is that all heat flow will go through the paddle and none through the surrounding plastic.)

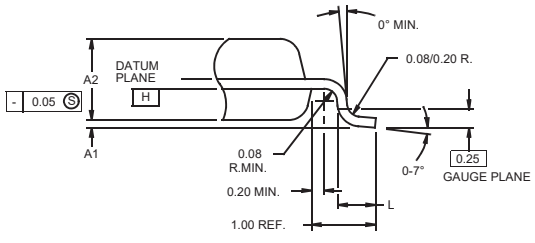
Low Plastic Quad Flatpack Package with Top Exposed Pad (LQFP-TEP)



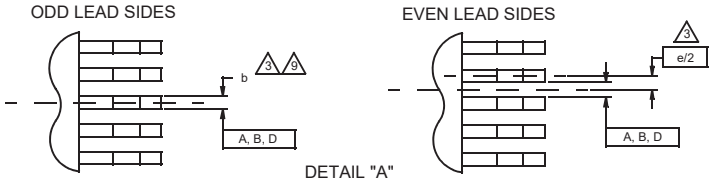
TOP VIEW







DETAIL "B"



DETAIL "A"

Q128.14x20A

128 Lead Low Quad Flatpack with Top Exposed Pad

SYMBOL	MILLIMETERS BHB MIN	NOM	MAX	NOTES
A	-	-	1.60	
A1	0.05	-	0.15	13
A2	1.35	1.40	1.45	
D		22 BSC		4
D1		20 BSC		7, 8
D2		12.50 BSC		14
E		16 BSC		4
E1		14 BSC		7, 8
E2		6.5 BSC		14
L	0.45	0.60	0.75	
N		128		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

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NOTES:

1. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at center lines between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254mm per side on D1 and E1 dimensions.
6. “N” is the total number of terminals.
7. These dimensions to be determined at datum plane H.
8. Package top dimensions are smaller than package bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located at the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC publication 95 Registration MS-026, variations BHA & BHB.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
14. Dimensions D2 and E2 represent the size of the exposed pad. The actual dimensions may be reduced up to 0.76mm due to mold flash.

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Revision History

DATE	CHANGE
January 8, 2016	• Page 31: Power Supply Sequence Section - update power supply sequence
April 1, 2015	• Update to Elevate format.
November 25, 2013	• Page 12 - Note 24: Change from Tested at VCC, VEE to VCC – 1V, VEE + 1V. • Page 14 - Spec # 14710: Change from Tested at VEE, (VCC + VEE)/2, VCC to Tested at VEE + 1V (VCC + VEE)/2, VCC – 1V

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Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PACKAGE DWG. NO.
ISL55185CNEZ	ISL55185CNEZ	0 to +70	128 Lead, 14x20mm LQFP w/exposed pad	Q128.14X20A
ISL55185CNEZ-LB	Evaluation Board			
ISL55185CNEZ-SYS	Evaluation Board			

NOTES:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020..

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