

IS62C5128BL, IS65C5128BL

512K x 8 HIGH-SPEED CMOS STATIC RAM

JULY 2011

FEATURES

- High-speed access time: 45ns
- Low Active Power: 50 mW (typical)
- Low Standby Power: 10 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single 5V $\pm$ 10% power supply
- Fully static operation: no clock or refresh required
- Available in 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

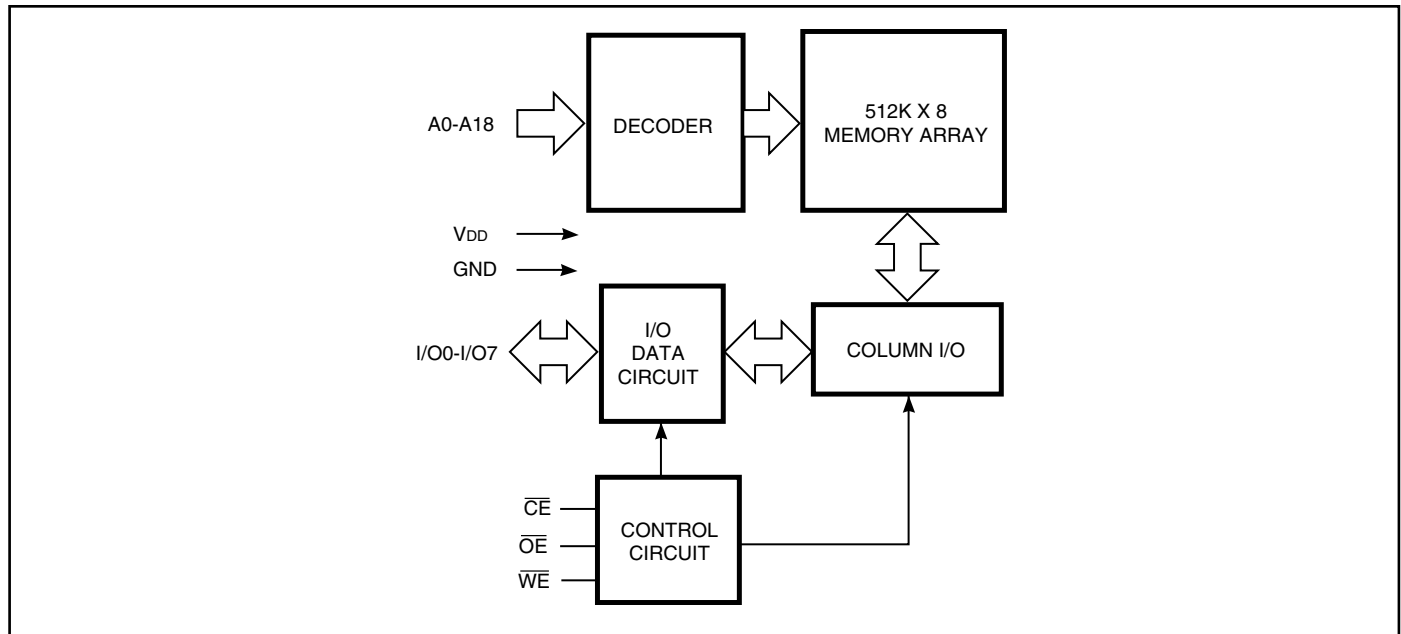
The *ISSI* IS62C5128BL and IS65C5128BL are high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 45ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS62C5128BL and IS65C5128BL are packaged in the JEDEC standard 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages

FUNCTIONAL BLOCK DIAGRAM



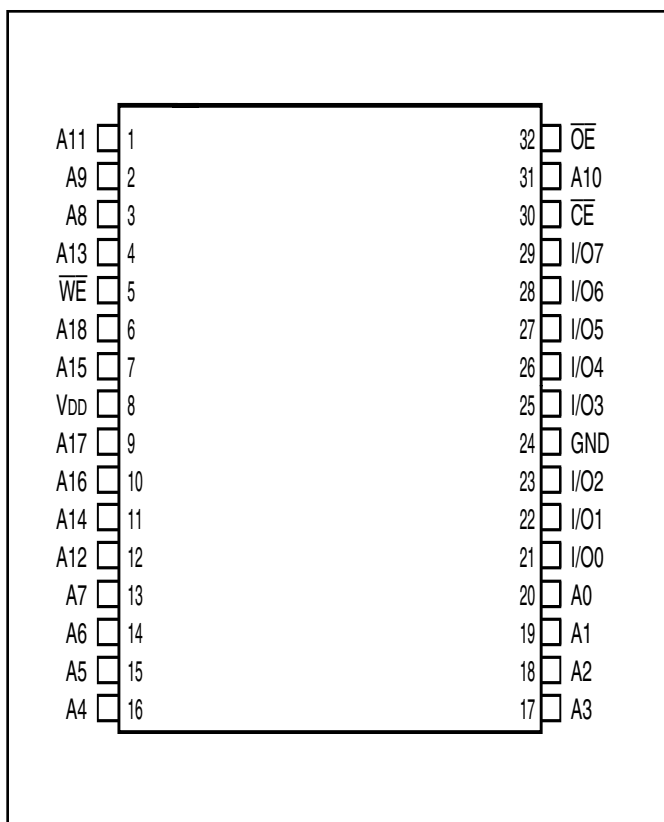
Copyright © 2010 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

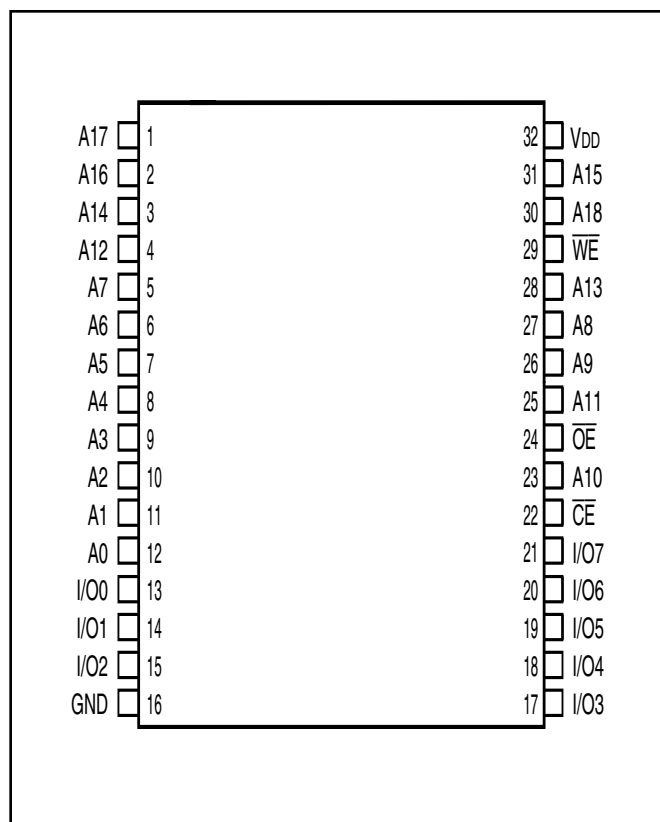
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATION

32-pin sTSOP (TYPE I)



32-pin SOP 32-pin TSOP (TYPE II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O PIN	
				I/O0-I/O7	V _{DD} Current
Not Selected	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{CC1} , I _{CC2}
Read	H	L	L	D _{OUT}	I _{CC1} , I _{CC2}
Write	L	L	X	D _{IN}	I _{CC1} , I _{CC2}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.5	W
I _{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -1.0 mA		2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 2.1 mA		—	0.4	V
V _{IH}	Input HIGH Voltage ⁽¹⁾			2.2	V _{DD} + 0.5	V
V _{IL}	Input LOW Voltage ⁽¹⁾			-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} Outputs Disabled	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA

Note:

1. V_{ILL} (min) = -2.0V AC (pulse width <10 ns). Not 100% tested.
V_{IHH} (max) = V_{DD} + 2.0V AC (pulse width <10 ns). Not 100% tested.

OPERATING RANGE

Range	Ambient Temperature	V _{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	45
Industrial	-40°C to +85°C	5V ± 10%	45
Automotive	-40°C to +125°C	5V ± 10%	45

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns		Unit
				Min.	Max.	
I _{CC}	Average operating Current	$\overline{CE} = V_{IL}$, V _{DD} = Max. I _{OUT} = 0 mA, f = 0	Com.	—	10	mA
			Ind.	—	10	
			Auto.	—	10	
I _{CC1}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	15	mA
			Ind.	—	20	
			Auto.	—	25	
			typ. ⁽²⁾		10	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} , $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	1	mA
			Ind.	—	1.5	
			Auto.	—	2	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ V _{SS} + 0.2V, f = 0	Com.	—	10	μA
			Ind.	—	15	
			Auto.	—	35	
			typ.		4	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

-45				
Symbol	Parameter	Min.	Max.	Unit
t_{RC}	Read Cycle Time	45	—	ns
t_{AA}	Address Access Time	—	45	ns
t_{OHA}	Output Hold Time	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	20	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	15	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	5	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	15	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	5	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

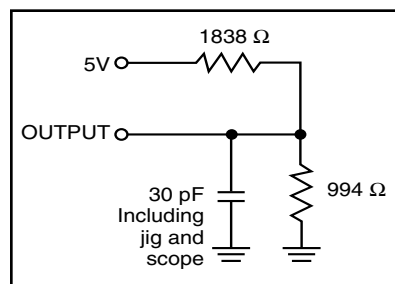
AC TEST LOADS


Figure 1

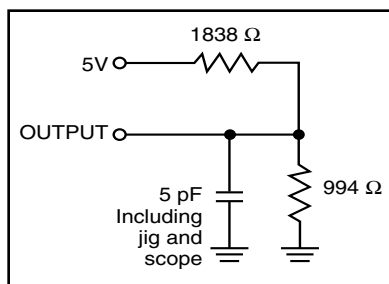
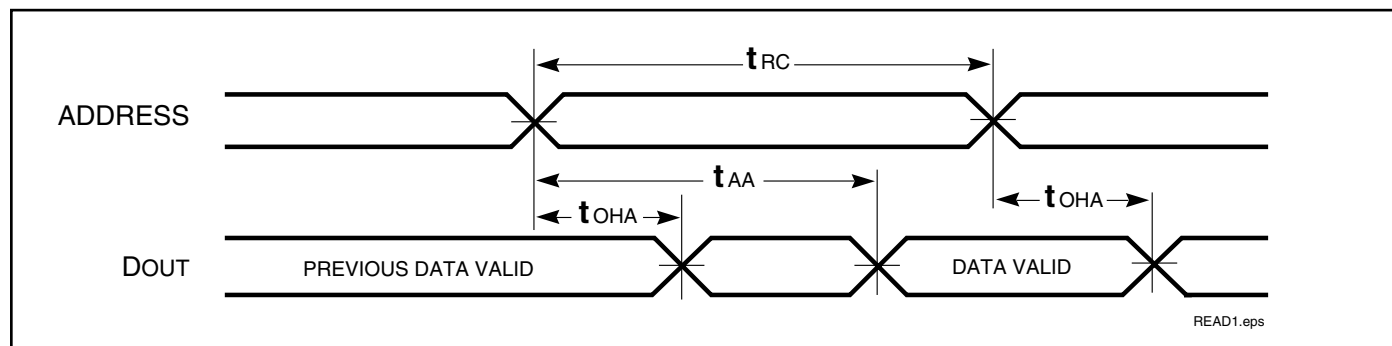
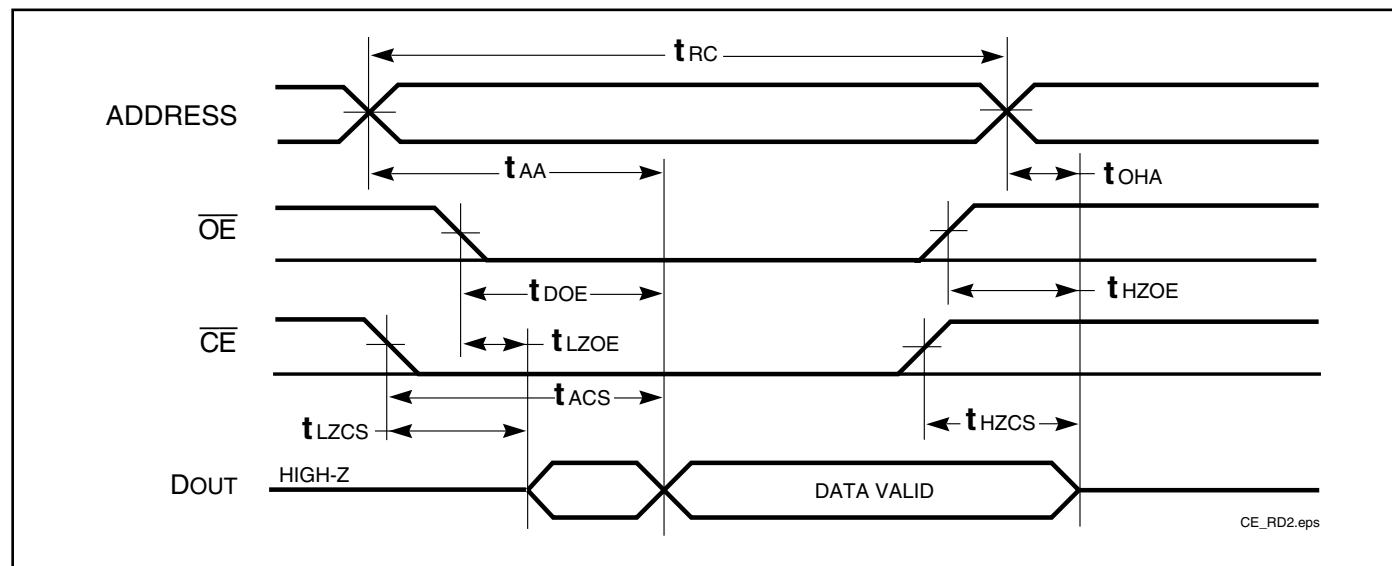


Figure 2

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)READ CYCLE NO. 2^(1,3)

Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL} .
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

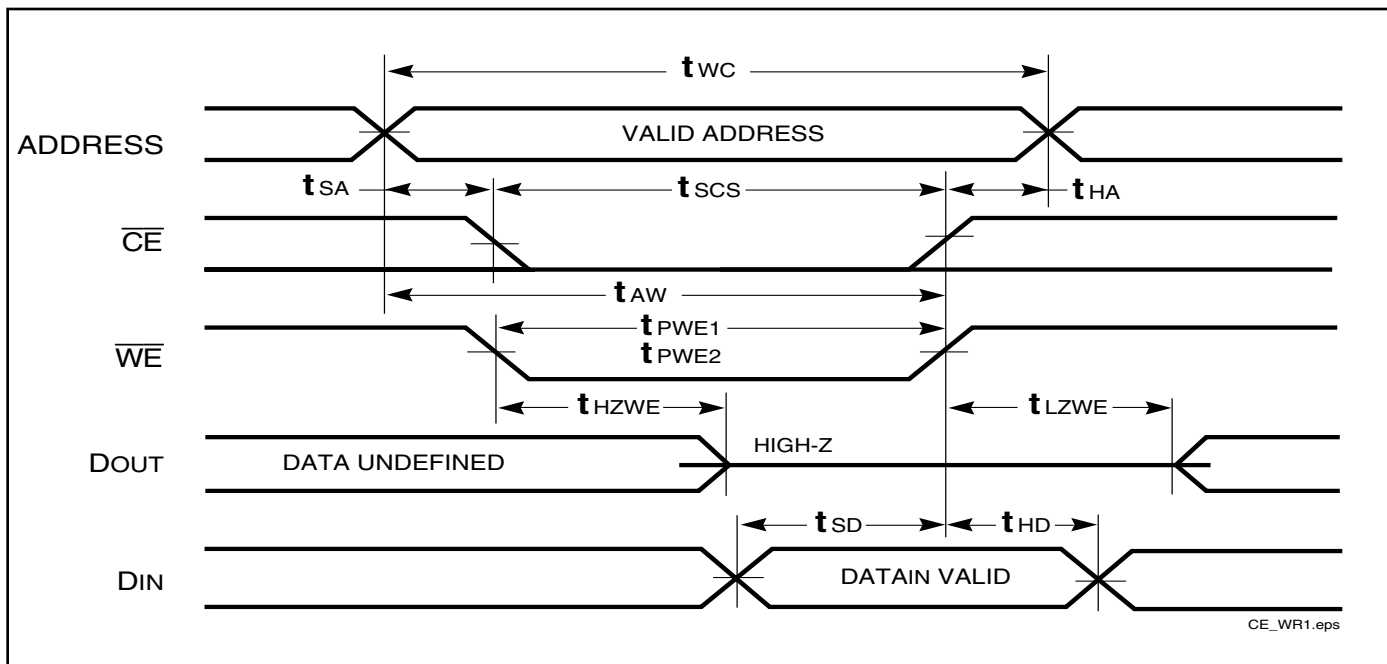
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-45		Unit
		Min.	Max.	
t _{WC}	Write Cycle Time	45	—	ns
t _{SCE}	$\overline{\text{CE}}$ to Write End	35	—	ns
t _{AW}	Address Setup Time to Write End	35	—	ns
t _{HA}	Address Hold from Write End	0	—	ns
t _{SA}	Address Setup Time	0	—	ns
t _{PWE1}	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ =High)	35	—	ns
t _{PWE2}	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ =Low)	35	—	ns
t _{SD}	Data Setup to Write End	25	—	ns
t _{HD}	Data Hold from Write End	0	—	ns
t _{HZWE} ⁽²⁾	$\overline{\text{WE}}$ LOW to High-Z Output	—	15	ns
t _{LZWE} ⁽²⁾	$\overline{\text{WE}}$ HIGH to Low-Z Output	5	—	ns

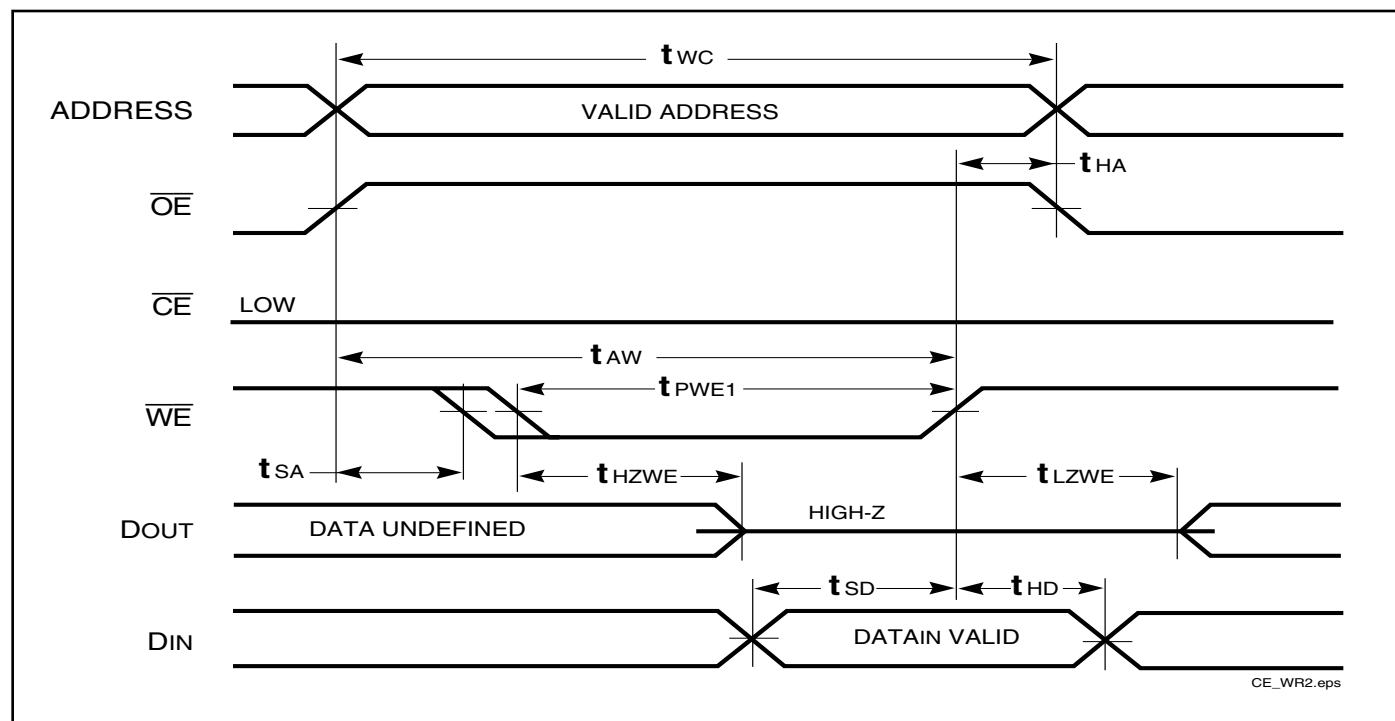
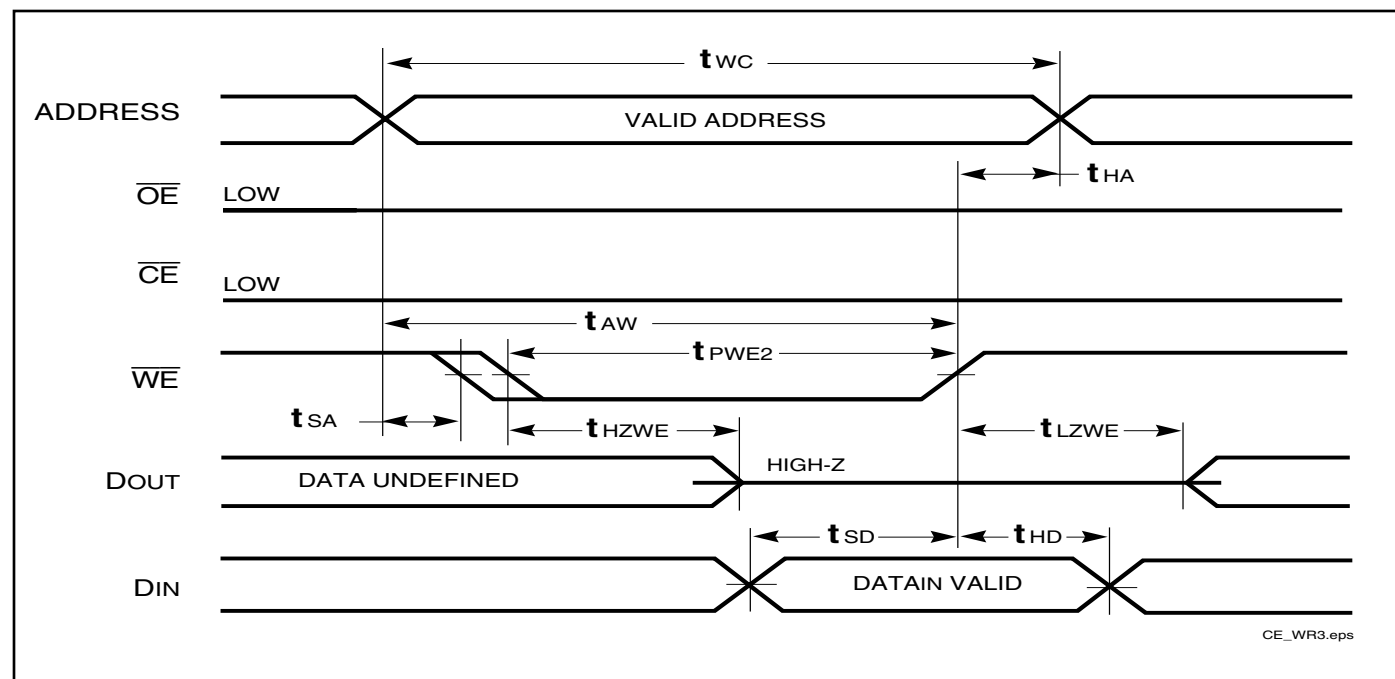
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)^(1,2)**Notes:**

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) ^(1,2)

WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) ⁽¹⁾

Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

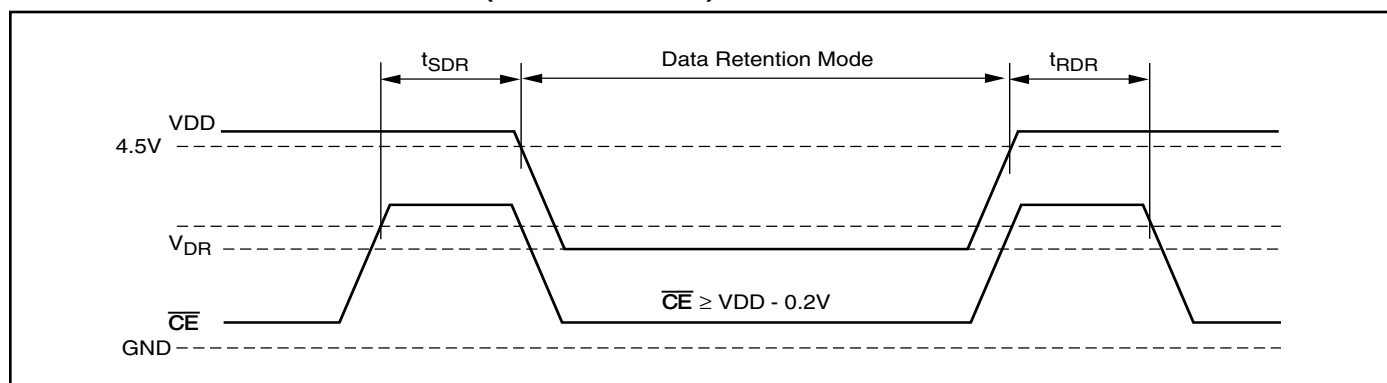
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.0	5.5	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V$, $\overline{CE} \geq V_{DD} - 0.2V$	—	10	μA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	—	15	
		Auto. typ. ⁽¹⁾	—	35	
				2	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

Note:

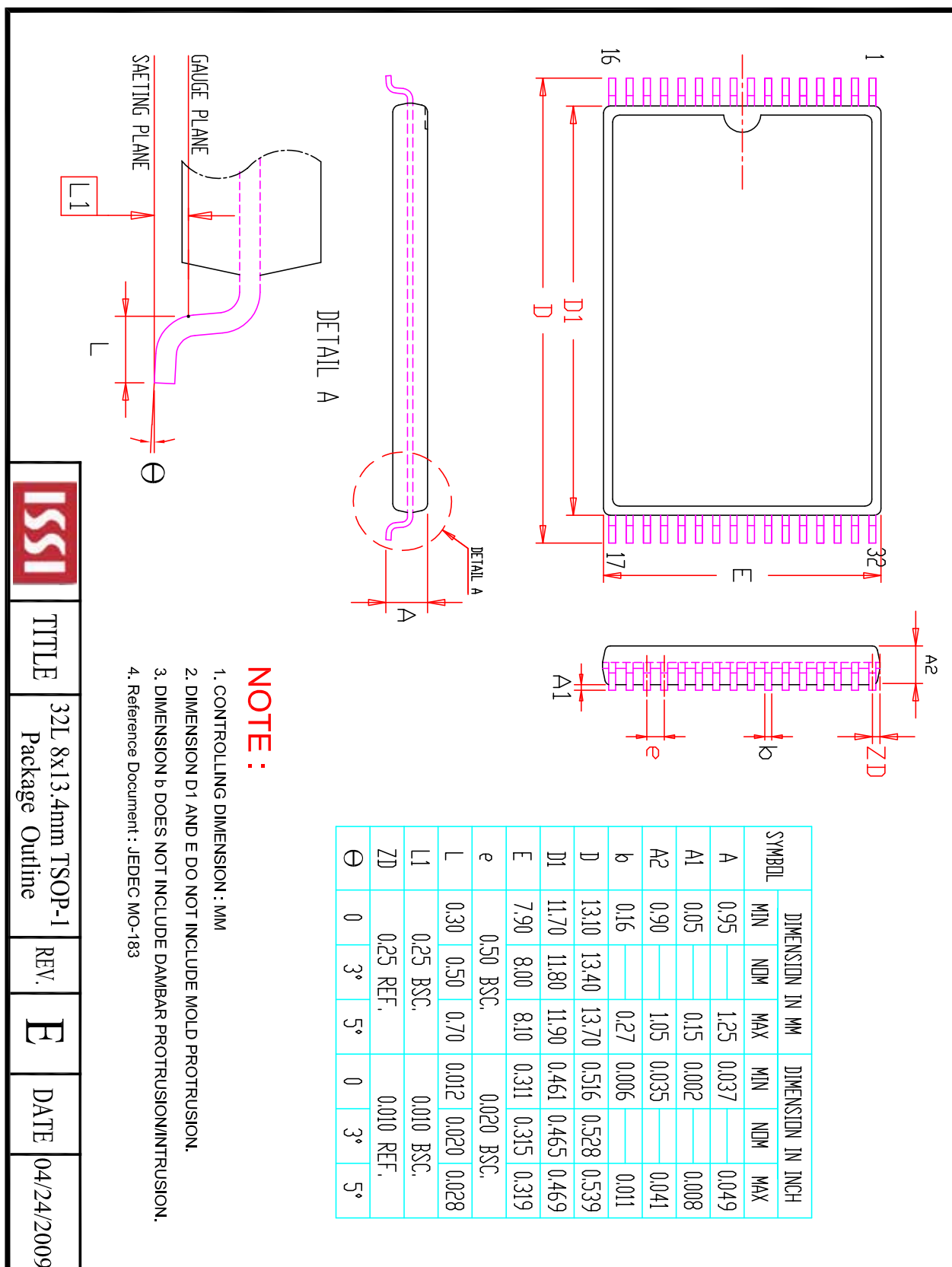
1. Typical Values are measured at $V_{DD} = 5V$, $T_A = 25^\circ C$ and not 100% tested.

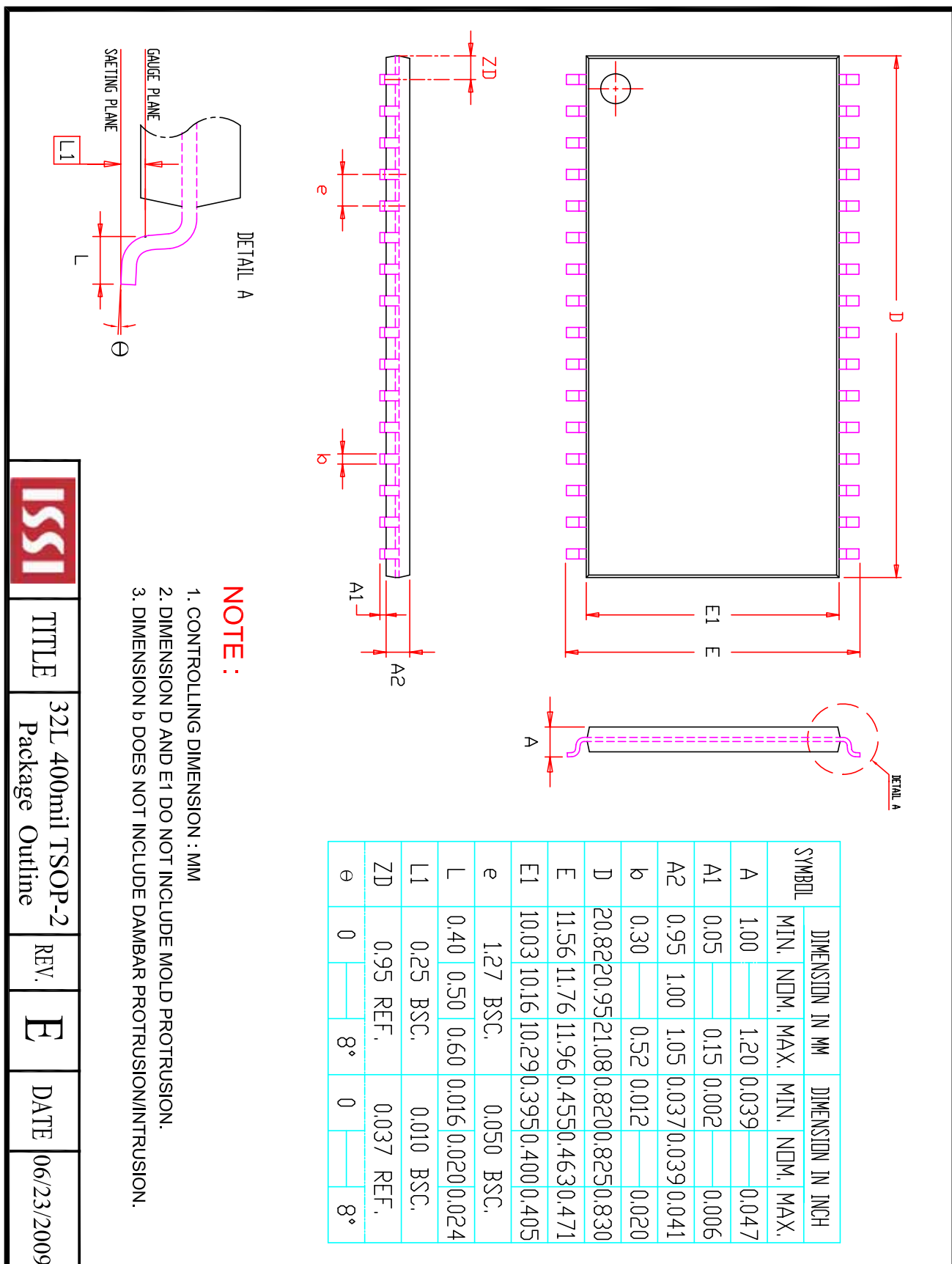
DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION**Industrial Range: –40°C to +85°C**

Speed (ns)	Order Part No.	Package
45	IS62C5128BL-45QI	450-mil Plastic SOP
	IS62C5128BL-45QLI	450-mil Plastic SOP, Lead-free
	IS62C5128BL-45HI	32-pin STSOP-I
	IS62C5128BL-45HLI	32-pin STSOP-I, Lead-free
	IS62C5128BL-45TI	32-pin TSOP-II
	IS62C5128BL-45TLI	32-pin TSOP-II, Lead-free





TITLE

32L 400mil TSOP-2
Package Outline

REV.

E

DATE

06/23/2009

