# IS62C1024

## 128K x 8 HIGH-SPEED CMOS STATIC RAM

**JULY 1996**

### FEATURES

- High-speed access time: 35, 45, 55, 70 ns
- Low active power: 450 mW (typical)
- Low standby power: 500 µW (typical) CMOS standby
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V (±10%) power supply

### DESCRIPTION

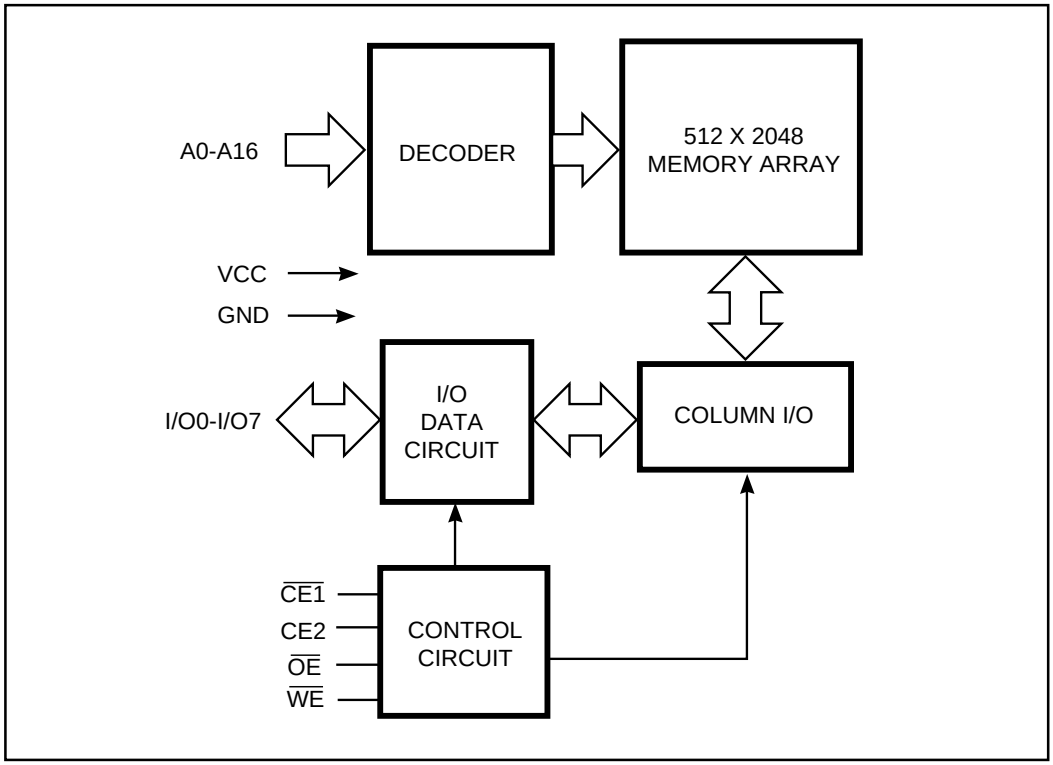
The *ISSI* IS62C1024 is a low power,131,072-word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

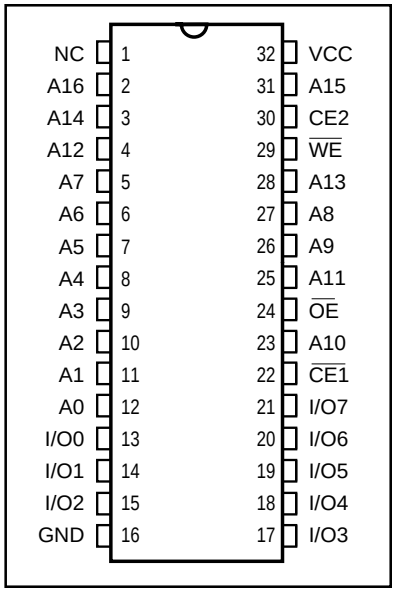
Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62C1024 is available in 32-pin 600-mil plastic DIP, 525-mil plastic SOP and TSOP (type 1) packages.

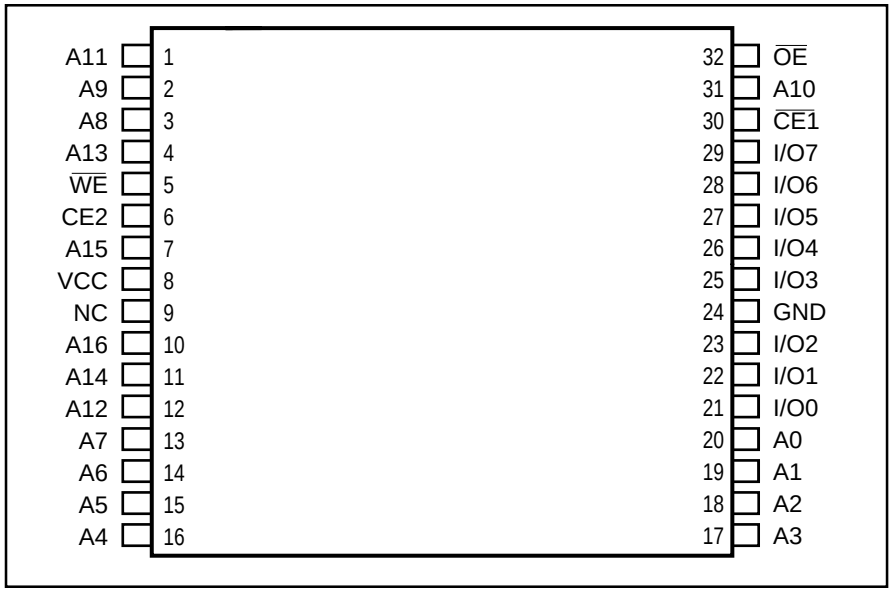
### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION
### 32-Pin SOP and DIP




## PIN CONFIGURATION
### 32-Pin TSOP (Type 1)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A16 | Address Inputs |
| $\overline{CE1}$ | Chip Enable 1 Input |
| CE2 | Chip Enable 2 Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| Vcc | Power |
| GND | Ground |

## OPERATING RANGE

| Range | Ambient Temperature | Vcc |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | –40°C to +85°C | 5V ± 10% |

## TRUTH TABLE

| Mode | $\overline{WE}$ | $\overline{CE1}$ | CE2 | $\overline{OE}$ | I/O Operation | Vcc Current |
|---|---|---|---|---|---|---|
| Not Selected | X | H | X | X | High-Z | $I_{SB1}$, $I_{SB2}$ |
| (Power-down) | X | X | L | X | High-Z | $I_{SB1}$, $I_{SB2}$ |
| Output Disabled | H | L | H | H | High-Z | $I_{CC}$ |
| Read | H | L | H | L | $D_{OUT}$ | $I_{CC}$ |
| Write | L | L | H | X | $D_{IN}$ | $I_{CC}$ |

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $T_{BIAS}$ | Temperature Under Bias | –10 to +85 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.5 | W |
| $I_{OUT}$ | DC Output Current (LOW) | 20 | mA |

**Notes:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE[1,2]

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, Vcc = 5.0V.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –1.0 mA | | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 2.1 mA | | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | Com.<br>Ind. | –5<br>–10 | 5<br>10 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{CC}$ | Com.<br>Ind. | –5<br>–10 | 5<br>10 | µA |

**Notes:**
1. $V_{IL}$ = –3.0V for pulse width less than 10 ns.

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| | | | | -35 ns | | -45 ns | | -55 ns | | -70 ns | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Unit |
| $I_{CC}$ | Vcc Dynamic Operating Supply Current | $V_{CC}$ = Max., $\overline{CE}$ = $V_{IL}$<br>$I_{OUT}$ = 0 mA, f = $f_{MAX}$ | Com.<br>Ind. | —<br>— | 150<br>160 | —<br>— | 135<br>145 | —<br>— | 120<br>130 | —<br>— | 90<br>100 | mA |
| $I_{SB1}$ | TTL Standby Current (TTL Inputs) | $V_{CC}$ = Max.,<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\overline{CE1}$ ≥ $V_{IH}$,<br>or CE2 ≤ $V_{IL}$, f = 0 | Com.<br>Ind. | —<br>— | 40<br>60 | —<br>— | 40<br>60 | —<br>— | 40<br>60 | —<br>— | 40<br>60 | mA |
| $I_{SB2}$ | CMOS Standby Current (CMOS Inputs) | $V_{CC}$ = Max.,<br>$\overline{CE1}$ ≤ $V_{CC}$ – 0.2V,<br>CE2 ≤ 0.2V, $V_{IN}$ > $V_{CC}$ – 0.2V,<br>or $V_{IN}$ ≤ 0.2V, f = 0 | Com.<br>Ind. | —<br>— | 30<br>40 | —<br>— | 30<br>40 | —<br>— | 30<br>40 | —<br>— | 30<br>40 | mA |

**Notes:**
1. At f = $f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | -35 Min. | -35 Max. | -45 Min. | -45 Max. | -55 Min. | -55 Max. | -70 Min. | -70 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 35 | — | 45 | — | 55 | — | 70 | — | ns |
| $t_{AA}$ | Address Access Time | — | 35 | — | 45 | — | 55 | — | 70 | ns |
| $t_{OHA}$ | Output Hold Time | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| $t_{ACE1}$ | $\overline{CE1}$ Access Time | — | 35 | — | 45 | — | 55 | — | 70 | ns |
| $t_{ACE2}$ | CE2 Access Time | — | 35 | — | 45 | — | 55 | — | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ Access Time | — | 10 | — | 20 | — | 25 | — | 35 | ns |
| $t_{LZOE}$[2] | $\overline{OE}$ to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZOE}$[2] | $\overline{OE}$ to High-Z Output | 0 | 10 | 0 | 15 | 0 | 20 | 0 | 25 | ns |
| $t_{LZCE1}$[2] | $\overline{CE1}$ to Low-Z Output | 3 | — | 5 | — | 7 | — | 10 | — | ns |
| $t_{LZCE2}$[2] | CE2 to Low-Z Output | 3 | — | 5 | — | 7 | — | 10 | — | ns |
| $t_{HZCE}$[2] | $\overline{CE1}$ or CE2 to High-Z Output | 0 | 10 | 0 | 15 | 0 | 20 | 0 | 25 | ns |

**Notes:**
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

## AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1a and 1b |

## AC TEST LOADS

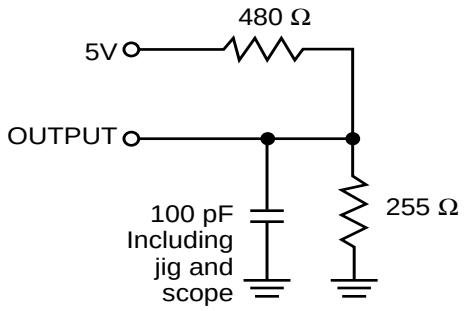



**Figure 1a.**

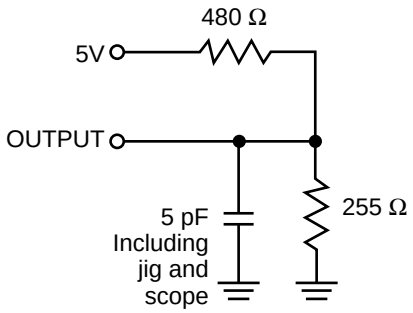
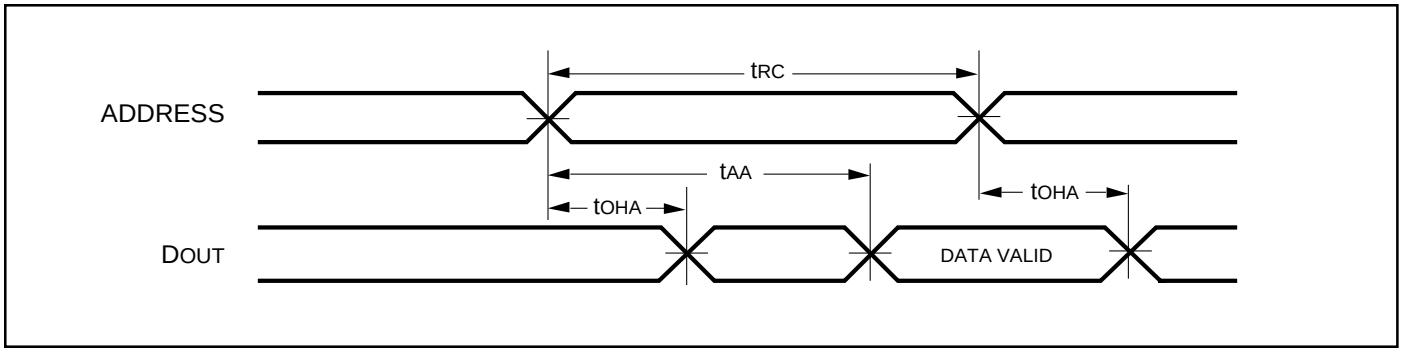


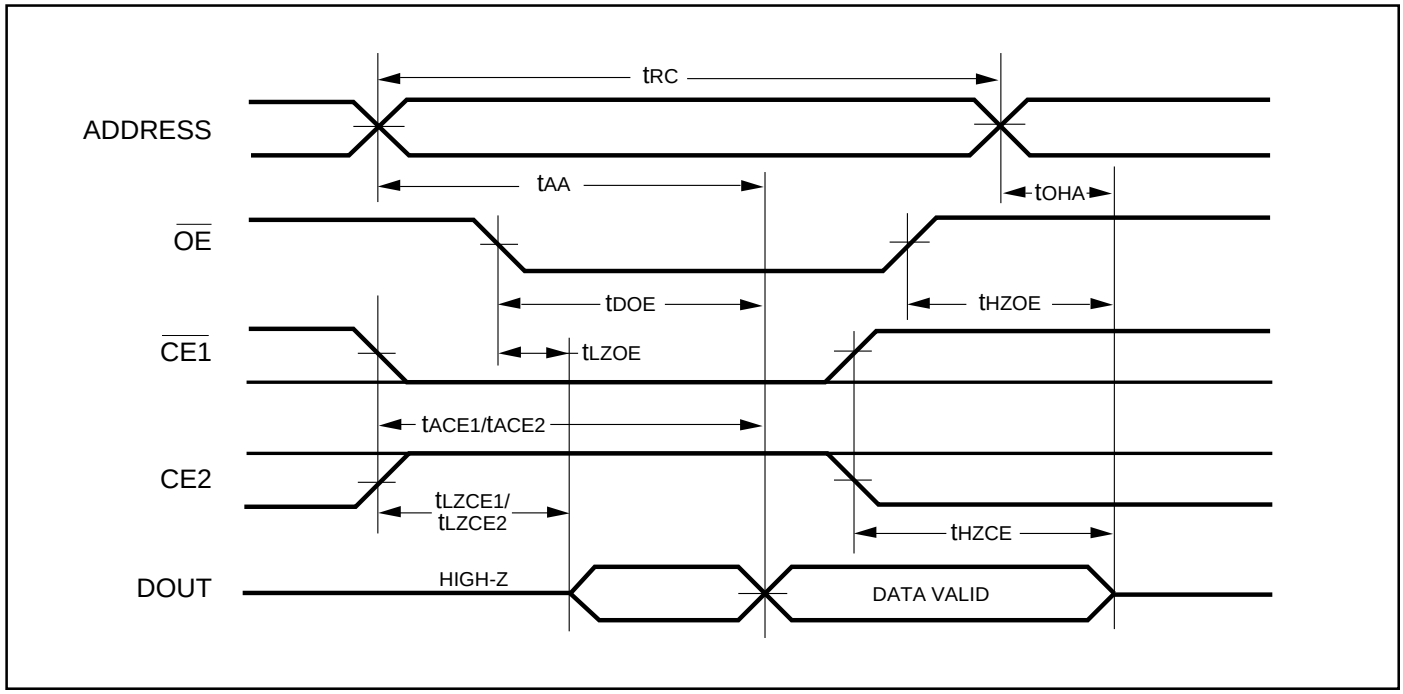

**Figure 1b.**

## AC WAVEFORMS

### READ CYCLE NO. 1[1,2]




### READ CYCLE NO. 2[1,3]




**Notes:**
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

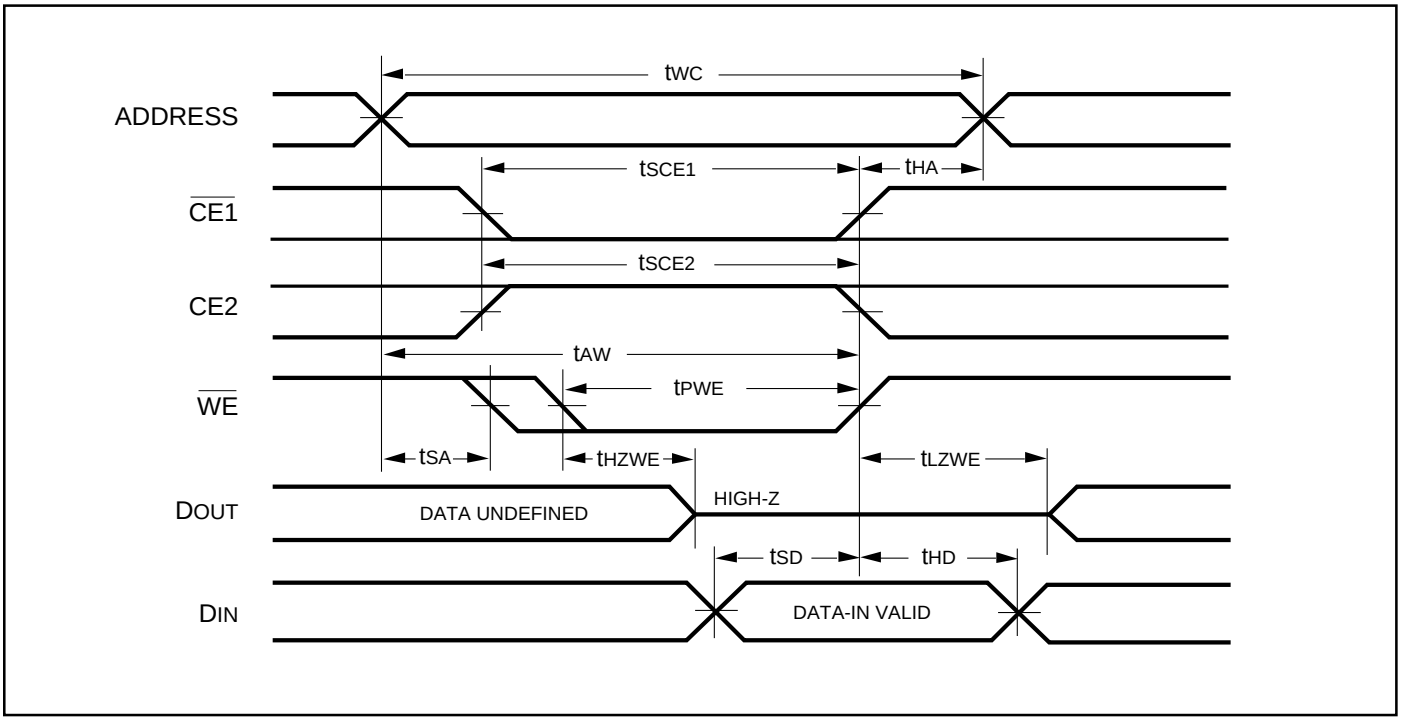
## WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range, Standard and Low Power)

| | | -35 | | -45 | | -55 | | -70 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Unit |
| $t_{WC}$ | Write Cycle Time | 35 | — | 45 | — | 55 | — | 70 | — | ns |
| $t_{SCE1}$ | $\overline{CE1}$ to Write End | 25 | — | 35 | — | 50 | — | 60 | — | ns |
| $t_{SCE2}$ | CE2 to Write End | 25 | — | 35 | — | 50 | — | 60 | — | ns |
| $t_{AW}$ | Address Setup Time to Write End | 25 | — | 35 | — | 45 | — | 60 | — | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{SA}$ | Address Setup Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PWE}$[4] | $\overline{WE}$ Pulse Width | 25 | — | 35 | — | 40 | — | 50 | — | ns |
| $t_{SD}$ | Data Setup to Write End | 20 | — | 25 | — | 25 | — | 30 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZWE}$[2] | $\overline{WE}$ LOW to High-Z Output | — | 10 | — | 15 | — | 20 | — | 25 | ns |
| $t_{LZWE}$[2] | $\overline{WE}$ HIGH to Low-Z Output | 3 | — | 5 | — | 5 | — | 5 | — | ns |

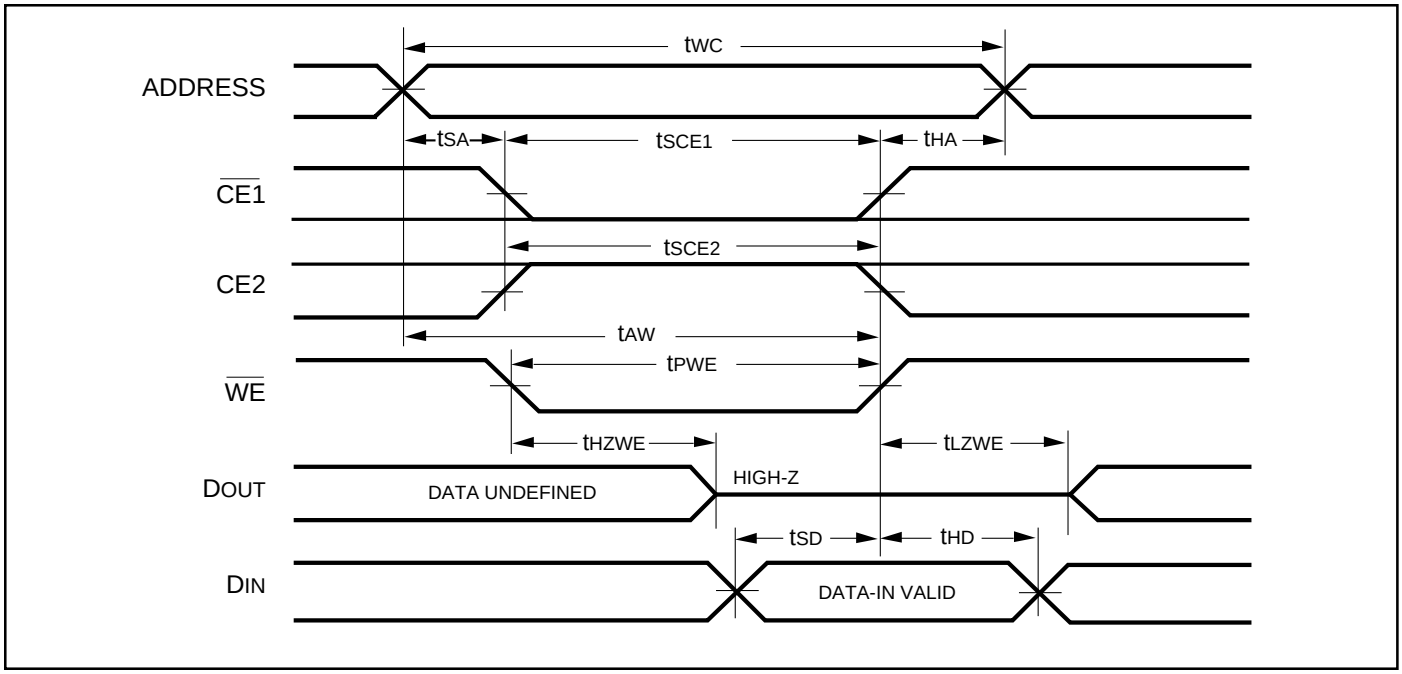
**Notes:**
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

## AC WAVEFORMS

### WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



## WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)[1,2]




**Notes:**
1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = $V_{IH}$.

## ORDERING INFORMATION
## Commercial Range: 0°C to +70°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 35 | IS62C1024-35W | 600-mil Plastic DIP |
| 35 | IS62C1024-35Q | 525-mil Plastic SOP |
| 35 | IS62C1024-35T | TSOP, Type 1 |
| 45 | IS62C1024-45W | 600-mil Plastic DIP |
| 45 | IS62C1024-45Q | 525-mil Plastic SOP |
| 45 | IS62C1024-45T | TSOP, Type 1 |
| 55 | IS62C1024-55W | 600-mil Plastic DIP |
| 55 | IS62C1024-55Q | 525-mil Plastic SOP |
| 55 | IS62C1024-55T | TSOP, Type 1 |
| 70 | IS62C1024-70W | 600-mil Plastic DIP |
| 70 | IS62C1024-70Q | 525-mil Plastic SOP |
| 70 | IS62C1024-70T | TSOP, Type 1 |

## ORDERING INFORMATION
## Industrial Range: –40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 35 | IS62C1024-35WI | 600-mil Plastic DIP |
| 35 | IS62C1024-35QI | 525-mil Plastic SOP |
| 35 | IS62C1024-35TI | TSOP, Type 1 |
| 45 | IS62C1024-45WI | 600-mil Plastic DIP |
| 45 | IS62C1024-45QI | 525-mil Plastic SOP |
| 45 | IS62C1024-45TI | TSOP, Type 1 |
| 55 | IS62C1024-55WI | 600-mil Plastic DIP |
| 55 | IS62C1024-55QI | 525-mil Plastic SOP |
| 55 | IS62C1024-55TI | TSOP, Type 1 |
| 70 | IS62C1024-70WI | 600-mil Plastic DIP |
| 70 | IS62C1024-70QI | 525-mil Plastic SOP |
| 70 | IS62C1024-70TI | TSOP, Type 1 |

NOTICE

Integrated Silicon Solution, Inc., reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. Integrated Silicon Solution, Inc. assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein reflect representative operating parameters, and may vary depending upon a user's specific application. While the information in this publication has been carefully checked, Integrated Silicon Solution, Inc. shall not be liable for any damages arising as a result of any error or omission.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurances, to its satisfaction, that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; and (c) potential liability of Integrated Silicon Solution, Inc. is adequately protected under the circumstances.



***Integrated Silicon Solution, Inc.***
680 Almanor Avenue
Sunnyvale, CA 94086
Tel: (408) 733-4774
Fax: (408) 245-4774
800-379-4774
http://www.issiusa.com