IS41C16128

128K x 16 (2-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

AUGUST 1998

FEATURES

- Extended Data-Out (EDO) Page Mode access cycle
- TTL compatible inputs and outputs
- Refresh Interval: 512 cycles/8 ms
- Refresh Mode : $\overline{RAS}$ -Only, $\overline{CAS}$ -before-$\overline{RAS}$ (CBR), and Hidden
- JEDEC standard pinout
- Single +5V ± 10% power supply
- Byte Write and Byte Read operation via two $\overline{CAS}$
- Available in 40-pin SOJ and TSOP (Type II)
- Industrial temperature available

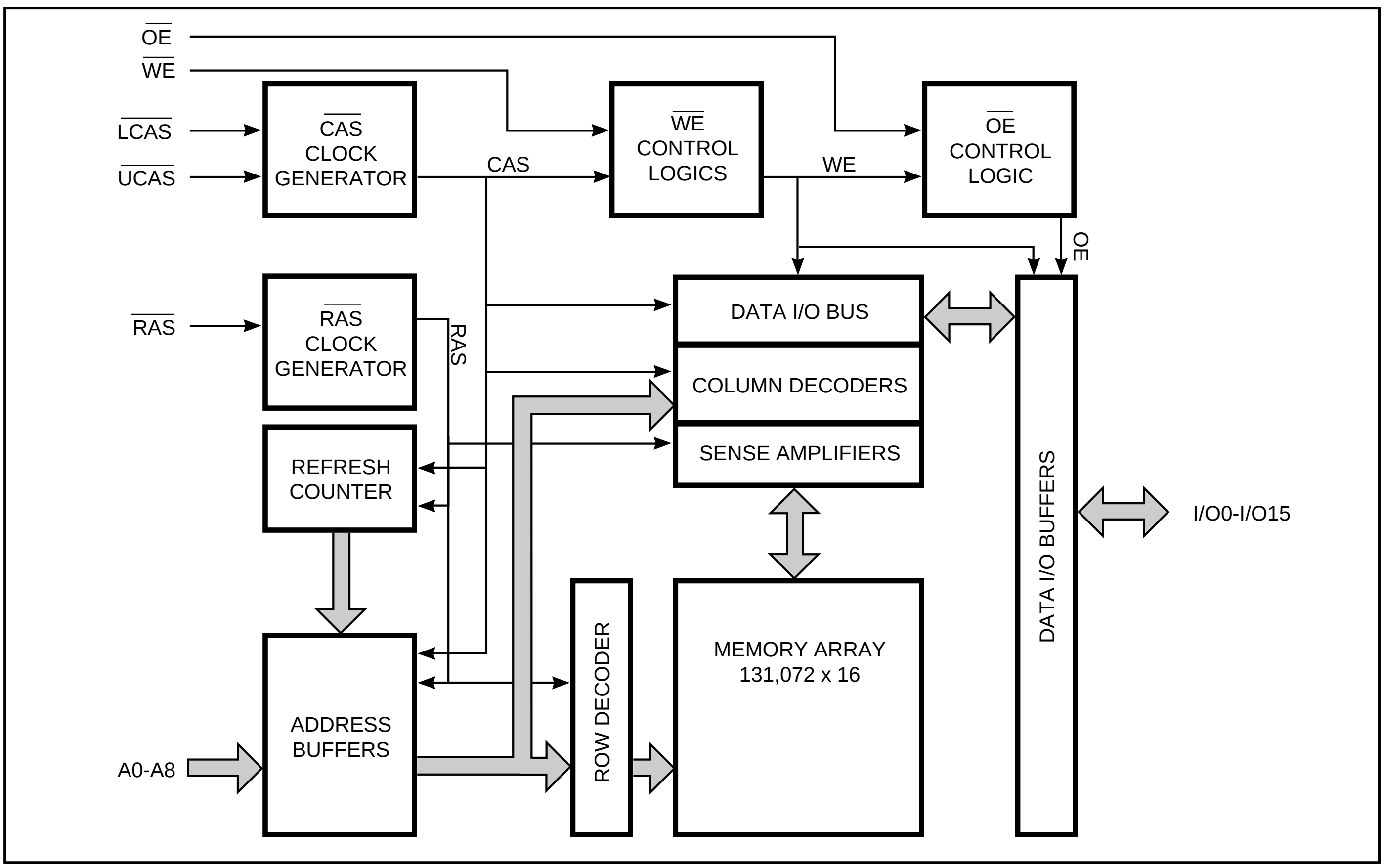
DESCRIPTION

The *ISSI* IS41C16128 is a 131,072 x 16-bit high-performance CMOS Dynamic Random Access Memory. The IS41C16128 offers an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 256 random accesses within a single row with access cycle time as short as 12 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes the IS41C16128 ideal for use in 16-, 32-bit wide data bus systems.

These features make the IS41C16128 ideally suited for high band-width graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS41C16128 is packaged in a 40-pin 400-mil SOJ and TSOP (Type II).

FUNCTIONAL BLOCK DIAGRAM

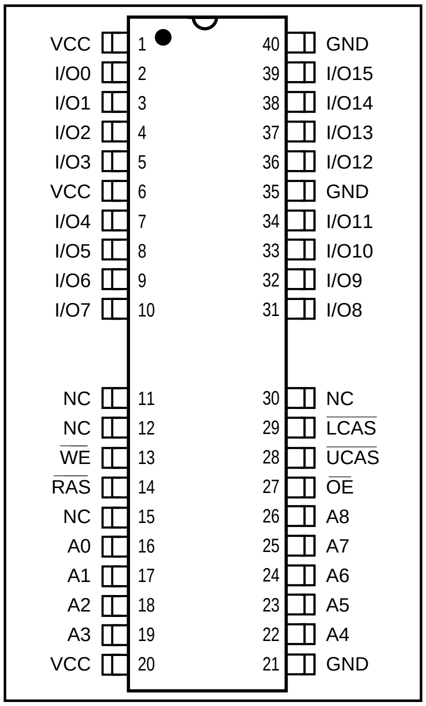


KEY TIMING PARAMETERS

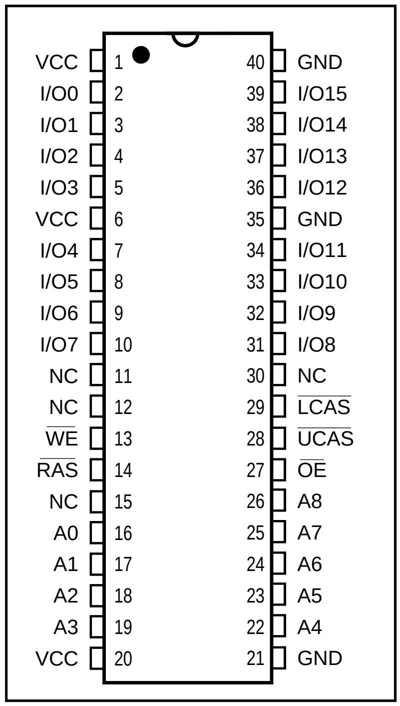
Parameter	-35	-40	-45	-50	-60
Max. $\overline{RAS}$ Access Time (t_{RAC})	35 ns	40 ns	45 ns	50 ns	60 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	10 ns	12 ns	13 ns	14 ns	15 ns
Max. Column Address Access Time (t_{AA})	18 ns	20 ns	22 ns	25 ns	30 ns
Min. EDO Page Mode Cycle Time (t_{PC})	12 ns	15 ns	17 ns	20 ns	25 ns
Min. Read/Write Cycle Time (t_{RC})	60 ns	75 ns	80 ns	90 ns	110 ns

PIN CONFIGURATIONS

40-Pin TSOP (Type II)



40-Pin SOJ



PIN DESCRIPTIONS

A0-A8	Address Inputs
I/O0-15	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Address t_R/t_C	I/O
Standby		H	H	H	X	X	X	High-Z
Read: Word		L	L	L	H	L	ROW/COL	D_{OUT}
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte, D_{OUT} Upper Byte, High-Z
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, D_{OUT}
Write: Word (Early Write)		L	L	L	L	X	ROW/COL	D_{IN}
Write: Lower Byte (Early Write)		L	L	H	L	X	ROW/COL	Lower Byte, D_{IN} Upper Byte, High-Z
Write: Upper Byte (Early Write)		L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, D_{IN}
Read-Write[1,2]		L	L	L	H→L	L→H	ROW/COL	D_{OUT}, D_{IN}
EDO Page-Mode Read[2]	1st Cycle:	L	H→L	H→L	H	L	ROW/COL	D_{OUT}
	2nd Cycle:	L	H→L	H→L	H	L	NA/COL	D_{OUT}
	Any Cycle:	L	L→H	L→H	H	L	NA/NA	D_{OUT}
EDO Page-Mode Write[1]	1st Cycle:	L	H→L	H→L	L	X	ROW/COL	D_{IN}
	2nd Cycle:	L	H→L	H→L	L	X	NA/COL	D_{IN}
EDO Page-Mode Read-Write[1,2]	1st Cycle:	L	H→L	H→L	H→L	L→H	ROW/COL	D_{OUT}, D_{IN}
	2nd Cycle:	L	H→L	H→L	H→L	L→H	NA/COL	D_{OUT}, D_{IN}
Hidden Refresh[2)]	Read	L→H→L	L	L	H	L	ROW/COL	D_{OUT}
	Write	L→H→L	L	L	L	X	ROW/COL	D_{OUT}
$\overline{RAS}$ -Only Refresh		L	H	H	X	X	ROW/NA	High-Z
CBR Refresh[3]		H→L	L	L	X	X	X	High-Z

Notes:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
3. At least one of the two $\overline{CAS}$ signals must be active ($\overline{LCAS}$ or $\overline{UCAS}$).

Functional Description

The IS41C16128 is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 17 address bits. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address is latched by the Column Address Strobe ($\overline{CAS}$). $\overline{RAS}$ is used to latch the first nine bits and $\overline{CAS}$ is used to latch the latter nine bits.

The IS41C16128 has two $\overline{CAS}$ controls, $\overline{LCAS}$ and $\overline{UCAS}$. The $\overline{LCAS}$ and $\overline{UCAS}$ inputs internally generates a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 128K x 16 DRAMs. The key difference is that each $\overline{CAS}$ controls its corresponding I/O tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$ and $\overline{RAS}$). $\overline{LCAS}$ controls I/O0 through I/O7 and $\overline{UCAS}$ controls I/O8 through I/O15.

The IS41C16128 $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{LCAS}$ or $\overline{UCAS}$) transitioning LOW and the last transitioning back HIGH. The two $\overline{CAS}$ controls give the IS41C16128 both BYTE READ and BYTE WRITE cycle capabilities.

Memory Cycle

A memory cycle is initiated by bring $\overline{RAS}$ LOW and it is terminated by returning both $\overline{RAS}$ and $\overline{CAS}$ HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. A new cycle must not be initiated until the minimum precharge time t_{RP}, t_{CP} has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of $\overline{CAS}$ or $\overline{OE}$, whichever occurs last, while holding $\overline{WE}$ HIGH. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{AA}, t_{CAC} and t_{OEA} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{CAS}$ and $\overline{WE}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

Refresh Cycle

To retain data, 512 refresh cycles are required in each 8 ms period. There are two ways to refresh the memory.

1. By clocking each of the 512 row addresses (A0 through A8) with $\overline{RAS}$ at least once every 8 ms. Any read, write, read-modify-write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated by the falling edge of $\overline{RAS}$, while holding $\overline{CAS}$ LOW. In $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{CAS}$-before-$\overline{RAS}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Extended Data Out Page Mode

EDO page mode operation permits all 256 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

In EDO page mode, due to the extended data function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one $\overline{RAS}$ cycle, but the performance is equivalent to that of the fast page mode in that case.

Power-On

After application of the V_{CC} supply, an initial pause of 200 µs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ signal).

During power-on, it is recommended that $\overline{RAS}$ track with V_{CC} or be held at a valid V_{IH} to avoid current surges.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameters		Rating	Unit
V_T	Voltage on Any Pin Relative to GND		–1.0 to +7.0	V
V_{CC}	Supply Voltage		–1.0 to +7.0	V
I_{OUT}	Output Current		50	mA
P_D	Power Dissipation		1	W
T_A	Operation Temperature	Com. Ind.	0 to +70 –40 to +85	°C
T_{STG}	Storage Temperature		–55 to +125	°C

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input High Voltage		2.4	—	VCC + 1.0	V
V_{IL}	Input Low Voltage		–1.0	—	+0.8	V
T_A	Ambient Temperature	Com. Ind.	0 –40	— —	+70 +85	°C

CAPACITANCE[1,2]

Symbol	Parameter	Max.	Unit
C_{IN1}	Input Capacitance: A0-A8	5	pF
C_{IN2}	Input Capacitance: $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{IO}	Data Input/Output Capacitance: I/O0-I/O15	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V ± 10%.

ELECTRICAL CHARACTERISTICS[1] (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	Any input 0V $\leq V_{IN} \leq$ 5.5V Other inputs not under test = 0V		–10	10	µA
I_{IO}	Output Leakage Current	Output is disabled (Hi-Z) 0V $\leq V_{OUT} \leq$ 5.5V		–10	10	µA
V_{OH}	Output High Voltage Level	I_{OH} = –2.5 mA		2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = +2.1 mA		—	0.4	V
I_{CC1}	Stand-by Current: TTL	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ $\geq V_{IH}$		—	2	mA
I_{CC2}	Stand-by Current: CMOS	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ $\geq V_{CC}$ – 0.2V		—	1	mA
I_{CC3}	Operating Current: Random Read/Write[2,3,4] Average Power Supply Current	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, Address Cycling, t_{RC} = t_{RC} (min.)	-35	—	230	mA
			-40	—	130	
			-45	—	120	
			-50	—	110	
			-60	—	100	
I_{CC4}	Operating Current: EDO Page Mode[2,3,4] Average Power Supply Current	$\overline{RAS}$ = V_{IL}, $\overline{LCAS}$, $\overline{UCAS}$, Cycling t_{PC} = t_{PC} (min.)	-35	—	220	mA
			-40	—	90	
			-45	—	85	
			-50	—	80	
			-60	—	70	
I_{CC5}	Refresh Current: $\overline{RAS}$ -Only[2,3] Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{LCAS}$, $\overline{UCAS}$ $\geq V_{IH}$ t_{RC} = t_{RC} (min.)	-35	—	230	mA
			-40	—	130	
			-45	—	120	
			-50	—	100	
			-60	—	100	
I_{CC6}	Refresh Current: CBR[2,3,5] Average Power Supply Current	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ Cycling t_{RC} = t_{RC} (min.)	-35	—	230	mA
			-40	—	130	
			-45	—	120	
			-50	—	100	
			-60	—	100	

Notes:

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS[1,2,3,4,5,6] (Recommended Operating Conditions unless otherwise noted.)

		-35		-40		-45		-50		-60		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Random READ or WRITE Cycle Time	60	—	75	—	80	—	90	—	110	—	ns
t_{RAC}	Access Time from $\overline{RAS}$ [6, 7]	—	35	—	40	—	45	—	50	—	60	ns
t_{CAC}	Access Time from $\overline{CAS}$ [6, 8, 15]	—	10	—	12	—	13	—	14	—	15	ns
t_{AA}	Access Time from Column-Address[6]	—	18	—	20	—	22	—	25	—	30	ns
t_{RAS}	$\overline{RAS}$ Pulse Width	35	10K	40	10K	45	10K	50	10K	60	10K	ns
t_{RP}	$\overline{RAS}$ Precharge Time	20	—	25	—	25	—	30	—	40	—	ns
t_{CAS}	$\overline{CAS}$ Pulse Width[26]	6	10K	6	10K	7	10K	8	10K	10	10K	ns
t_{CP}	$\overline{CAS}$ Precharge Time[9, 25]	5	—	5	—	7	—	8	—	10	—	ns
t_{CSH}	$\overline{CAS}$ Hold Time [21]	35	—	40	—	45	—	50	—	60	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time[10, 20]	11	28	17	28	18	32	19	36	20	45	ns
t_{ASR}	Row-Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RAH}	Row-Address Hold Time	6	—	6	—	7	—	8	—	10	—	ns
t_{ASC}	Column-Address Setup Time[20]	0	—	0	—	0	—	0	—	0	—	ns
t_{CAH}	Column-Address Hold Time[20]	6	—	6	—	7	—	8	—	10	—	ns
t_{AR}	Column-Address Hold Time (referenced to $\overline{RAS}$)	30	—	30	—	35	—	40	—	40	—	ns
t_{RAD}	$\overline{RAS}$ to Column-Address Delay Time[11]	12	20	12	20	13	22	14	25	15	30	ns
t_{RAL}	Column-Address to $\overline{RAS}$ Lead Time	18	—	20	—	22	—	25	—	30	—	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RSH}	$\overline{RAS}$ Hold Time[27]	8	—	12	—	13	—	14	—	15	—	ns
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z[15, 29]	3	—	3	—	3	—	3	—	3	—	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time[21]	5	—	5	—	5	—	5	—	5	—	ns
t_{OD}	Output Disable Time[19, 28, 29]	3	15	3	15	3	15	3	15	3	15	ns
t_{OE}	Output Enable Time[15, 16]	—	10	—	10	—	12	—	15	—	15	ns
t_{OEHC}	$\overline{OE}$ HIGH Hold Time from $\overline{CAS}$ HIGH	10	—	10	—	10	—	10	—	10	—	ns
t_{OEP}	$\overline{OE}$ HIGH Pulse Width	10	—	10	—	10	—	10	—	10	—	ns
t_{OES}	$\overline{OE}$ LOW to $\overline{CAS}$ HIGH Setup Time	5	—	5	—	5	—	5	—	5	—	ns
t_{RCS}	Read Command Setup Time[17, 20]	0	—	0	—	0	—	0	—	0	—	ns
t_{RRH}	Read Command Hold Time (referenced to $\overline{RAS}$)[12]	0	—	0	—	0	—	0	—	0	—	ns
t_{RCH}	Read Command Hold Time (referenced to $\overline{CAS}$)[12, 17, 21]	0	—	0	—	0	—	0	—	0	—	ns
t_{WCH}	Write Command Hold Time[17, 27]	5	—	6	—	7	—	8	—	10	—	ns
t_{WCR}	Write Command Hold Time (referenced to $\overline{RAS}$)[17]	30	—	30	—	35	—	40	—	50	—	ns
t_{WP}	Write Command Pulse Width[17]	5	—	6	—	7	—	8	—	10	—	ns
t_{WPZ}	$\overline{WE}$ Pulse Widths to Disable Outputs	10	—	10	—	10	—	10	—	10	—	ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time[17]	8	—	12	—	13	—	14	—	15	—	ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time[17, 21]	8	—	12	—	13	—	14	—	15	—	ns
t_{WCS}	Write Command Setup Time[14, 17, 20]	0	—	0	—	0	—	0	—	0	—	ns
t_{DHR}	Data-in Hold Time (referenced to $\overline{RAS}$)	30	—	30	—	35	—	40	—	40	—	ns

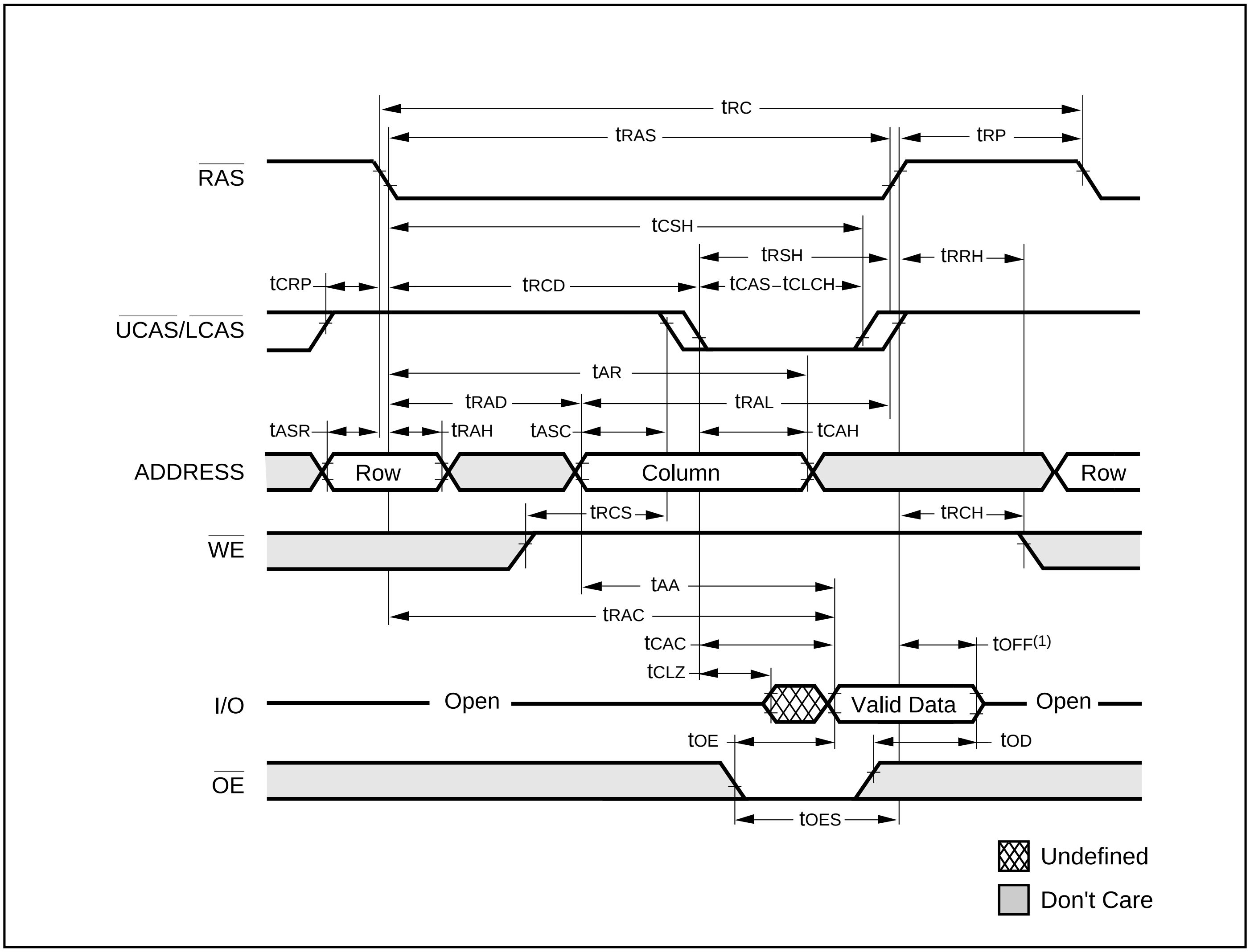
AC CHARACTERISTICS (Continued)[1,2,3,4,5,6] (Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-35 Min.	-35 Max.	-40 Min.	-40 Max.	-45 Min.	-45 Max.	-50 Min.	-50 Max.	-60 Min.	-60 Max.	Units
t_{ACH}	Column-Address Setup Time to $\overline{CAS}$ Precharge during WRITE Cycle	15	—	15	—	15	—	15	—	15	—	ns
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle[18]	8	—	8	—	8	—	10	—	15	—	ns
t_{DS}	Data-In Setup Time[15, 22]	0	—	0	—	0	—	0	—	0	—	ns
t_{DH}	Data-In Hold Time[15, 22]	6	—	6	—	7	—	8	—	10	—	ns
t_{RWC}	READ-MODIFY-WRITE Cycle Time	80	—	100	—	115	—	125	—	140	—	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle[14]	45	—	50	—	60	—	70	—	80	—	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time[14, 20]	25	—	30	—	32	—	34	—	36	—	ns
t_{AWD}	Column-Address to $\overline{WE}$ Delay Time[14]	30	—	30	—	40	—	42	—	49	—	ns
t_{PC}	EDO Page Mode READ or WRITE Cycle Time[24]	12	—	15	—	17	—	20	—	25	—	ns
t_{RASP}	$\overline{RAS}$ Pulse Width in EDO Page Mode	35	100K	40	100K	45	100K	50	100K	60	100K	ns
t_{CPA}	Access Time from $\overline{CAS}$ Precharge[15]	—	21	—	23	—	25	—	27	—	34	ns
t_{PRWC}	EDO Page Mode READ-WRITE Cycle Time[24]	40	—	45	—	46	—	47	—	56	—	ns
t_{COH}	Data Output Hold after $\overline{CAS}$ LOW	3	—	3	—	3	—	3	—	3	—	ns
t_{OFF}	Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$ [13,15,19, 29]	3	15	3	15	3	15	3	15	3	15	ns
t_{WHZ}	Output Disable Delay from $\overline{WE}$	3	15	3	15	3	15	3	15	3	15	ns
t_{CLCH}	Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ returning HIGH[23]	10	—	10	—	10	—	10	—	10	—	ns
t_{CSR}	$\overline{CAS}$ Setup Time (CBR REFRESH)[30, 20]	8	—	10	—	10	—	10	—	10	—	ns
t_{CHR}	$\overline{CAS}$ Hold Time (CBR REFRESH)[30, 21]	8	—	10	—	10	—	10	—	10	—	ns
t_{ORD}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle	0	—	0	—	0	—	0	—	0	—	ns
t_{REF}	Refresh Period (512 Cycles)	—	8	—	8	—	8	—	8	—	8	ms
t_T	Transition Time (Rise or Fall)[2, 3]	1	50	1	50	1	50	1	50	1	50	ns

Notes:

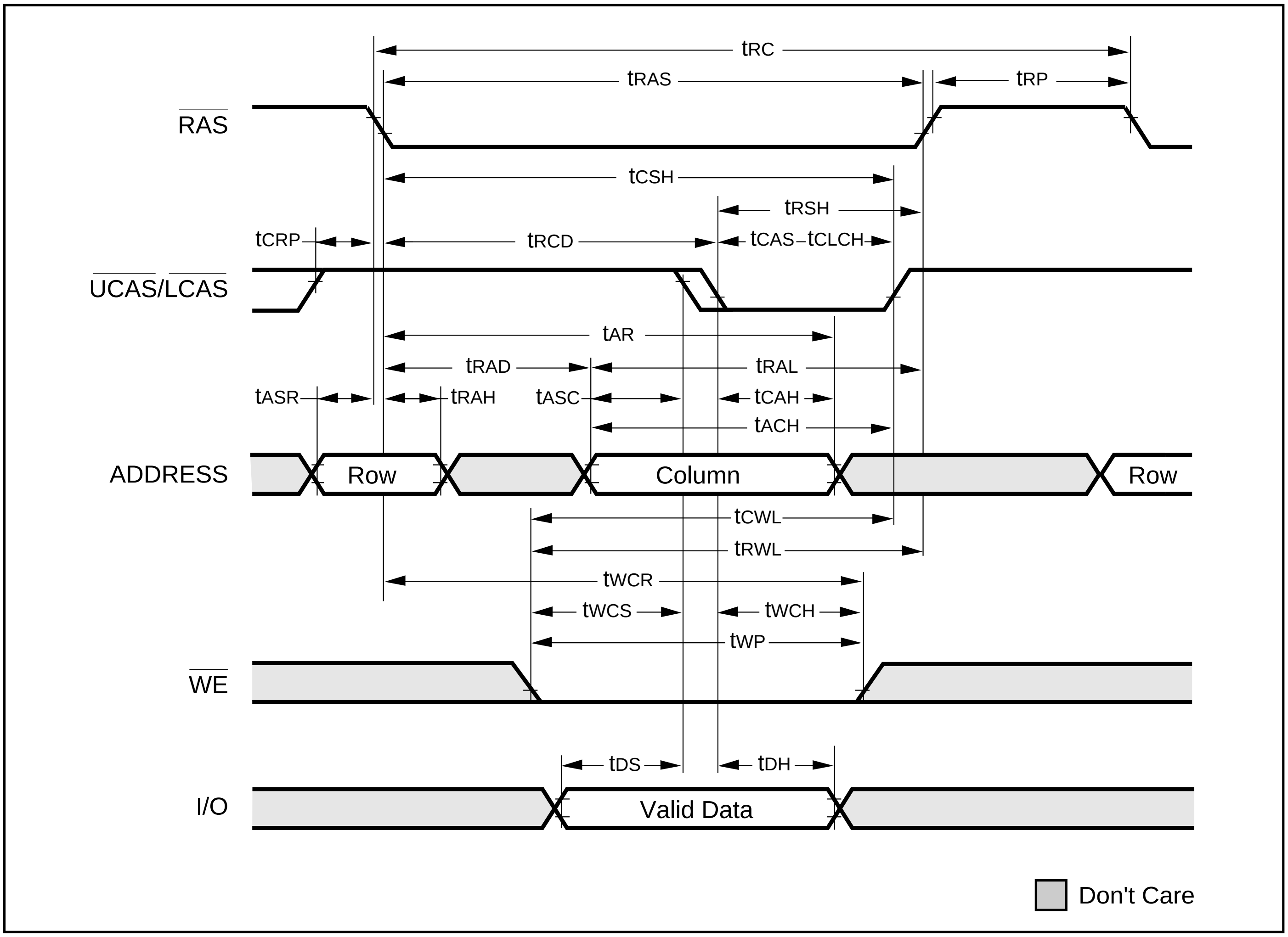
1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycle ($\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
5. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (MAX).
9. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed for t_{CP}.
10. Operation with the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, access time is controlled exclusively by t_{CAC}.
11. Operation within the t_{RAD} (MAX) limit ensures that t_{RCD} (MAX) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, access time is controlled exclusively by t_{AA}.
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
14. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$ -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input, I/O0-I/O7 by $\overline{LCAS}$ and I/O8-I/O15 by $\overline{UCAS}$.
16. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, I/O goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{WE}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. The first $\chi\overline{CAS}$ edge to transition LOW.
21. The last $\chi\overline{CAS}$ edge to transition HIGH.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling $\chi\overline{CAS}$ edge to first rising $\chi\overline{CAS}$ edge.
24. Last rising $\chi\overline{CAS}$ edge to next cycle's last rising $\chi\overline{CAS}$ edge.
25. Last rising $\chi\overline{CAS}$ edge to first falling $\chi\overline{CAS}$ edge.
26. Each $\chi\overline{CAS}$ must meet minimum pulse width.
27. Last $\chi\overline{CAS}$ to go LOW.
28. I/Os controlled, regardless $\overline{UCAS}$ and $\overline{LCAS}$.
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

READ CYCLE

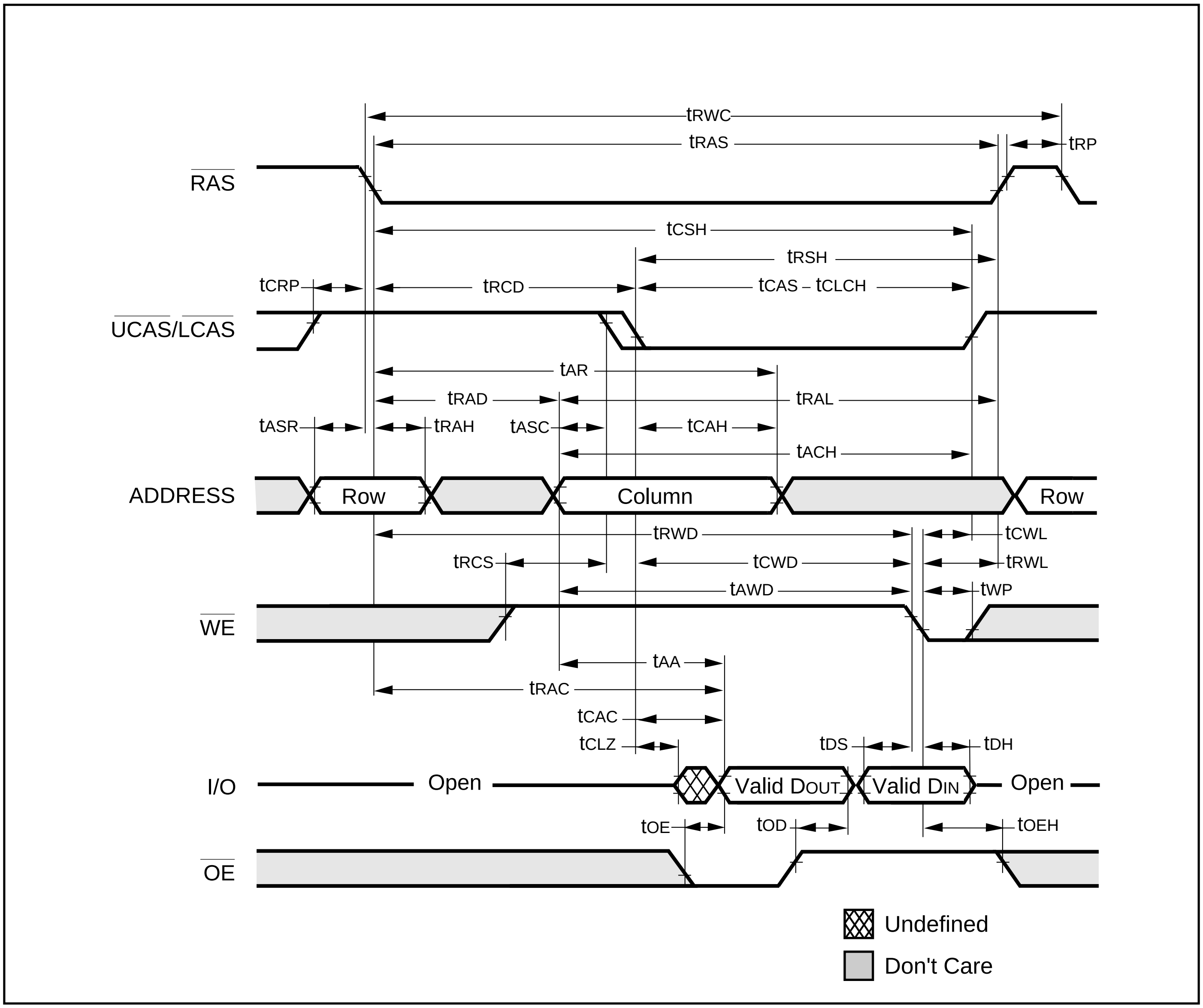


Note:
1. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

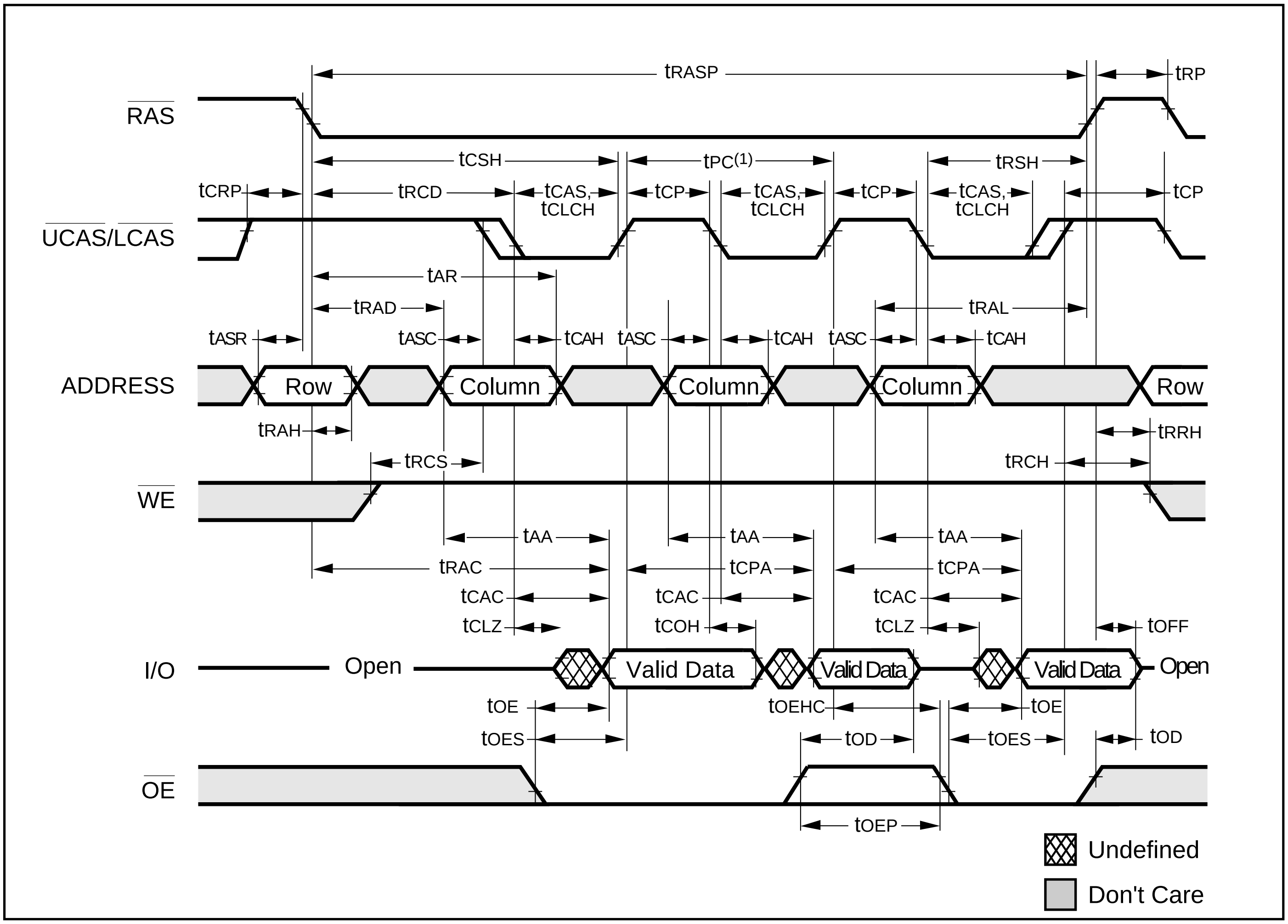
EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



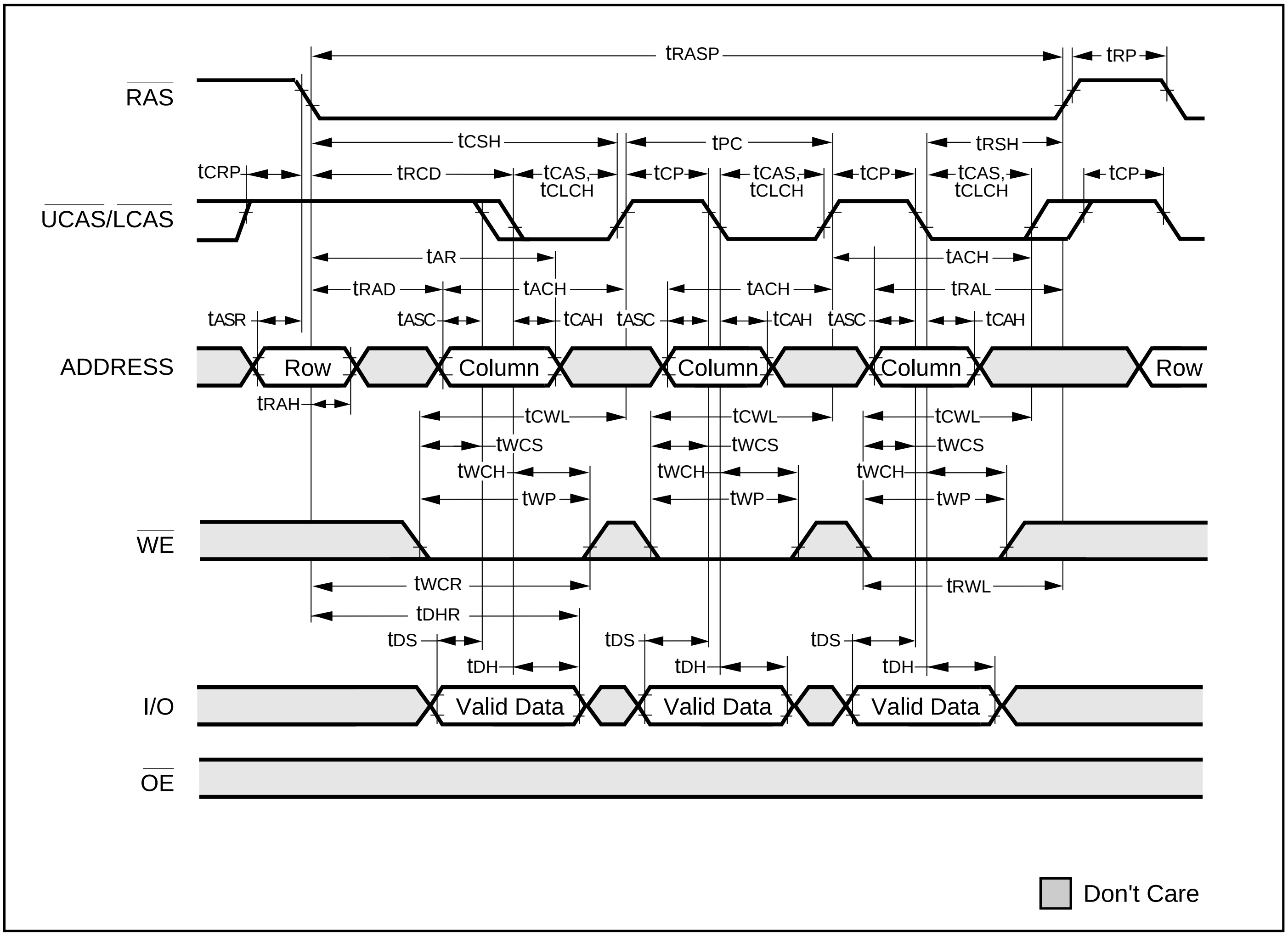
EDO-PAGE-MODE READ CYCLE



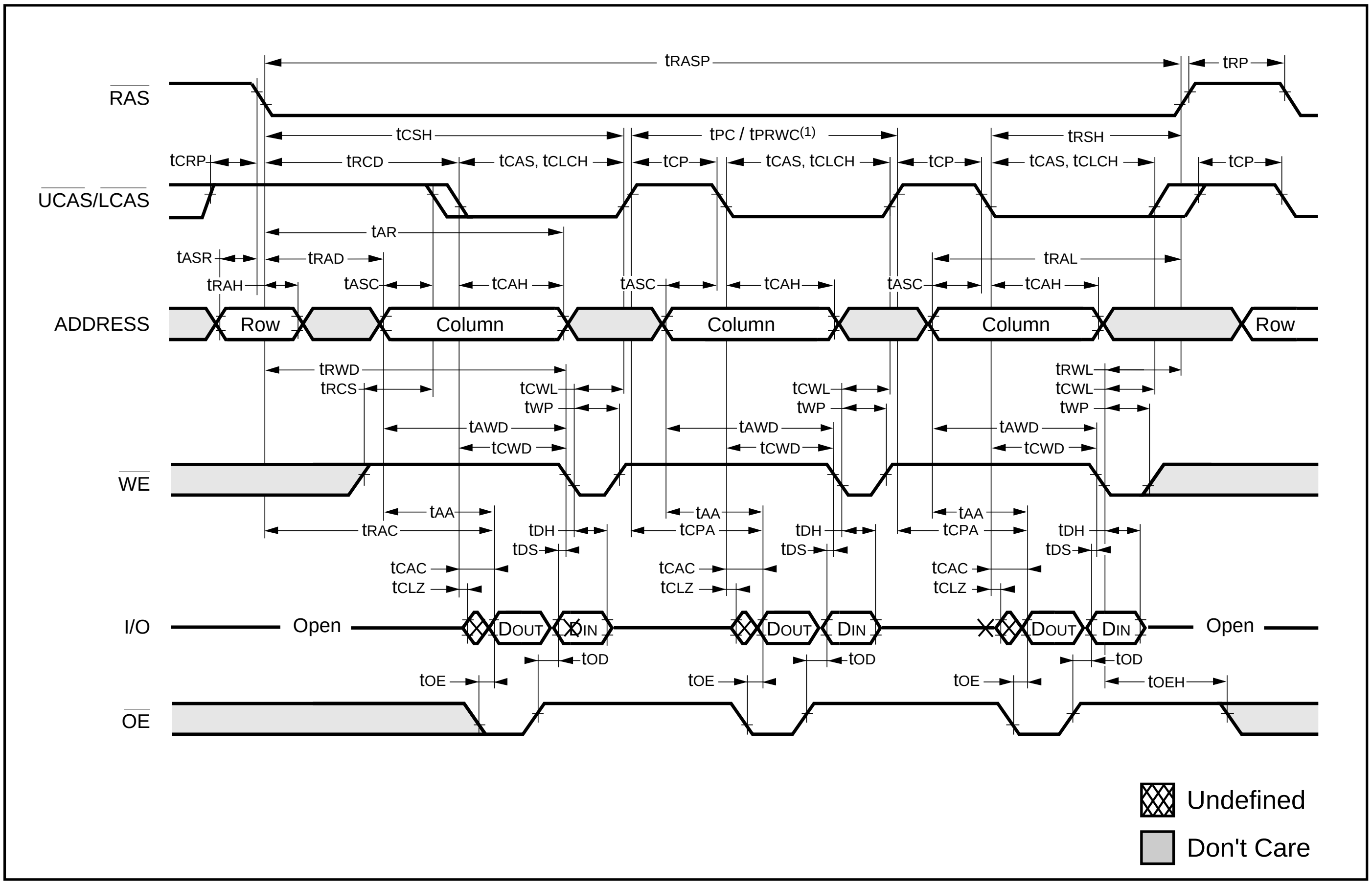
Note:

1. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specifications.

EDO-PAGE-MODE EARLY-WRITE CYCLE



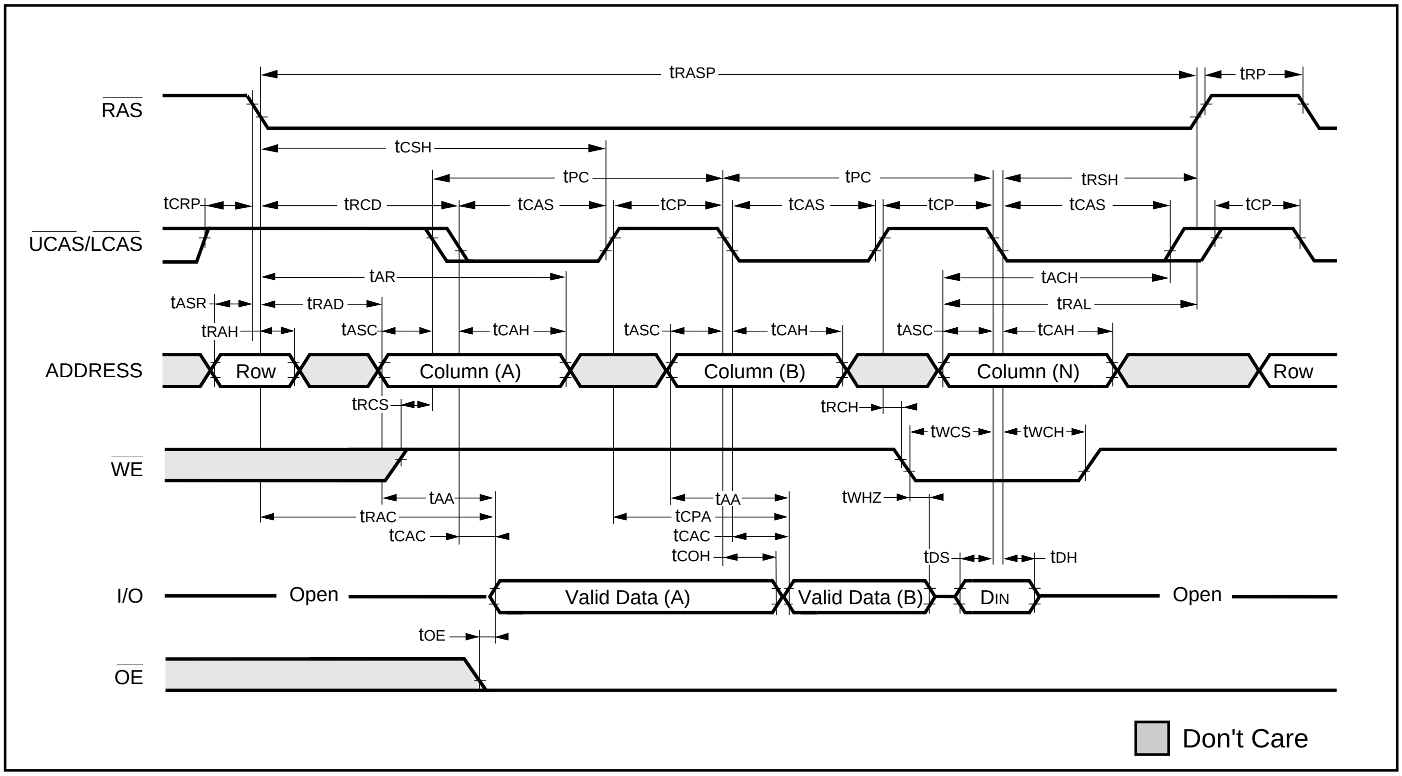
EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



Note:

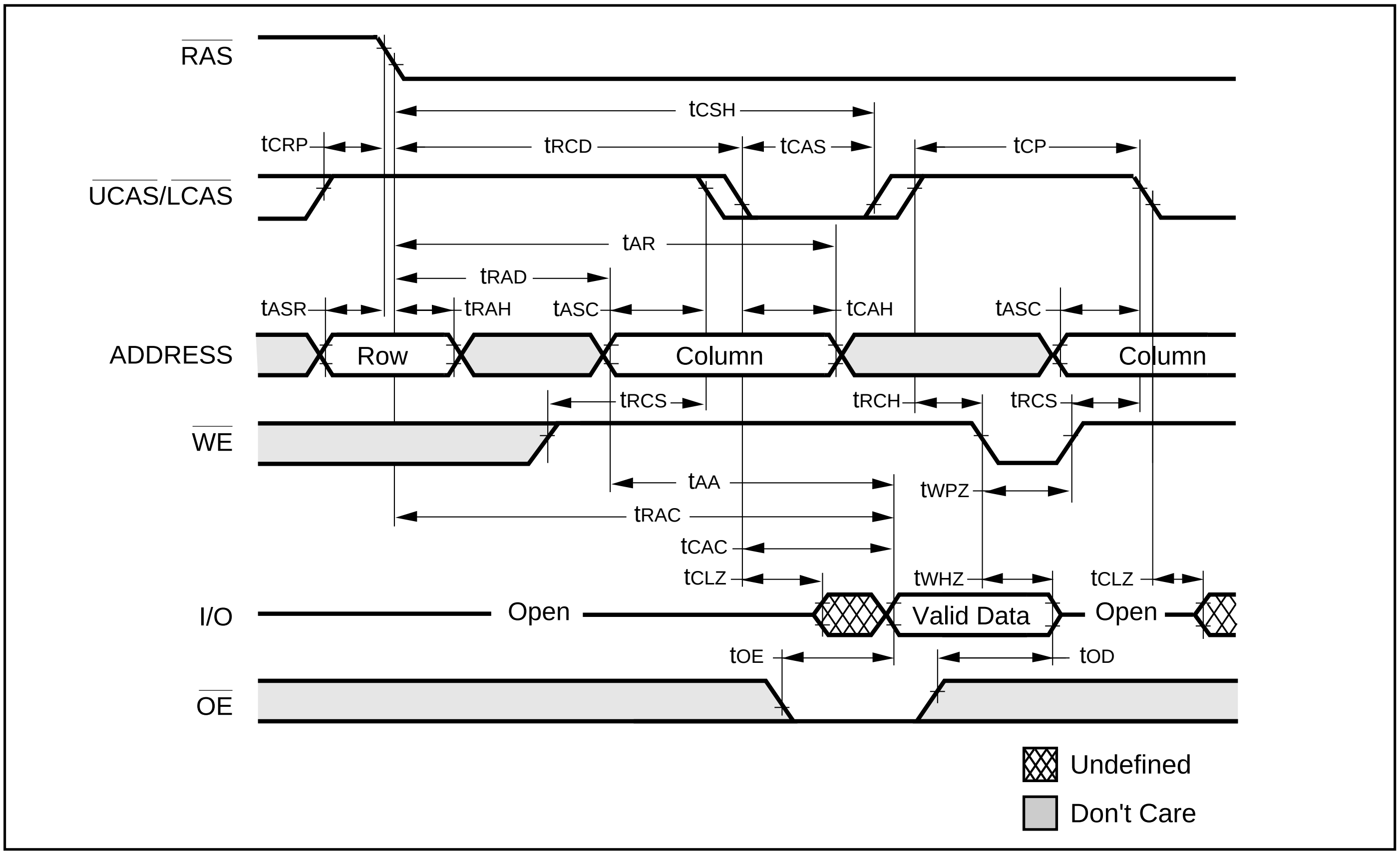
1. tPC can be measured from falling edge of CAS to falling edge of CAS , or from rising edge of CAS to rising edge of CAS . Both measurements must meet the tPC specifications.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Psuedo READ-MODIFY WRITE)

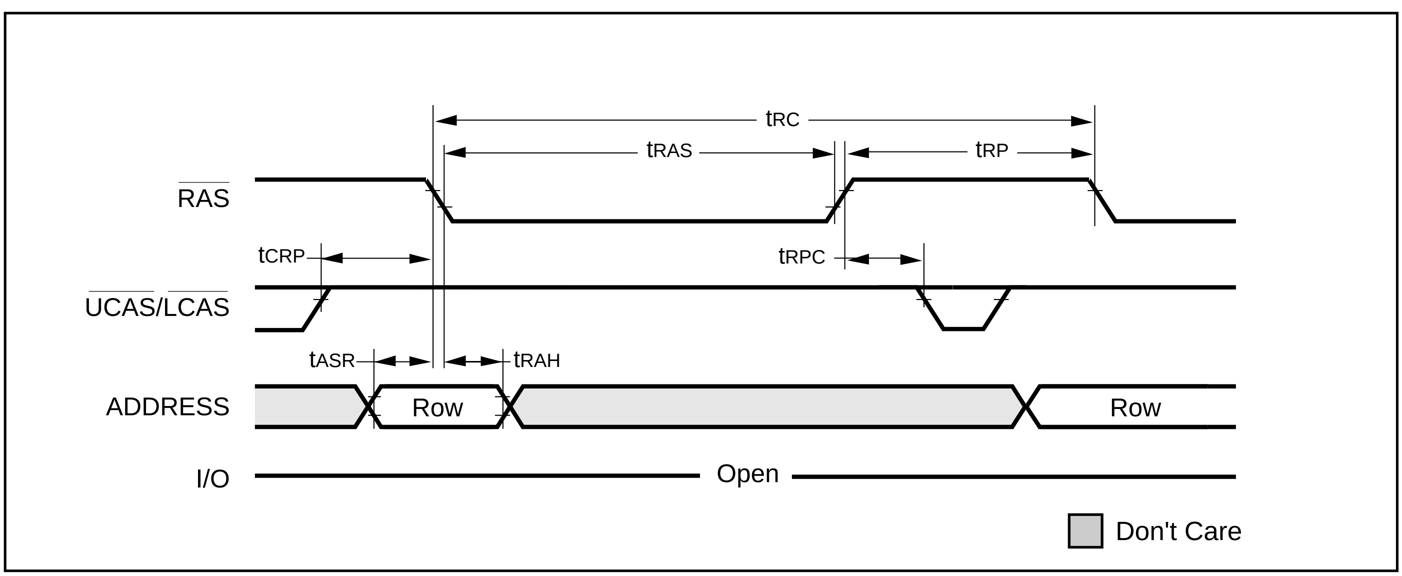


AC WAVEFORMS

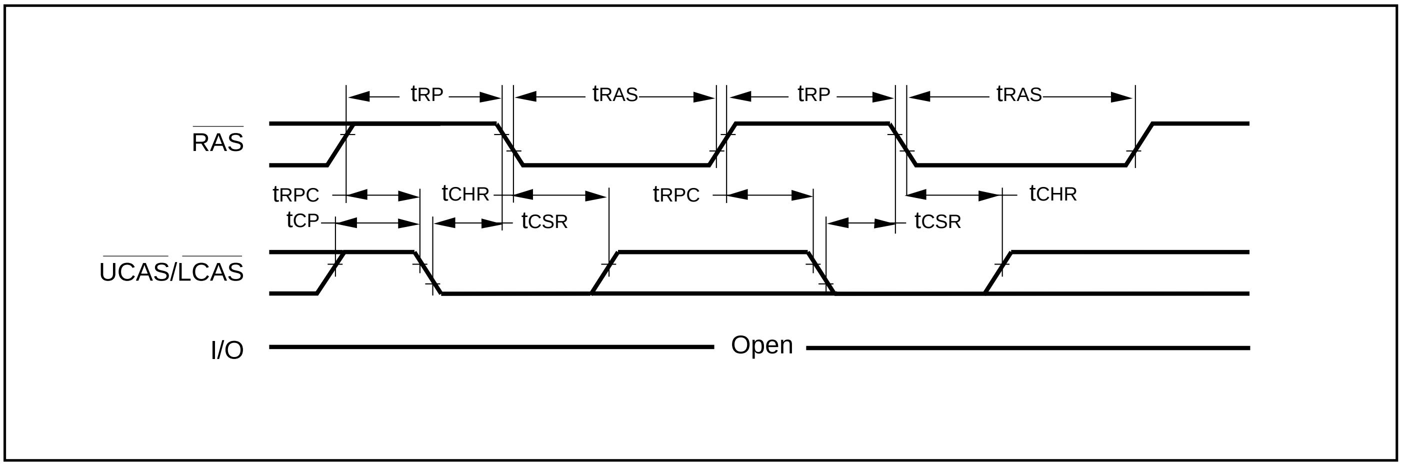
READ CYCLE (With $\overline{WE}$ -Controlled Disable)



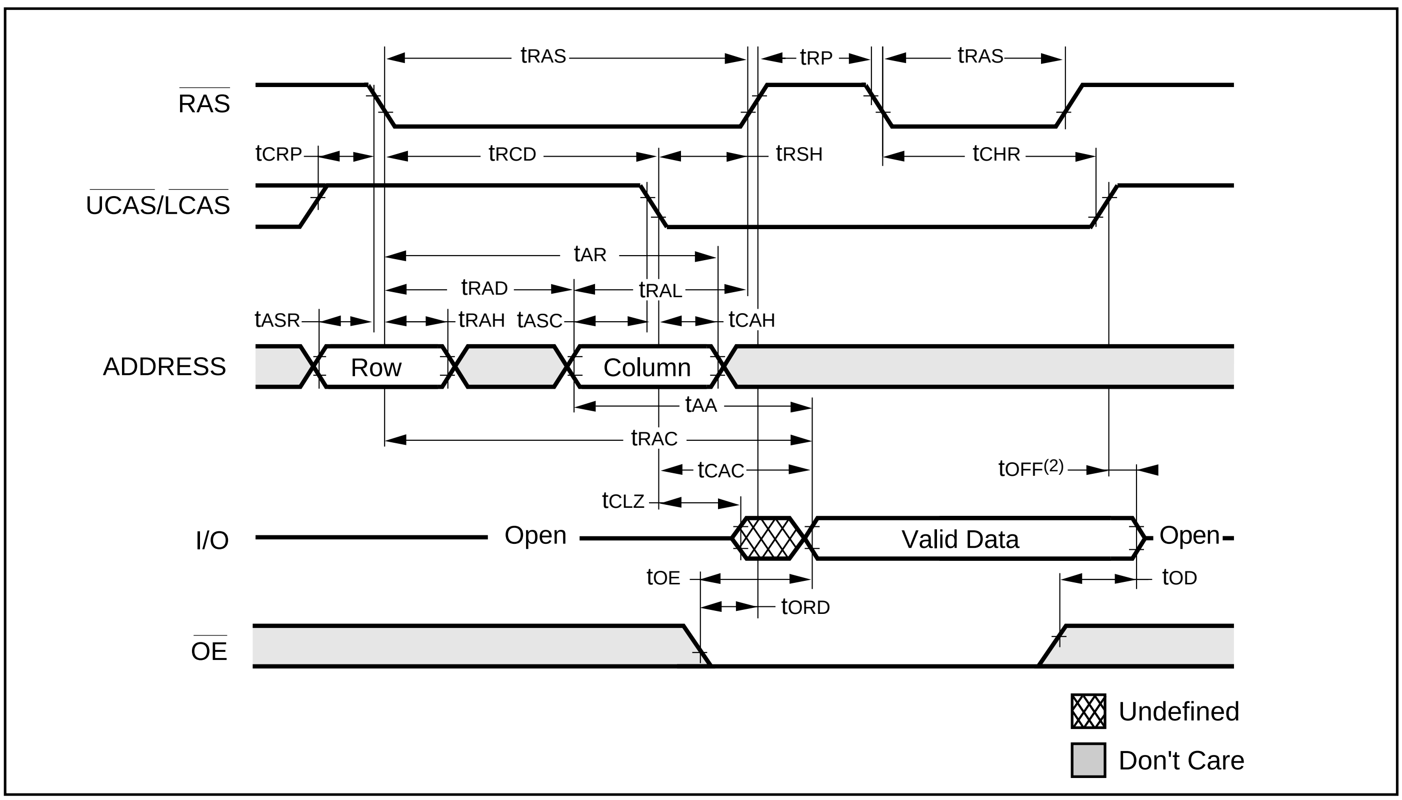
$\overline{RAS}$ -ONLY REFRESH CYCLE ($\overline{OE}$, $\overline{WE}$ = DON'T CARE)



CBR REFRESH CYCLE (Addresses; WE , OE = DON'T CARE)



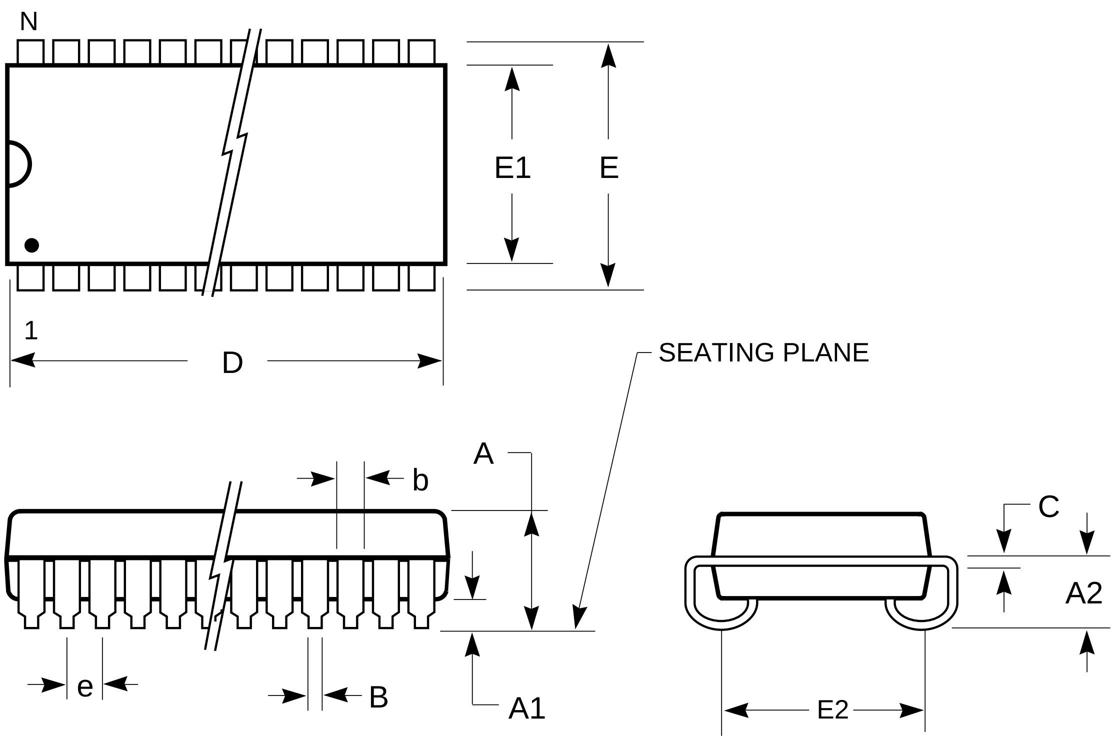
HIDDEN REFRESH CYCLE (WE = HIGH; OE = LOW)(1)



Notes:
1. A Hidden Refresh may also be performed after a Write Cycle. In this case, WE = LOW and OE = HIGH.
2. tOFF is referenced from rising edge of RAS or CAS , whichever occurs last.

400-MIL PLASTIC SOJ

Package Code: K

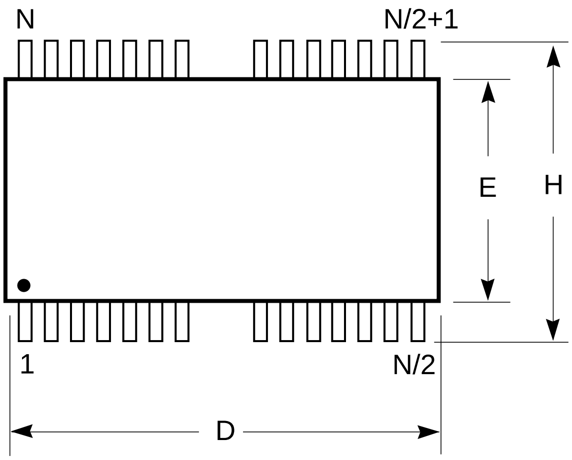


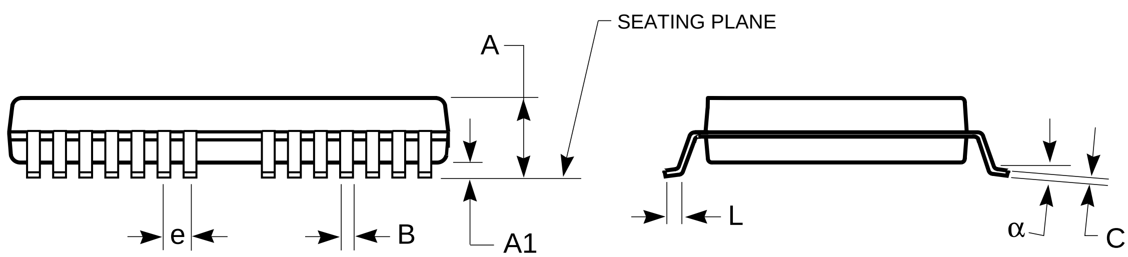
400-mil Plastic SOJ (K)				
	Inches		Millimeters	
Symbol	Min	Max	Min	Max
Ref. Std.				
N		40		
A	—	0.144	—	3.66
A1	0.025	—	0.66	—
A2	0.082	—	2.08	—
B	0.015	0.019	0.38	0.48
b	0.026	0.032	0.66	0.81
C	0.007	0.013	0.18	0.33
D	1.020	1.030	25.91	26.16
E	0.430	0.450	10.92	11.43
E1	0.395	0.405	10.03	10.28
E2	0.346	0.386	8.79	9.80
e	0.050 BSC		1.27 BSC	

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PLASTIC TSOP

Package Code: T (Type 2)





Plastic TSOP (T - Type II)				
	Inches		Millimeters	
Symbol	Min	Max	Min	Max
Ref. Std.				
N	40/44			
A	0.039	0.047	1.00	1.20
A1	0.002	0.008	0.05	0.20
B	0.012	0.016	0.30	0.40
C	0.0047	0.0083	0.12	0.21
D	0.721	0.729	18.313	18.517
E	0.462	0.470	11.735	11.938
e	0.0315 BSC		0.800 BSC	
H	0.396	0.404	10.058	10.262
L	0.017	0.023	0.432	0.584
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Speed (ns)	Order Part No.	Package
35	IS41C16128-35K	400-mil SOJ
35	IS41C16128-35T	400-mil TSOP (Type 2)
40	IS41C16128-40K	400-mil SOJ
40	IS41C16128-40T	400-mil TSOP (Type 2)
45	IS41C16128-45K	400-mil SOJ
45	IS41C16128-45T	400-mil TSOP (Type 2)
50	IS41C16128-50K	400-mil SOJ
50	IS41C16128-50T	400-mil TSOP (Type 2)
60	IS41C16128-60K	400-mil SOJ
60	IS41C16128-60T	400-mil TSOP (Type 2)

Industrial Range: –40°C to 85°C

Speed (ns)	Order Part No.	Package
35	IS41C16128-35KI	400-mil SOJ
35	IS41C16128-35TI	400-mil TSOP (Type 2)
40	IS41C16128-40KI	400-mil SOJ
40	IS41C16128-40TI	400-mil TSOP (Type 2)
45	IS41C16128-45KI	400-mil SOJ
45	IS41C16128-45TI	400-mil TSOP (Type 2)
50	IS41C16128-50KI	400-mil SOJ
50	IS41C16128-50TI	400-mil TSOP (Type 2)
60	IS41C16128-60KI	400-mil SOJ
60	IS41C16128-60TI	400-mil TSOP (Type 2)

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