CAN FD Bus Transceiver with LDO

GENERAL DESCRIPTION

The IS32IO1163 is a CAN FD transceiver integrated with 5V LDO. The CAN FD transceiver meets ISO 11898-2/5 requirements and supports the low power mode specified in ISO 11898-6 with local/remote wakeup capability. The CAN FD allows up to 5Mbps data rate.

The built-in LDO is 5V and can supply up to 100mA external loads such as MCU, sensors, or actuators. IS32IO1163A is 5V I/O compatible (its VIO pin is internally shorted to V1). IS32IO1163B supports independent VIO through pin 5 and can be 3.3V IO compatible.

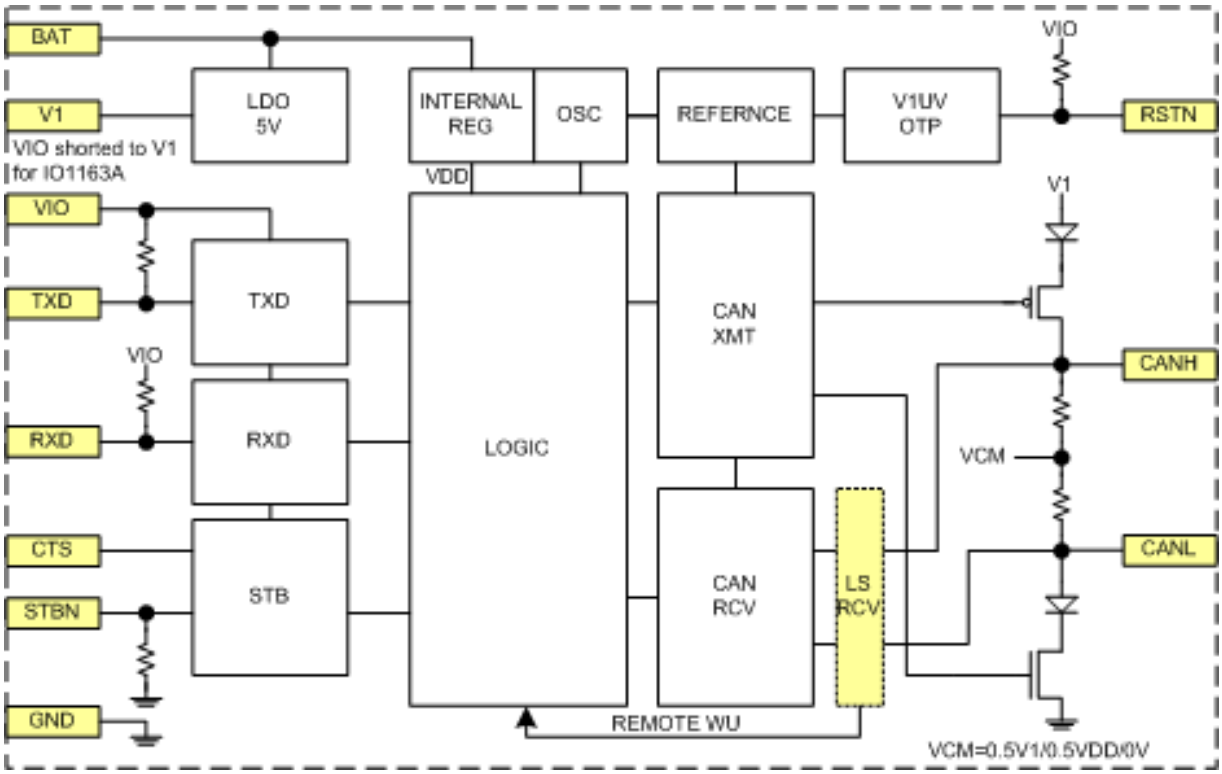
IS32IO1163 is in a standard eTSSOP-14 and FCDFN-14 packages.

APPLICATIONS

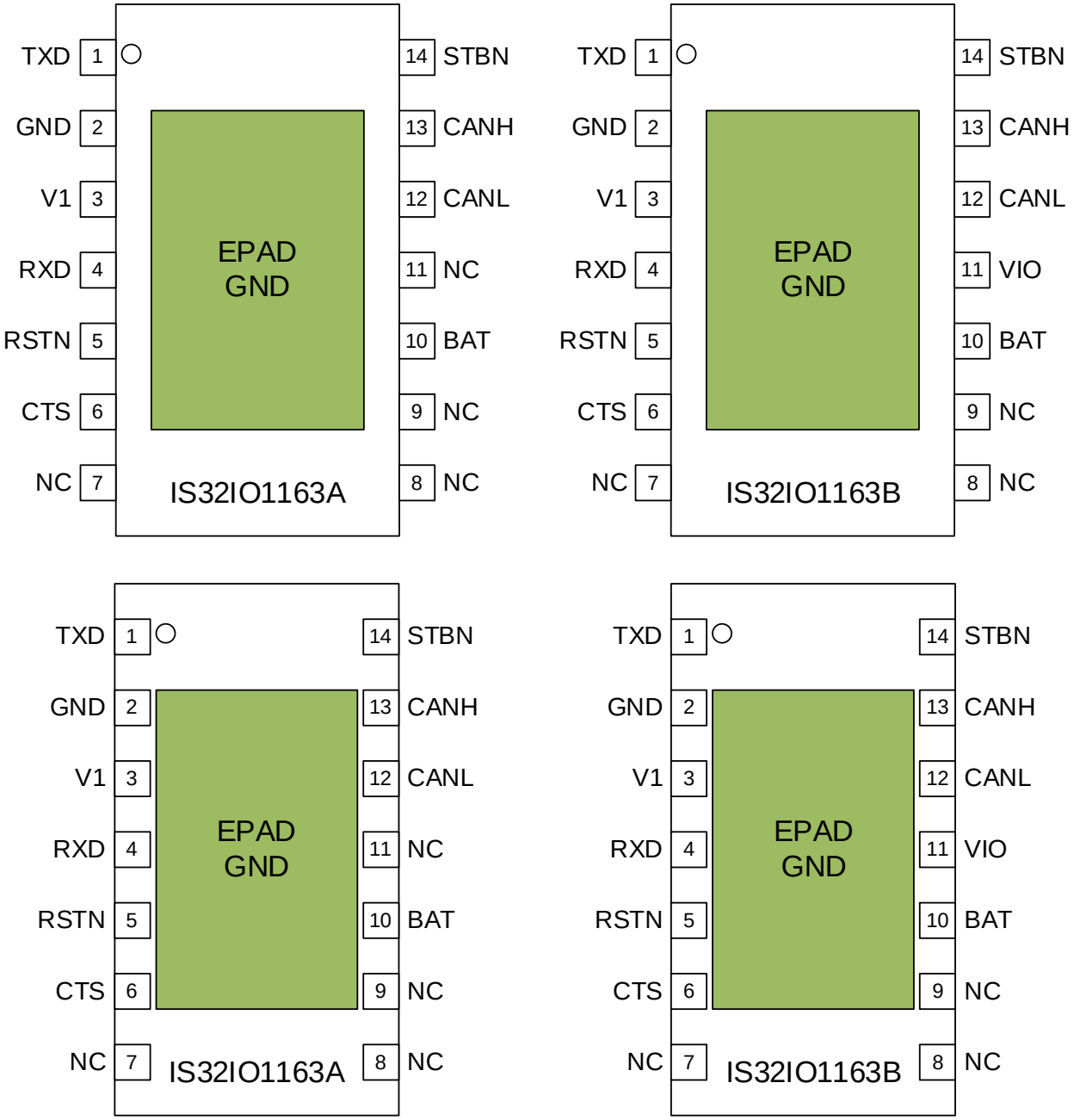
- Automotive
- Industrial Networks

FEATURES

- Battery voltage 6.3V to 32V
- Compliant to ISO 11898-2/5
- ISO 11898-6 low power mode with remote wake-up capability
- High-speed CAN FD data up to 5Mbps
- +/- 8KV HBM ESD for CANH/CANL pins
- Built-in LDO V1 to supply external circuits
  - 5V nominal output with typical +/- 3% accuracy
  - Supply up to 100mA
  - 150mA current limit
  - Under-voltage detection
- Optimized for low electromagnetic emission/ immunity (EME/EMI)
- +/-12V wide range common mode range
- Bus connections are fully floating when BAT loses power
- VIO input allows 5V/3.3V IO interface
- Over temperature shut-down and recovery
- Bidirectional reset pin
- TSSOP-14 with exposed pad (eTSSOP), and flip chip DFN-14 (FCDFN-14) packages
- ROHS & Halogen-Free compliant package
- TSCA compliance
- AEC-Q100 qualification
- IS32IO1163A VIO internal connects to V1
- IS32IO1163B Independent VIO pin



PIN OUT



TOP VIEW

EPAD should be connected to GND

PIN DESCRIPTION

PIN #	NAME	I/O	DESCRIPTION
1	TXD	I	Transmit data input. TXD has an internal pull-up resistor to VIO.
2	GND	G	Ground power supply.
3	V1	O/P	5V LDO output, the output also serves as CAN transmit circuit supply.
4	RXD	O	Receive data output. Also indicates the remote wakeup status. RXD has an internal pull-up resistor to VIO in CAN offline and CAN offline bias modes.
5	RSTN	I/O	Reset input/output. RSTN is pulled low when V1 is under-voltage or over-temperature. If pulled down externally, the transceiver will be put in reset states. RSTN has an internal pull-up resistor to VIO.
6	CTS	O	Transceiver status. CTS=high when the transceiver is in normal mode and ready.
7	NC	-	No connection
8	NC	-	No connection
9	NC	-	No connection
10	BAT	P	Positive supply +6.3V to +32V
11	NC/VIO	-/P	NC for IS32IO1163A and VIO is shorted internally to V1. VIO power for IS32IO1163B for 3.0V to 5.5V IO interface supply.
12	CANL	I/O	CAN bus low.
13	CANH	I/O	CAN bus high.
14	STBN	I	Standby control. STBN=0 puts the transceiver in the standby state. STBN has an internal pull-down resistor.

Pin Functional Descriptions

IS32IO1163 integrates the physical layer function for conventional CAN and FD CAN bus applications. It is compliant with ISO 11898-2:2016.

Supply Pin (BAT)

BAT is the primary supply for the internal circuits and CAN bus front-end. It must be supplied with a voltage of 6.3V to 32V. The maximum BAT supply ramp up and down time during switching on/off should be less than 50ms to ensure correct reset behavior. If BAT is lost, the bus pins present no load on the bus.

LDO5V Output Pin (V1)

LDO5V is always enabled when BAT supply is present except in over-temperature conditions. V1 should have external decoupling capacitors of 1uF and 0.1uF. V1 supplies the CAN transceiver circuit during normal and CAN offline bias modes. In addition, V1 can provide up to 100mA for external circuits. When using V1 for external supply, the thermal impact must be taken into consideration especially at high BAT voltage as the heat dissipation increases linearly as BAT voltage increases.

V1 output has typical output accuracy of +/- 3% (4.85V to 5.15V). V1 has under voltage detection at 4.3V and that will force RSTN low if under voltage is detected.

Supply Pin (VIO)

VIO is used for interface logic supply. It can be supplied with a voltage less or equal to V1. In IS32IO1163A, VIO is shorted to V1 internally.

Ground Pin (VSS)

This is the negative supply.

Reset Pin (RSTN)

RSTN is a bi-directional open-drain pin and has an internal pull-up resistance to VIO. RSTN is forced low by IS32IO1163 when V1 is under-voltage or over-temperature. RSTN can also be forced to low externally. If RSTN=0, IS32IO1163 enters reset mode which causes CAN to enter CAN Offline state.

Mode Control Pin (STBN)

STBN controls the operation mode. STBN has an internal pull-down resistance.

If STBN=1, normal transceiver operation is enabled. STBN=0, the transceiver is in standby low power mode (includes CAN offline or CAN offline bias modes.). In standby mode, only the low-power receiver front-end is in operation to detect any remote wakeup event.

The transition time from standby to normal mode is around 80usec. External MCU should allow at least 100usec to start transmission when exiting standby mode.

Transmit Data Pin (TXD)

TXD is the input pin for transmitting data. TXD has an internal pull-up resistance to VIO.

TXD=1 is for recessive bus state and TXD=0 for dominant bus state. TXD=0 has a timeout mechanism to prevent rogue behavior. When transitioning from standby to normal mode, TXD=1 must be met first for further normal transmission of dominant output.

Receive Data Pin (RXD)

RXD is the output pin of receiving data.

RXD=1 reflects recessive bus state and RXD=0 for dominant bus state in normal mode.

In standby mode, only low-power receiver front-end is enabled and RXD is kept high. When a remote wakeup frame is detected, RXD is forced low and latched. Host can monitor RXD state during standby mode for detecting bus wakeup.

When transitioning from standby to normal mode, RXD may see output glitches due to output handover from a low-power receiver circuit to a high-speed receiver circuit.

Status Pin (CTS)

CTS indicates the status of CAN transceiver. CTS is high to indicate to host that the transceiver is in normal active mode that data can be transmitted and received to and from CAN bus. CTS is low when V1 is under-voltage or TXD=0 timeout in normal mode, and CTS is also low in standby mode.

Bus Pin (CANH and CANL)

CANH and CANL are CAN bus pins. Typically, the CAN bus is terminated at both ends with 120 Ohm termination resistors. And the effective 120 Ohm is implemented using two 60 Ohm in series with a center tap connected to a split voltage typically at 2.5V.

Within IS32IO1163, the CANH and CANL pins are also internally biased to VCM through two 15K Ohm resistors separately. VCM is ½ V1 in CAN active, VCM is ½VDD (internal 5V supply) in CAN offline bias mode, and VCM is 0V in CAN offline mode.

In normal operation (CAN active mode), when transmitting a dominant output, CANH and CANL are separately pulled up and down by current sources that produce positive voltage swing across CANH and CANL for dominant level. For recessive output, the current sources are both turned off, so CANH has the same level of CANL by the termination resistor. The driving of the current sources has edge rate control for better EMI performance. Both CANH and CANL have reverse-blocking diodes for isolation.

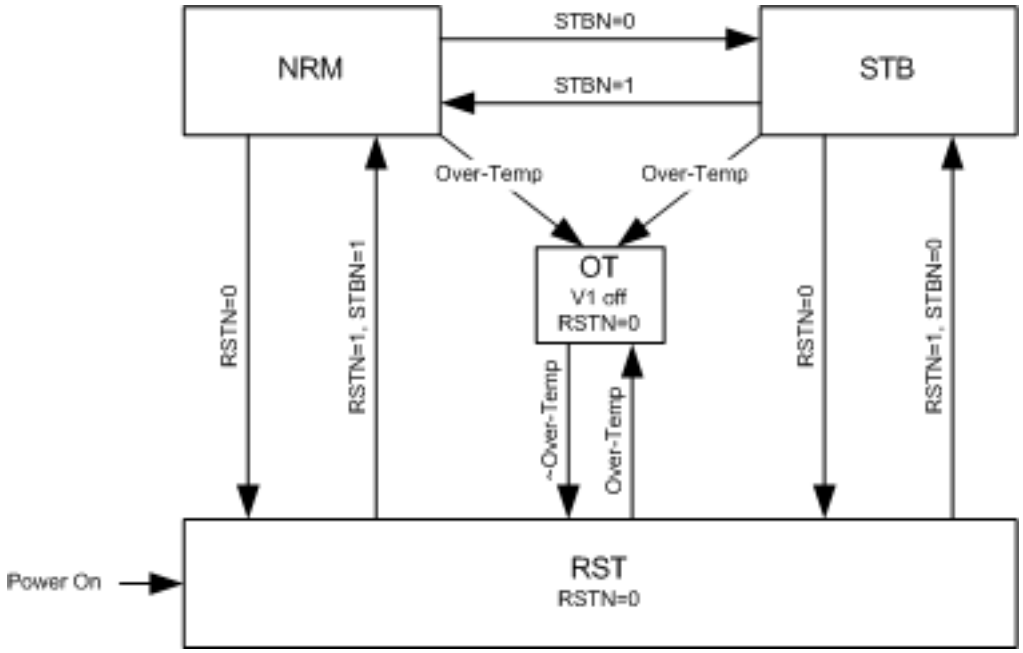
For CAN receive in normal operation, a high-speed receiver detects a single-end threshold (0.5V to 0.9V) of (CANH-CAHL) to determine if the bus is in the dominant state. The receiver output is then sent to RXD buffer.

In standby mode (CAN offline and CAN offline bias modes), the transmitter and the high-speed receiver are disabled to save power. A low-power receiver is active in the standby mode with similar characteristics for the purpose of detecting wake-up events on the bus.

1. Function Descriptions

1.1 Device Operation States

IS32IO1163 operation can be described in the following simple state diagram consisting of only four states, Normal (NRM), Standby (STB), Reset (RST), and Over-temperature (OT) states.



IS32IO1163 is in the normal state when the transceiver is ready for operation. Standby state is a power conservation mode that only the low-power receiver is active to detect remote wakeup. Transition between normal state and standby state is by STBN input level.

IS32IO1163 enters reset mode whenever RSTN is 0. There are several conditions or events resulting in RSTN=0, which include under-voltage, over-temperature, as well as forced low externally. When these conditions are absent, IS32IO1163 exits reset state to normal or standby states depending on STBN input. Both receive and transmit functions of the transceiver are disabled in reset state. When exiting reset state, RSTN=0 is always extended by 20 to 25msec.

If over-temperature occurs, all states transit to the over-temperature state. In this state, V1 and the transceiver functions are disabled to reduce power consumption, and RSTN is also pulled low. IS32IO1163 remains in OT state under over-temperature conditions. Recovering from over-temperature state, IS32IO1163 enters to reset state and then transits to NRM or STB states when RSTN is released from low.

Please note the state machine is clocked by an on-chip 100KHz oscillator. The transition time between states can take up to 80usec considering the enable/disable settling time of the analog circuits.

1.2 CAN Operation States

IS32IO1163 implements ISO 11898-6 low power mode with remote wake-up capability. This can be described by the following state diagram. Please note this state machine is supervised by the device operation states. In essence, CAN ACTIVE is only possible in NRM state, and CAN OFFLINE/CAN OFFLINE BIAS are under STB state, while RST and OT states correspond to CAN OFF.

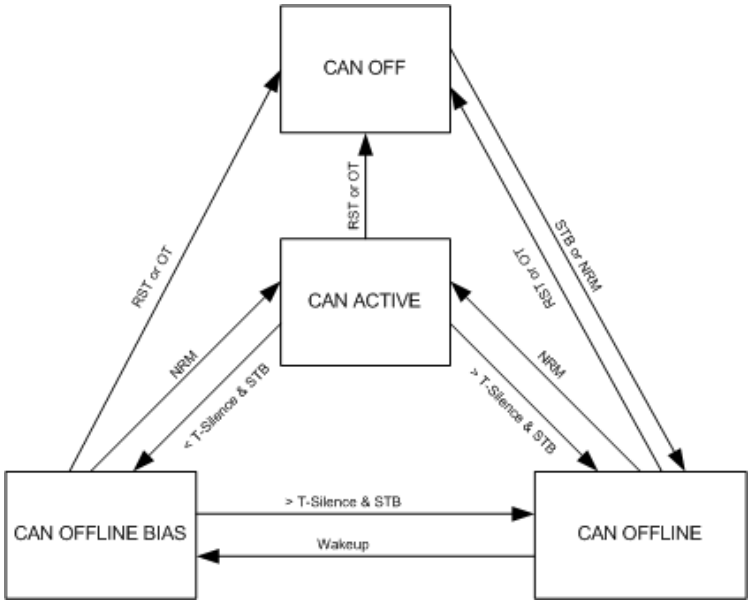
CAN active state is the normal operational state. In this state, the transceiver is enabled and both high-speed receiver and transmitter are enabled. There is a CAN activity timer that monitors CAN bus idle time out for $T_{SILENCE}$. This timer is enabled in CAN active and CAN offline bias states and disabled in CAN offline and off states. If STB=1, depending on $T_{SILENCE}$ flag, CAN active state transits to either CAN offline bias or offline state.

CAN offline state is the low-power state that only the low-power receiver front-end is enabled to detect remote wakeup conditions. If remote wakeup is detected, RXD is forced low and transits to CAN offline bias state.

CAN offline bias state is an intermediate state between CAN offline and CAN active state. When entering from CAN active state if STB=1 and < $T_{SILENCE}$, CAN offline bias state presides until $T_{SILENCE}$ is expired and then transits to CAN offline state. Similarly, CAN offline bias state is entered from CAN offline state after wakeup is detected. It only stays in CAN offline bias state for $T_{SILENCE}$ then back to CAN offline state unless STB is low.

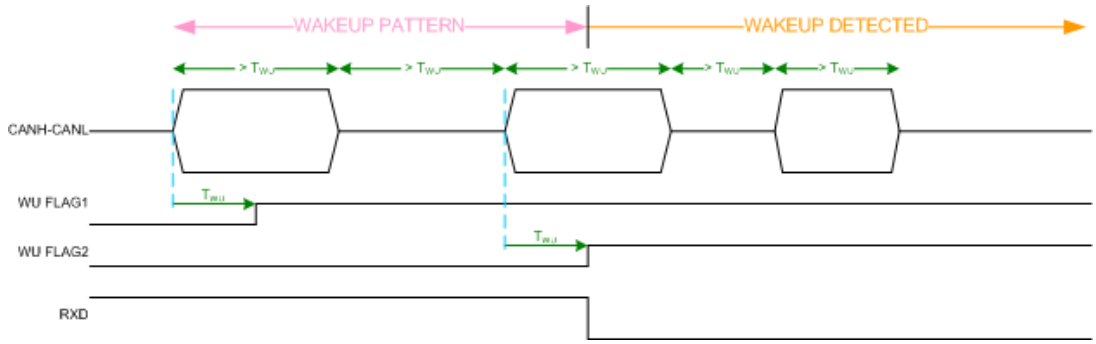
CAN off state is a safe state that is destined from all other states if RST or OT condition occurs. It remains in CAN off state unless RST and OT conditions are removed. In this state, V1 is off, the transceiver is disabled, and

CANH/CANL bus pins are forced into a floating state avoiding any load to the bus. When RST or OT is not present, CAN off state always transits to CAN offline state.



1.3 Remote Wakeup Detection

In both CAN offline or offline bias states, only the low-power receiver front-end is enabled for detecting the bus wake-up pattern as defined in ISO 11898-2:2016 Figure 11 state diagram. The bus signal needs to have two consecutive dominant states with a recessive state in between as shown in the following wakeup pattern timing diagram. The duration of these dominant and recessive states must be longer than T_{WU}. This pattern must be met within T_{WUTO}, otherwise, the pattern detection is nullified and restarts detection.



When the wake-up pattern is detected, RXD output is pulled low to inform the host. RXD remains low until IS32IO1163 enters CAN active state.

1.4 TXD Normal Mode Entry and Dominant Timeout

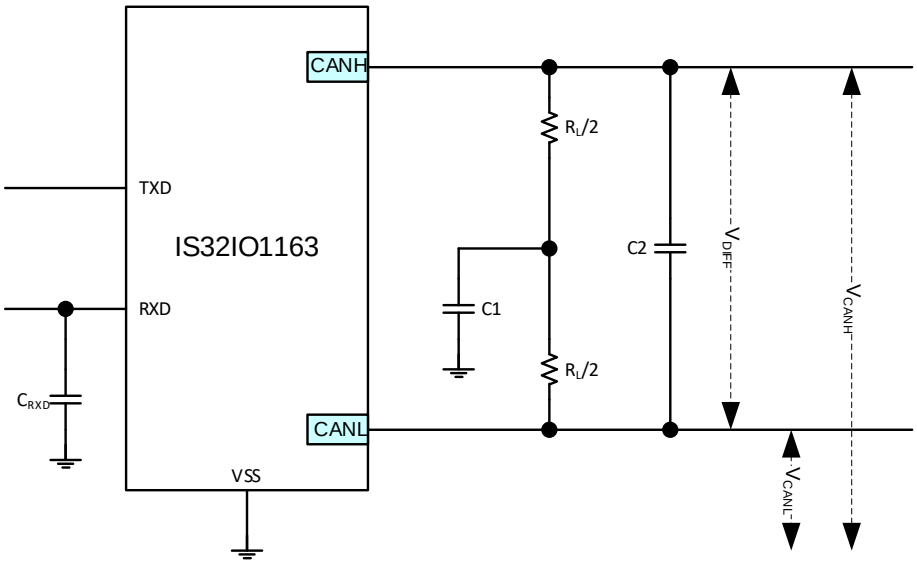
To prevent accidentally transmitting dominant state onto the bus when entering CAN active state as the transmitter is turning on, TXD must be first 1 to enable the transmission. In other words, if TXD is 0 entering CAN active state, the corresponding dominant state is not entered. The driver is then enabled when a TXD=1 event is seen.

In CAN active state, if TXD is 0 continuously exceeding $T_{DOM,TO}$, the driver is also disabled while remaining in CAN active state. This is to prevent rogue behavior from interfering with normal bus operation. The timeout condition is cleared if TXD=1 is detected.

1.5 Loss of Supply and Ground

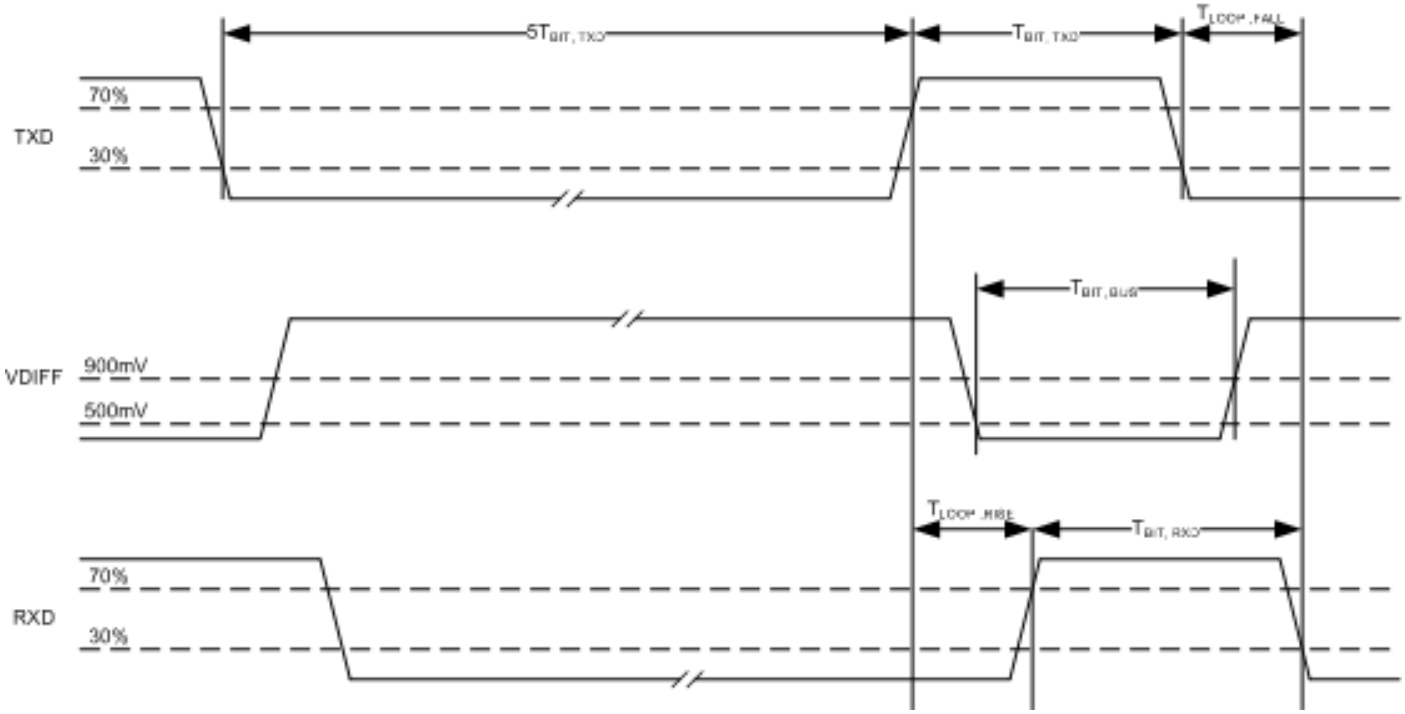
In the events of losing supply or ground, the transceiver presents no load to the bus. This is accomplished by the isolation diodes at the transmitter driver output. The bus still sees a differential resistance of around 40K Ohm due to the receiver biasing network, however, there is minimum DC leakage path to supply or ground.

1.6 Test Circuit



V_{DIFF} Differential voltage between CANH and CANL.
V_{CANH} Single-end voltage on CANH.
V_{CANL} Single-end voltage on CANL.
R_L Bus load resistance. 60 Ohm unless otherwise specified.
C1 4.7nF unless otherwise specified.
C2 100pF unless otherwise specified.
C_{RXD} 15pF unless otherwise specified.

1.7 HS-PMA Implementation Timing Diagram



$T_{BIT, TXD}$ = 1000ns for 1Mbit/s
$T_{BIT, TXD}$ = 500ns for 2Mbit/s
$T_{BIT, TXD}$ = 200ns for 5Mbit/s

2. Electrical Specifications

2.1 Maximum Limits

Parameter	Conditions	MIN	MAX	Unit
Voltage on Pin	Pin BAT	-0.3	40	V
	Pin V1	-0.3	6	V
	Pin VIO	-0.3	5.5	V
	PIN RXD, TXD, CTS, STBN, RSTN	-0.3	VIO	V
	Pin CANH, CANL	-27	40	V
	VDIFF = V(CANH) – V(CANL)	-5	10	V
ESD Rating	HBM			
	Pin CANH, CANL *1	-8	+8	kV
	Pin BAT	-4	+4	kV
	at any other pin	-2	+2	kV
	MM			
	Any Pin	-200	+200	V
	CDM			
	Corner Pins	-750	+750	V
	Any Pin	-500	+500	V
Junction Temperature		-40	+150	℃
Storage Temperature		-55	+150	℃

Note *1: BAT, V1/VIO, and GND are tied to the ground.

2.2 Thermal Characteristics

Symbol	Parameter	Conditions	TYP	Unit
R_{THJA}	Thermal resistance from junction to ambient	TSSOP-14 package free air	60	℃/W

2.3 DC Characteristics

V_{BAT} = 6.3V to 32V. T_J = -40℃ to +150℃. V(CANH) and V(CANL) within +/- 12V.

Typical values are given at V_{BAT} = 13V, V_{V1}=5V, and V_{VIO}=V_{V1} unless otherwise specified.

Refer to Section 2.6 for the test circuit with typical values of R_L=60Ω, C_1=4.7nF, C_{RXD}=15pF used.

All voltages are defined with respect to VSS or ground.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Pin BAT, V1 and VIO						
V_{BAT}	Supply voltage		6.3	13	32	V
$V_{BAT, PON}$	Supply voltage, power on	100msec ramp up/down time	4.8	5.3	5.8	V
$I_{BAT, ACT, REC}$	Supply current, normal mode	Recessive output, V1 no load.	3.0	4.5	6.0	mA
$I_{BAT, ACT, DOM}$	Supply current, normal mode	Dominant output, V1 no load, R_L=60Ω	30	42	55	mA
$I_{BAT, STB,32V}$	Supply current, standby mode	I_{V1} = 0, input at default states	60	82	170	μA

$I_{BAT, STB,13V}$	Supply current, standby mode	I_{V1} = 0, input at default states	50	72	140	μA
$V_{V1, No load}$	V1 output voltage	V_{BAT} = 13V, I_{V1} = 0.	4.75	5.0	5.25	V
$V_{V1, 100mA}$	V1 output voltage	V_{BAT} = 13V, I_{V1} = 100mA.	4.60	4.9	5.10	V
$V_{V1, UVD}$	V1 under voltage detect		3.7	4.2	4.5	V
$V_{V1, UVH}$	V1 under voltage release hysteresis		-	0.2	-	V
$I_{V1, OUTPUT}$	V1 output current	V_{BAT} = 13V, without UVD	-	150	-	mA
$I_{V1, SC}$	V1 short-circuit current	V1 short to 0V, V_{BAT} = 6.3V	160	230	300	mA
V_{IO}	IO supply voltage	For IS32IO1163B only	2.9	-	5.25	V
I_{VIO}	VIO Supply current	V_{V1} = 5.0V, input default states	-	20	40	μA
Pin STB, TXD, RXD, CTS, RSTN						
V_{IH}	Logic input high voltage	STBN, TXD, RSTN pins	0.7V_{IO}	-	-	V
V_{IL}	Logic input low voltage	STBN, TXD, RSTN pins	-	-	0.3VIO	V
$V_{OH, RXD, CTS}$	Logic output high voltage	RXD, CTS pin, I_{OH} = -2mA	V_{IO} – 0.5	-	-	V
$V_{OL, RXD,}$	Logic output low voltage	RXD, CTS pin, I_{OL} = 4mA	-	-	0.5	V
$V_{OL, RSTN}$	Logic output low voltage RSTN	RSTN pin, I_{OL} = 2mA	-	-	0.8	V
$R_{PD, STBN}$	Pull down resistor STBN		35	65	85	KΩ
$R_{PU, TXD}$	Pull up resistor TXD		35	65	85	KΩ
$R_{PU, RXD}$	Pull up resistor RXD		60	80	110	KΩ
$R_{PU, RSTN}$	Pull up resistor RSTN		35	65	85	KΩ
Bus CANH/CANL						
R_{DIFF}	Differential Input Resistance		20	30	40	KΩ
R_{CAN}	Single-end Resistance		10	15	20	KΩ
M_{CANR}	Matching of Resistance		-2	0	+2	%
C_{CAND}	Differential Capacitance	*1	-	10	-	pF
C_{CANS}	Single-End Capacitance	*1	-	8	-	pF
$I_{CANLK, LP}$	Bus Leakage Current, loss of power	V(CANH)=V(CANL)=5V, BAT=V1=VIO=GND=0V or short to 0V through 47KΩ	-10	-	+10	μA
Bus Receive						
V_{THNRM}	Normal mode threshold	-12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	0.5	-	0.9	V
V_{HYSNRM}	Normal mode hysteresis	-12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	50	85	125	mV
$V_{REC,NRM}$	Normal mode recessive differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	-3.0	-	0.5	V
$V_{DOM,NRM}$	Normal mode dominant differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	0.9	-	8.0	V

V_{THSTB}	Standby mode threshold	V(CANH), V(CANL) within +/-12V	0.4	-	1.15	V
$V_{REC,STB}$	Standby mode recessive differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	-3.0	-	0.4	V
$V_{DOM,STB}$	Standby mode dominant differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	1.15	-	8.0	V
V_{CANCM}	Common mode voltage range		-12	2.5	12	V
Bus Transmit						
$V_{OUT, RECN}$	NRM mode Recessive CANH/CANL output voltage	R_L not present	0.45	0.5	0.55	V1
$V_{OUTD, RECN}$	NRM mode Recessive Differential Output Voltage	R_L not present	-50	0	50	mV
$I_{OUT, RECN}$	NRM Recessive Current	CANH=CANL= +32V to -15V, R_L = 50Ω - 65Ω	-5	0	5	mA
$V_{OUTH, DOM}$	CANH dominant single-end output	R_L = 50Ω - 65Ω	2.75	3.6	4.50	V
$V_{OUTL, DOM}$	CANL dominant single-end output	R_L = 50Ω - 65Ω	0.50	1.4	2.25	V
$V_{OUTD, DOM}$	Dominant output differential swing	$V_{OUTH,DOM}$ - $V_{OUTL,DOM}$ R_L = 50Ω - 65Ω	1.50	2.2	3.00	V
$V_{OUTD, DOM, ARB}$	Dominant output differential swing, arbitration	$V_{OUTH,DOM}$ - $V_{OUTL,DOM}$ R_L = 2240Ω	1.50	3.8	5.00	V
$S_{OUT, DOM}$	Dominant output symmetry	V1 - ($V_{OUT,CANH}$ + $V_{OUT,CANL}$) R_L = 50Ω - 65Ω	-0.50	0	0.50	V
V_{SYM}	Driver symmetry	R_L = 60Ω, C_1=4.7nF 1MHz square wave	0.9	1	1.1	-
$I_{OSCH, DOM}$	CANH dominant output short-circuit current	V(CANH) = 0V	-	50	80	mA
$I_{CANH, MAX}$	CANH output maximum current	V(CANH) = -3V to 18V	-	-	115	mA
$I_{OSCL, DOM}$	CANL dominant output short-circuit current	V(CANL) = 5V	-	50	80	mA
$I_{CANL, MAX}$	CANL output maximum current	V(CANL) = -3V to 18V	-	-	115	mA
$V_{OUT, RECS}$	STB mode Recessive CANH/CANL output voltage	R_L not present	-0.1	0	0.1	V
$V_{OUTD, RECS}$	STB mode Recessive Differential output Voltage	R_L not present	-100	0	100	mV
Thermal Protection						
T_{JOTS}	Shutdown temperature	*1	-	175	-	℃
T_{JOTR}	Recovery temperature	*1	-	145	-	℃

Note 1: Not tested. Guaranteed by design and characterization.

2.4 AC Characteristics

VBAT = 6.3V – 32V, TJ = -40℃ to +150℃. V(CANH) and V(CANL) within +/- 12V.

Refer to Sections 2.6/2.7 for the test circuit with typical values of RL=60Ω, C1=4.7nF, CRXD=15pF used and timing waveform.

Typical values are given at VBAT = 13V unless otherwise specified.

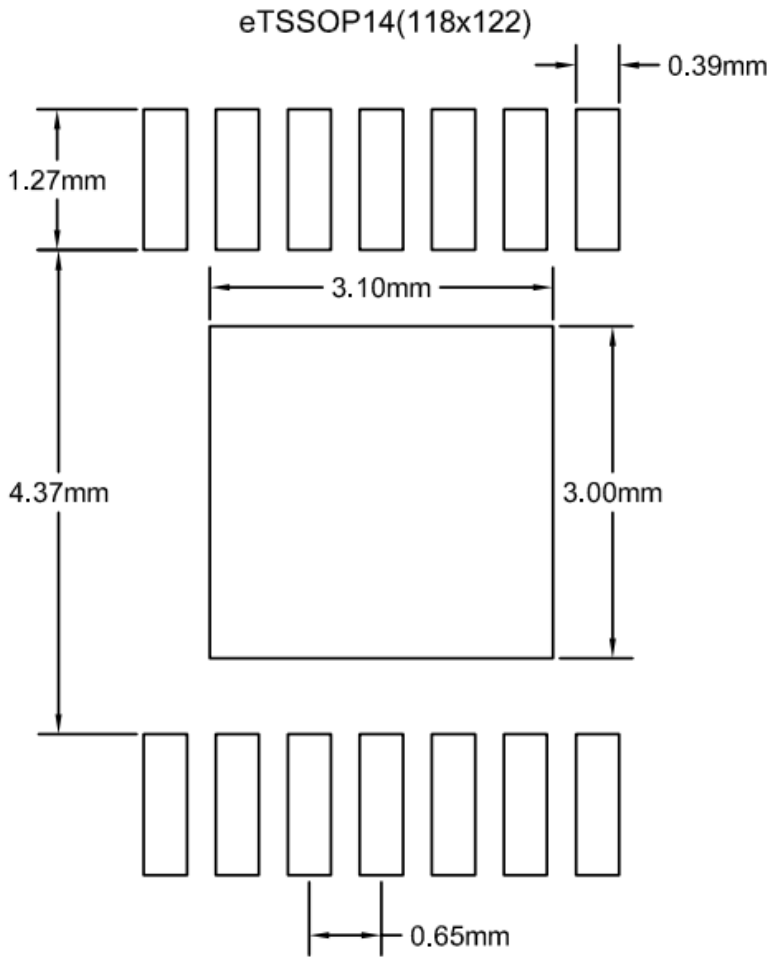
Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Timing Characteristics						
$T_{BAT, RAMP}$	Battery ramp up/down time	*1	-	-	50	ms
$T_{COLD START}$	Cold startup Delay	VBAT >= 6.3V startup	-	25	35	ms
$T_{WARM START}$	Warm startup Delay	RSTN startup	1.0	1.3	1.6	ms
T_{RSTN}	Reset extension time	RSTN applied externally	15	20	25	ms
$T_{PD,RX}$	Receive Propagation Delay	V_{CANCM}=2.5V, V_{CANDF}=1.5V C_{RXD} = 15 pF	-	90	-	ns
$T_{SYM, RX}$	Receive propagation delay mismatch	Recessive bit time distortion. *1	-20	-	+5	ns
$T_{PD,TX}$	Transmit Propagation Delay		-	60	-	ns
$T_{PDMS, TX}$	Transmit propagation delay mismatch	Recessive bit time distortion. *1	-25	-	+5	ns
T_{LOOP}	Loop delay	R_L = 60 Ω, C_1=4.7nF, C_2 = 100 pF, C_{RXD} = 15 pF	80	130	180	ns
$T_{BIT BUS, 2M}$	Transmitted recessive bit width 2Mbps	R_L = 60 Ω, C_2 = 100 pF. *1	435	-	530	ns
$T_{BIT RXD, 2M}$	Received recessive bit width 2Mbps	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF. *1	400	-	550	ns
$\Delta T_{BIT RXD, 2M}$	Received timing symmetry 2Mbps $T_{RXD,DOM} - T_{RXD,REC}$	R_L = 60 Ω, C_2 = 100 pF C_{RXD} = 15 pF. *1	-65	-	40	ns
$T_{BIT BUS, 5M}$	Transmitted recessive bit width 5Mbps	R_L = 60 Ω, C_2 = 100 pF. *1	155	-	210	ns
$T_{BIT RXD, 5M}$	Received recessive bit width 5Mbps	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF. *1	120	-	220	ns
$\Delta T_{BIT RXD, 5M}$	Received timing symmetry 5Mbps $T_{RXD,DOM} - T_{RXD,REC}$	R_L = 60 Ω, C_2 = 100 pF C_{RXD} = 15 pF. *1	-45	-	15	ns
$T_{DOM, TO}$	TXD dominant time-out time		1.8	2.7	4.0	ms
T_{WU}	Wakeup Filter Time	$V_{CAN,CM}$=0V, $V_{CAN,DIFF}$=1.2V	0.5	1.5	3.0	µs
T_{WUTO}	Wakeup detection timeout		500	700	1000	µs
$T_{SILENCE}$	Bus silence time		0.65	0.95	1.2	s
T_{TRANS}	State detection and transition, bias-on times	EN to CTS delay	-	180	220	µs

Note *1: Not tested. Guaranteed by design and characterization.

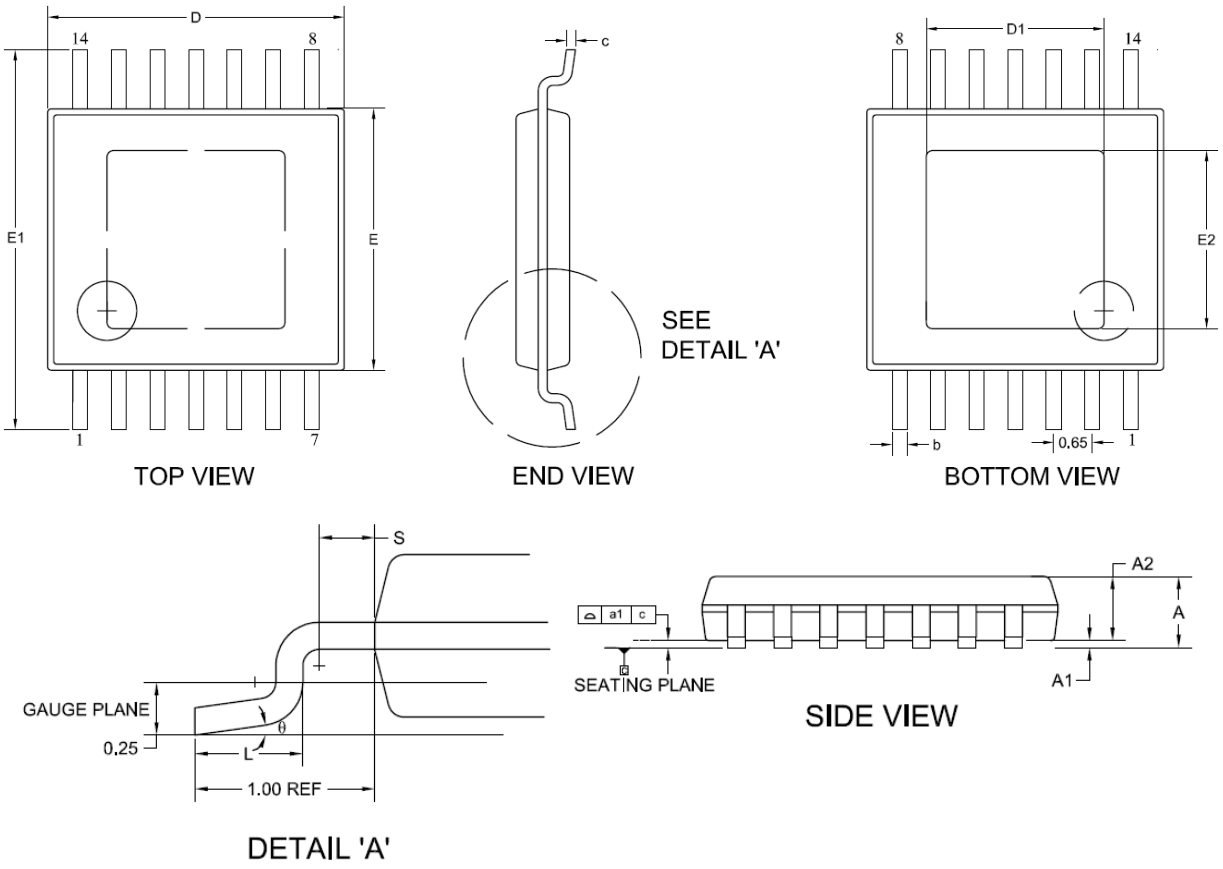
3. Packaging Outline

3.1 eTSSOP-14

RECOMMENDED LAND PATTERN



POD



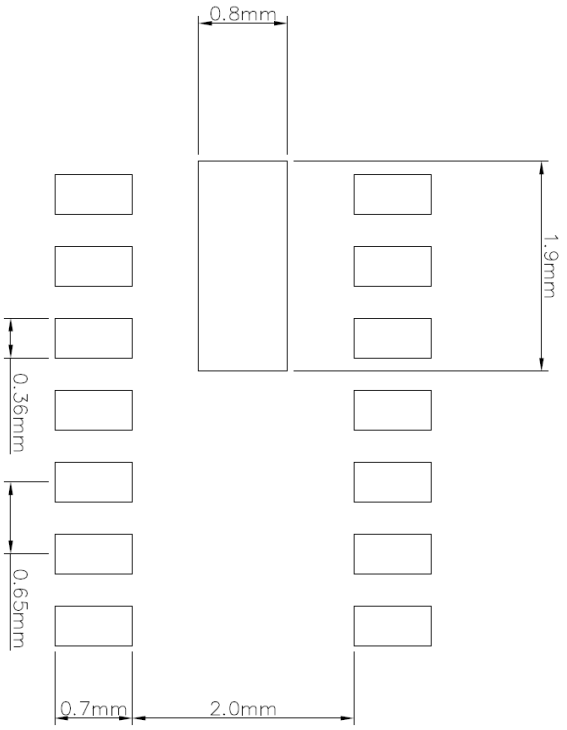
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

NOTE:

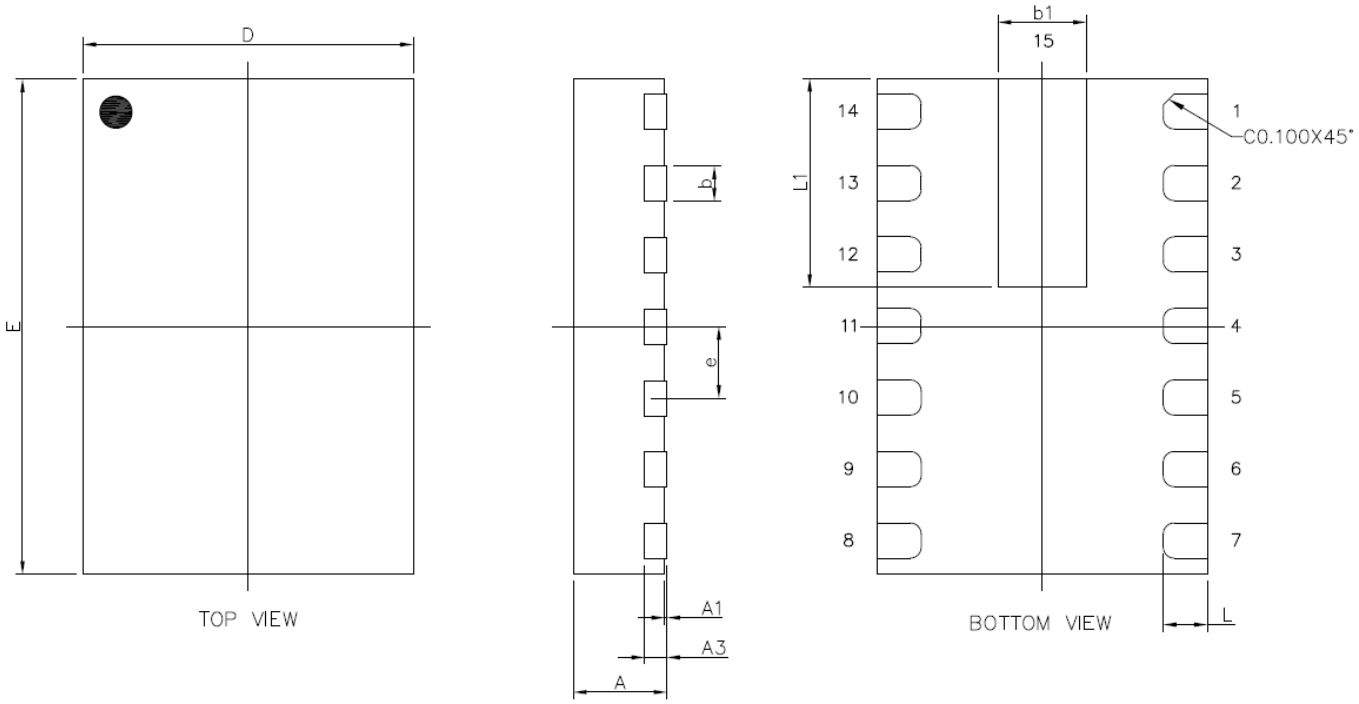
1. The thermal pad shows different shape among different factories.
2. Controlling dimension: mm
3. Reference document: JEDEC MO-153

3.2 FCDFN-14

RECOMMENDED LAND PATTERN



POD



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.27	0.32	0.37
b1	0.70	0.80	0.85
D	2.90	3.00	3.10
E	4.40	4.50	4.60
e	0.65 BSC		
L	0.35	0.40	0.45
L1	1.85	1.90	1.95

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-229F

4. Ordering Information

Temperature Range: -40℃ to 125℃

Order Part No.	Package	QTY/Reel	Remark
IS32IO1163A-ZLA3-TR	TSSOP-14 with exposed pad, Lead-free	2500	VIO internal connects to V1
IS32IO1163B-ZLA3-TR	TSSOP-14 with exposed pad, Lead-free	2500	Independent VIO pin
IS32IO1163A-DCLA3-TR	Flip chip DFN-14, Lead-free	2500	VIO internal connects to V1
IS32IO1163B-DCLA3-TR	Flip chip DFN-14, Lead-free	2500	Independent VIO pin

5. Revisions

Revision	Detailed Information	Date
A	Production Release	2023.06.13