IS1678

Bluetooth® 4.2 Dual-Mode Module

Features

- Bluetooth Classic (BR/EDR) and Low Energy (LE)
- Fully-certified, embedded 2.4 GHz Bluetooth 4.2 SoC, available in ROM-based (IS1678S) and Flash-based (IS1678SM) versions
- Transparent UART mode for seamless serial data over UART interface
- Configurable I/O pins for control and status
- Integrated crystal oscillator operates with 16 MHz external crystal
- Internal voltage regulator and matching circuitry
- Easy to configure with User Interface (UI) tool, a Windows®-based utility or directly by MCUs
- Firmware can be upgraded in the field over UART
- 4 Mbit Flash (only IS1678SM)
- Supports Apple® iPod Accessory Protocol (iAP2), (only IS1678SM)
- Supports Bluetooth 4.2 LE secure connections
- Supports Bluetooth 4.2 LE data packet length extension
- Ideal for portable battery operated devices
- Internal battery regulator circuitry
- One LED driver with 16 steps brightness control
- IC Size: 6 mm x 6 mm

RF/Analog

- Frequency: 2.402 GHz to 2.480 GHz
- Receive sensitivity: -90 dBm (BR/EDR), -92 dBm (LE)
- Class 2 output power (+2 dBm typical)

Data Throughput

Data throughput at 1 Mbps UART baud rate:

- BR/EDR: up to 32 Kbytes/s
- LE: up to 7 Kbytes/s

Data throughput at 115200 bps UART baud rate:

- BR/EDR: up to 10 Kbytes/s
- LE: up to 6 Kbytes/s

MAC/Baseband/Higher Layer

- Secure AES128 encryption
- Bluetooth 3.0: GAP, SPP, SDP, RFCOMM and L2CAP
- Bluetooth 4.2: GAP, GATT, ATT, SMP and L2CAP

Operating Conditions

- Operating voltage range: 3.3V to 4.2V
- Operating temperature: -20ºC to +70ºC

Applications

- Internet of Things (IoT)
- Secure Payment
- Home and Security
- Health and Fitness
- Industrial and Data Logger
- LED Lighting (16 configurations)

Packages

Type	QFN
Pin Count	40
Contact/Lead Pitch	0.5
Dimensions	6 x 6 x 0.9

Note: All dimensions are in millimeters (mm) unless specified.

IS1678

General Description

The IS1678S/SM is a fully-certified Bluetooth v4.2 (BR/EDR/LE) SoC that enables the user to easily add dual-mode Bluetooth wireless capability to their products. The IS1678 SoC is available in ROM-based (IS1678S) and Flash-based (IS1678SM) versions. Refer to
 9.0 "Ordering information" for additional information on the IS1678 SoC versions.

The IS1678 SoC bridges the customer products to smart phones or tablets for convenient data transfer, control, access to cloud applications, and delivering the local connectivity for IoT. The IS1678 SoC also supports GAP, SDP, SPP and GATT profiles. Data transfer is achieved over the Bluetooth link by sending or receiving data through Transparent UART mode, making it easy to integrate any microprocessor or microcontroller with the UART interface. It also enables an easy configuration by using a UI tool, a Windows-based utility or directly by MCU through UART.

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NOTES:

1.0   SYSTEM OVERVIEW

The IS1678S/SM is a fully-certified, embedded
2.4 GHz Bluetooth 4.2 (BR/EDR/LE) wireless SoC. It
includes an on-board Bluetooth stack, a power man-
agement subsystem, a 2.4 GHz transceiver, and a RF
power amplifier. Customers can embed Bluetooth func-
tionality to any applications using the IS1678S/SM
SoC.

The IS1678S/SM SoC enables rapid product develop-
ment and faster time to market, and it is designed to
provide integrators with the following features:

• Ease of integration and programming
• Reduced development time
• Low system cost
• Interoperability with Bluetooth hosts
• Wide range of applications

The IS1678S/SM SoC can independently maintain a
low-power wireless connection. The low power usage
and flexible power management maximize the lifetime
of the end-product in battery operated applications. A
wide operating temperature range enables its applica-
tions in indoor and outdoor environments.

Figure 1-1 illustrates a typical block diagram of the
IS1678S/SM SoC.

FIGURE 1-1:   IS1678S/SM SOC BLOCK DIAGRAM
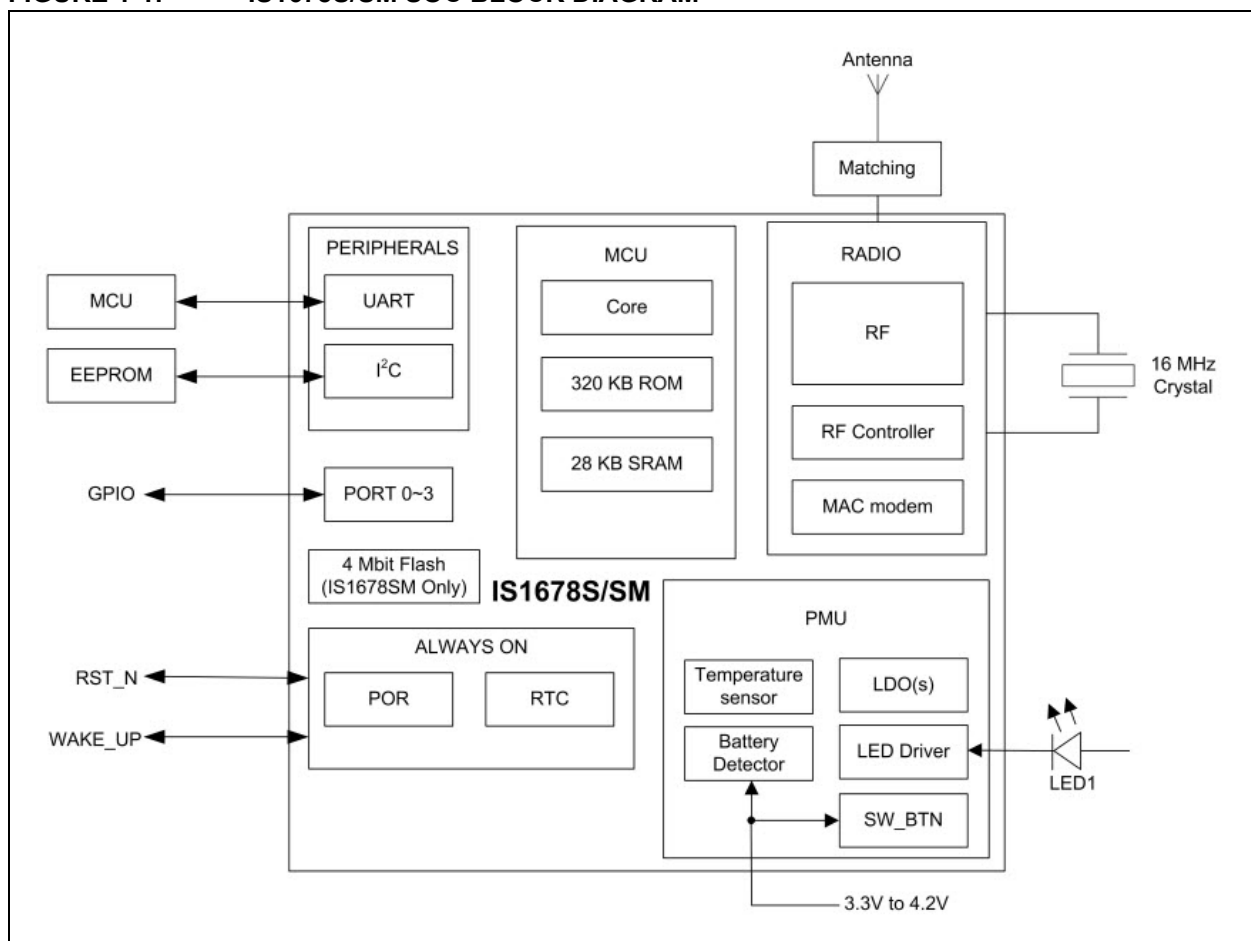
IS1678

1.1 Pin Assignment

Figure 1-2 illustrates the pin diagram of the IS1678S/SM SoC.
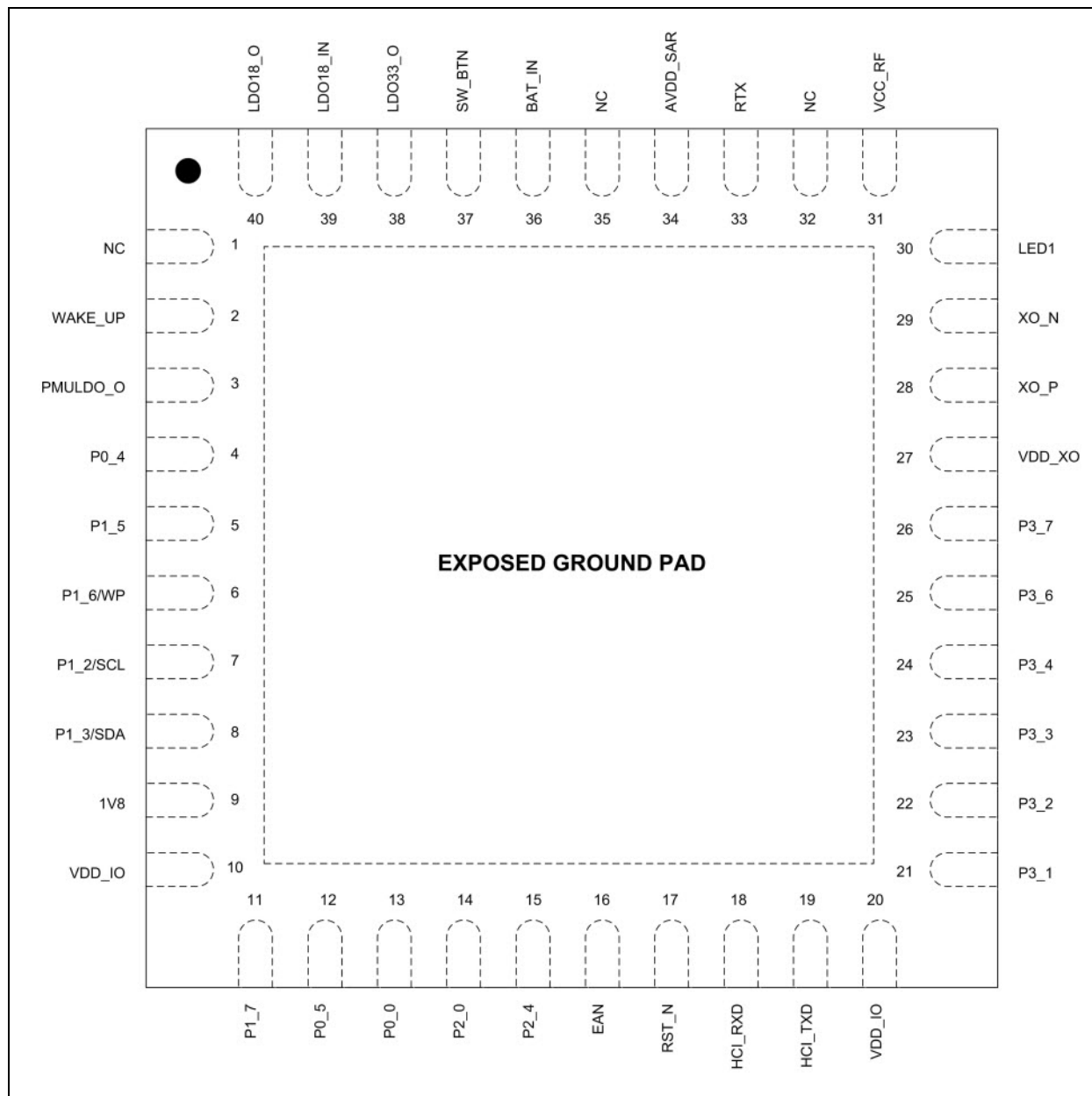
FIGURE 1-2: IS1678S/SM SOC PIN DIAGRAM

Table 1-1 provides various pins of the IS1678S/SM SoC.

TABLE 1-1:   PIN DESCRIPTION

Pin Number	Pin Name	Pin Type	Pin Description
1	NC	NC	No connection
2	WAKE_UP	DI	Wake-up from Sleep mode (active-low) (internal pull up)
3	PMULDO_O	Power	Power Management Unit (PMU) output (1.8V), for measurement purpose only. Do not connect to external devices Connect to GND through a 1 µF (X5R/X7R) capacitor
4	P0_4	DO	IS1678S/SM Status Indication pin, refer to Table 2-4
5	P1_5	DO	IS1678S/SM Status Indication pin, refer to Table 2-4
6	P1_6/WP	DO	EEPROM Write Protect (Connected to external EEPROM)
7	P1_2/SCL	DO	I^{2}C SCL to EEPROM or GPIO
8	P1_3/SDA	DIO	I^{2}C SDA to EEPROM or GPIO
9	1V8	Power	1.8V input for digital core power Connect to Ground through a 1 µF (X5R/X7R) capacitor
10	VDD_IO	Power	I/O positive supply input (3.3V) Connect to Ground through a 1 µF (X5R/X7R) capacitor
11	P1_7	DIO	Configurable control or Indication pin assigned to UART CTS (input)
12	P0_5	DIO	Configurable control or Indication pin
13	P0_0	DIO	Configurable control or Indication pin assigned to UART RTS (output)
14	P2_0	DI	System configuration pin along with P2_4 and EAN pins. It is used to set the IS1678S/SM SoC in one of the following three modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to download new firmware to the flash of IS1678SM SoC), refer to Table 2-1
15	P2_4	DI	System configuration pin along with P2_0 and EAN pins. It is used to set the IS1678S/SM SoC in any one of the following three modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to download new firmware to the flash of IS1678SM SoC), refer to Table 2-1
16	EAN	DI	External address-bus negative System configuration pin along with P2_0 and P2_4 pins. It is used to set the system in one of the following three modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to download new firmware to the flash of IS1678SM SoC), refer to Table 2-1 ROM: Must be pulled-high to VDD_IO FLASH: Must be pulled-down with 4.7 kOhm to GND
17	RST_N	DI	SoC reset (active-low) (internal pull up) Apply a pulse of at least 63 ns Connect to Ground through a 1 µF (X5R/X7R) capacitor
18	HCI_RXD	DI	UART data input
19	HCI_TXD	DO	UART data output
20	VDD_IO	Power	I/O positive supply input (3.3V) Connect to Ground through a 1 µF (X5R/X7R) capacitor

Legend: A = Analog   D = Digital   I = Input   O = Output

TABLE 1-1:   PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Pin Type	Pin Description
21	P3_1	DIO	Configurable control or Indication pin (Internally pulled-up, if configured as an input)
22	P3_2	DIO	Configurable control or Indication pin (Internally pulled-up, if configured as an input)
23	P3_3	DIO	Configurable control or Indication pin (Internally pulled-up, if configured as an input)
24	P3_4	DIO	Configurable control or Indication pin (Internally pulled-up, if configured as an input)
25	P3_6	DIO	Configurable control or Indication pin (Internally pulled-up, if configured as an input)
26	P3_7	DIO	Configurable control or Indication pin (Internally pulled-up, if configured as an input)
27	VDD_XO	Power	1.8V input for the external 16 MHz crystal Connect to Ground through a 1 µF (X5R/X7R) capacitor
28	XO_P	AI	Positive node for RF 16 MHz crystal input
29	XO_N	AI	Negative node for RF 16 MHz crystal input
30	LED1	DO	LED driver
31	VCC_RF	Power	Power input for VCO and RF (1.8V) Connect to Ground through a 1 µF (X5R/X7R) capacitor
32	NC	NC	No connection
33	RTX	AIO	External antenna connection (50 Ohm)
34	AVDD_SAR	Power	1.8V input for AVDD_SAR power Connect to Ground through a 1 µF (X5R/X7R) capacitor
35	NC	NC	No connection
36	BAT_IN	Power	Battery input. Main positive supply input Connect to Ground through a 10 µF (X5R/X7R) capacitor
37	SW_BTN	DI	Software Power Buttons: H: power on, L: power off
38	LDO33_O	Power	Internal 3.3V LDO regulator output Connect to Ground through a 10 µF (X5R/X7R) capacitor
39	LDO18_IN	Power	Internal 1.8V LDO regulator input Connect with LDO33_O
40	LDO18_O	Power	Internal 1.8V LDO regulator output Connect to Ground through a 1 µF (X5R/X7R) capacitor
41	EP	Power	Exposed Ground pad

Legend: A = Analog   D = Digital   I = Input   O = Output

2.0 APPLICATION INFORMATION

2.1 System Configuration Pins

The system configuration I/O pins P2_0, P2_4 and EAN are used to set the configuration and firmware programming modes. Each of these pins have internal pull up and allow configuration settings and firmware update from the UART. Table 2-1 provides the system configuration settings.

TABLE 2-1: SYSTEM CONFIGURATION SETTINGS

IC	P2_0	P2_4	EAN	Operational Mode
IS1678S	Low	High	High	Test mode (Write EEPROM)
	High	High	High	Application mode (Normal operation)
IS1678SM	Low	Low	High	Write Flash
	Low	High	Low	Test mode (Write EEPROM)
	High	High	Low	Application mode (Normal operation)

2.2 Control and Indication I/O Pins

The I/O pins, P0_0, P0_5, P1_7, P3_1, P3_2, P3_3, P3_4, and P3_7, are configuration control and indication signal pins. The control signals are input to the IS1678S/SM SoC and the indication signals are output from the IS1678S/SM SoC. Table 2-2 provides the default I/O pin configuration details.

TABLE 2-2: CONTROL AND INDICATION I/O PIN ASSIGNMENTS

PIN Symbol	Default Configuration
P0_0	UART_RTS[1,2]
P0_5	N/C
P1_7	UART_CTS[1,2]
P3_1	INQUIRY CONTROL
P3_2	LINK_DROP_CONTROL (DISCONNECT)
P3_3	UART_RX_IND
P3_4	PAIRING_KEY
P3_7	LOW_BATTERY_IND

Note 1: The RTS and CTS pins are fixed and cannot be configured while using the flow control, or else these pins can be configured as GPIOs.

2: The RTS can only be assigned to the P0_0 pin and the CTS can only be assigned to the P1_7 pin.

Table 2-3 provides the configurable functions and descriptions of I/O pins.

TABLE 2-3: CONFIGURABLE FUNCTIONS AND DESCRIPTIONS

Function Name	Description
Low Battery indication	This function when assigned to a pin, the output goes low when the battery level is below a specified level. The UI tool can set the low battery level
RSSI indication	This function when assigned to a pin, can be used to indicate the quality of the link based on the Received Signal Strength Indicator (RSSI) level. If the RSSI level is lower than the specified values, then the RSSI indication pin goes low
Link Drop control	This function when assigned to a pin, can be used to force the SoC to drop the current Bluetooth Low Energy (BLE) link with a peer device. Pulling the Link Drop pin low will force the disconnect. The pin needs to be pulled-low for at least 10 ms

TABLE 2-3:   CONFIGURABLE FUNCTIONS AND DESCRIPTIONS

Function Name	Description
UART RX indication	This function when assigned to a pin, enables communication with the UART, when the SoC is in Low-Power mode. When not in Low-Power mode, the SoC runs on a 16 MHz clock. If the user intends to provide data or commands via UART in the Low-Power mode, then the UART_RX_IND pin needs to be pulled-low and the user has to wait at least 5 ms before sending the data. Pulling the UART_RX_IND pin low allows the SoC to operate the 16 MHz clock and to enable UART
Pairing Key	This function when assigned to a pin, can be used to force the SoC to enter Standby mode. The pin needs to be pulled-down for at least 160 ms
Inquiry Control	This function when assigned to a pin, forces the SoC to enter Inquiry mode (Bluetooth Classic). The pin must be pulled-low for at least 240 ms for the device to enter Inquiry mode
Profile_IND	This function when assigned to a pin, can be used to indicate whether current connection is in Basic Data Rate (BDR)/Enhanced Data Rate (EDR) (Bluetooth Classic), or in BLE. If the Profile_IND pin is high, then the current connection is BDR/EDR connection. If low, then the current connection is a BLE connection. This pin is valid only for Link State

2.3   Status Indication I/O Pins

The I/O pins, P1_5 and P0_4, are status indicator pins: STATUS_IND_1 and STATUS_IND_2. Both the pins provide status indication to the host MCUs. Table 2-4 provides status indication of the P1_5 and P0_4 pins.

TABLE 2-4:   STATUS INDICATION

P1_5 /STATUS_IND_1	P0_4/STATUS_IND_2	Indication
High	High	Power-on (default setting) and Deep-sleep state. HH status must be stable for at least 500 ms
High	Low	Access state
Low	High	Link state (UART data transmitting)
Low	Low	Link state (no UART data being transmitted)

2.4   Power Tree

Figure 2-1 illustrates the power tree diagram of the
IS1678S/SM SoC.

FIGURE 2-1:   IS1678S/SM SOC POWER TREE DIAGRAM
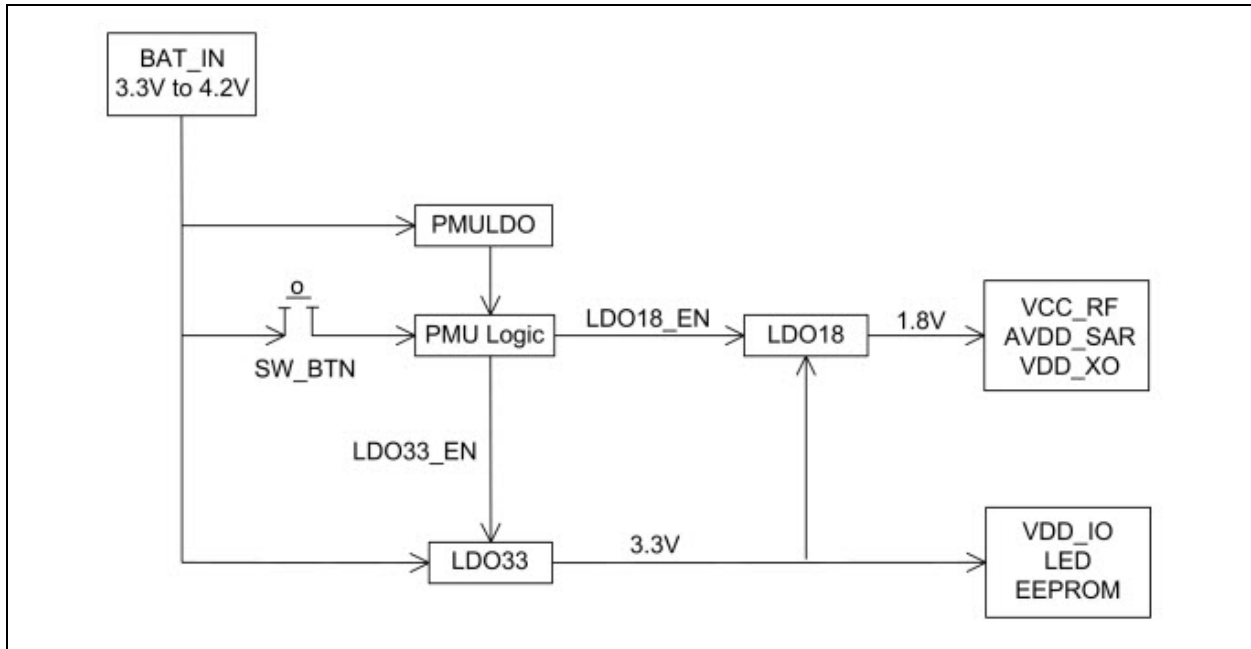
2.5 Software Power Button (SW_BTN)

The Software power button (SW_BTN) input pin powers the IS1678S/SM SoC ON (high) or OFF (low) into the S4 mode. The S4 mode is Deep-sleep mode and the S2 mode is Sleep mode. The S4 mode can only be triggered by the SW_BTN pin, and the power consumption is lower in the S4 mode.

Figure 2-2 through Figure 2-4 illustrate the waveforms of the IS1678S/SM SoC in the high and low status, that is access and link status.

FIGURE 2-2:   **SW_BTN TIMING (HIGH) AT APPLICATION MODE**

Note 1: MCU can send UART command, refer to P0_4/P1_5 status in Table 2-4.

    2: Reset pin is not connected.

    3: Time duration (475 ms) is for reference purpose only, the host MCU must check the status pin.
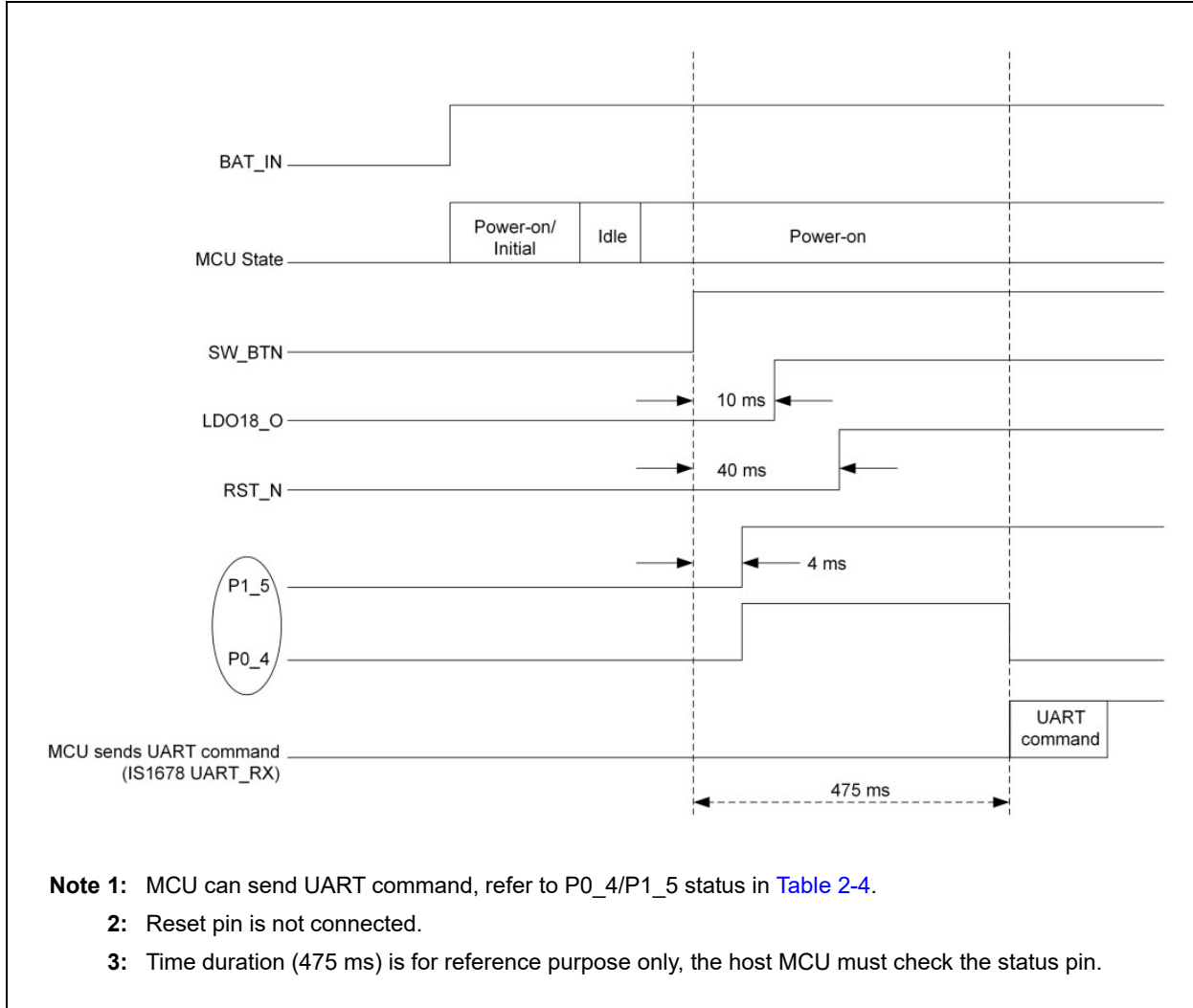
FIGURE 2-3: **SW_BTN TIMING (LOW) AT ACCESS STATES**

Note: Reset pin is not connected.
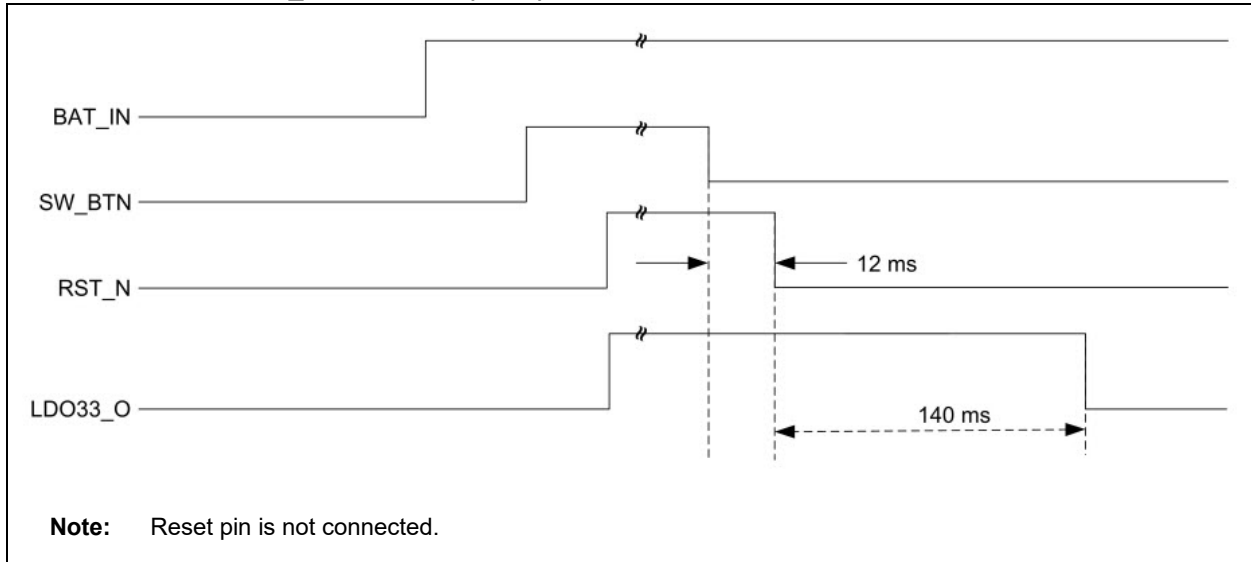
FIGURE 2-4: **SW_BTN TIMING (LOW) AT LINK STATES**

Note 1: Time duration (830 ms) is a typical value measured on iPhone® 6, which can vary from one smart phone to another.
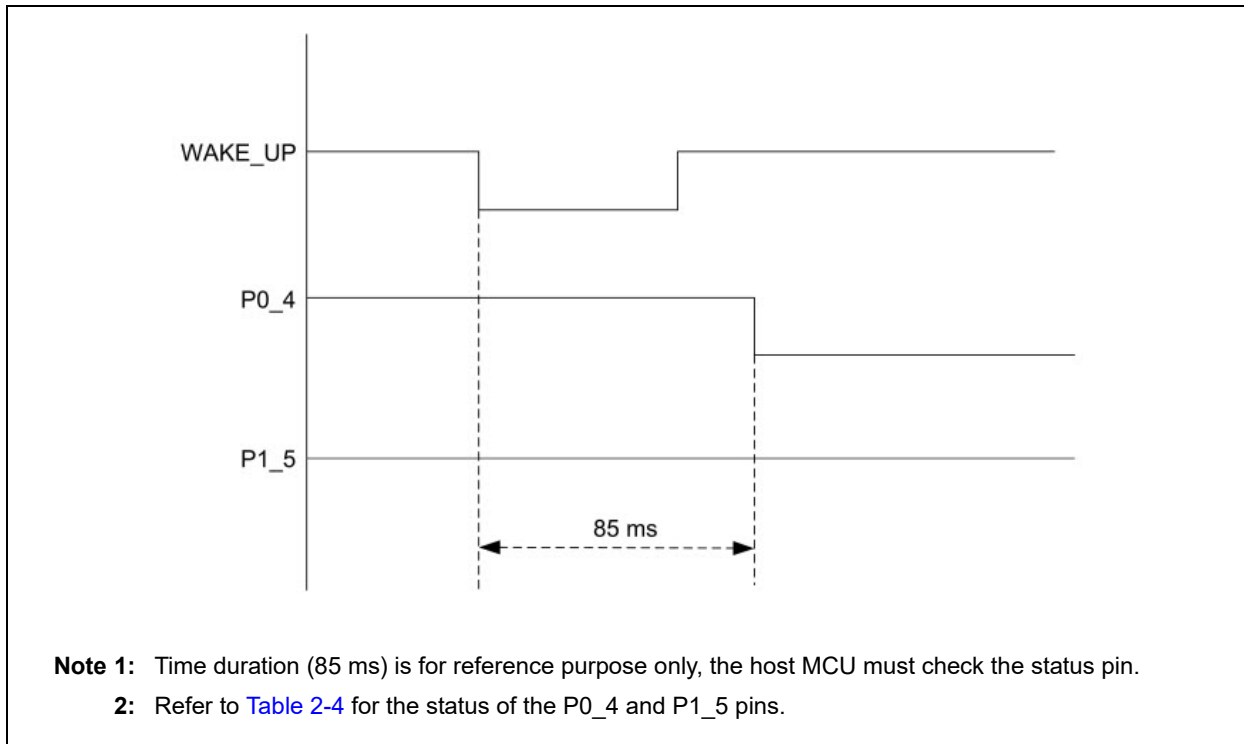
2: Reset pin is not connected.
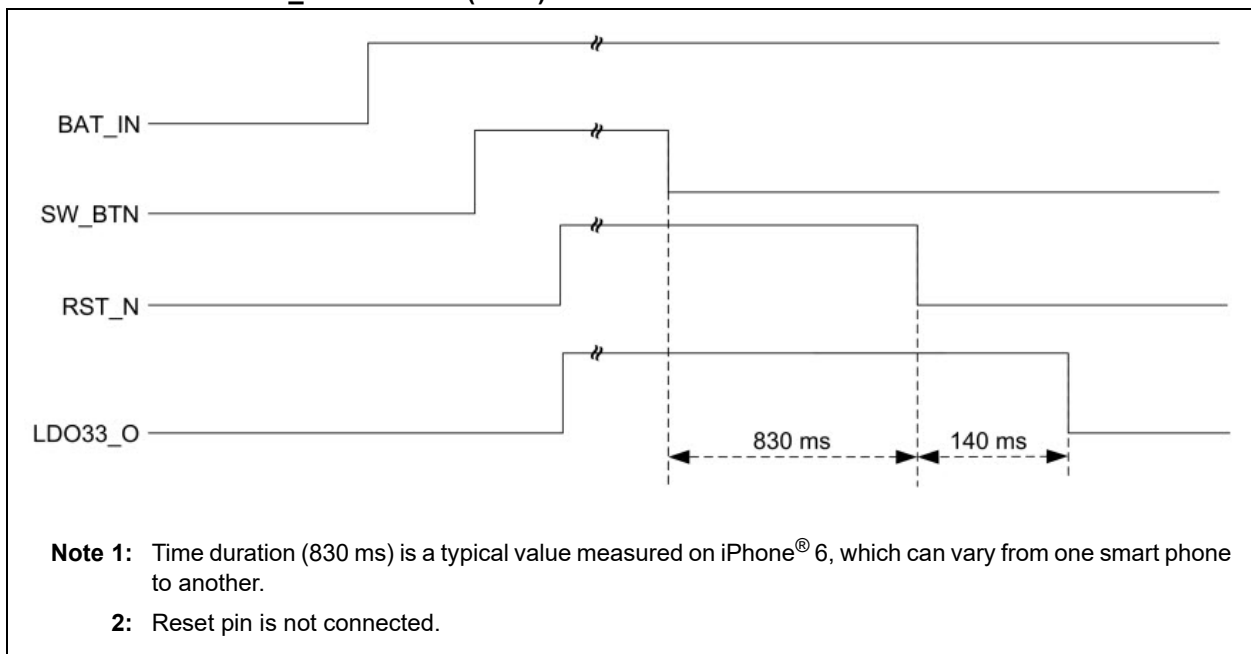
2.6 Wake-Up

The WAKE_UP input pin wakes up the IS1678S/SM SoC from the Sleep mode (S2) mode. The WAKE_UP pin is active-low and puts the SoC from Sleep mode (S2) to Standby mode. Figure 2-5 illustrates the timing diagram of the IS1678S/SM SoC in the wake-up mode.

FIGURE 2-5:   WAKE-UP TIME

Note 1: Time duration (85 ms) is for reference purpose only, the host MCU must check the status pin.

2: Refer to Table 2-4 for the status of the P0_4 and P1_5 pins.

2.7   External Reset

The watchdog timer (WDT) can reset the IS1678S/SM SoC. It has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power-on state. This action can also be driven by an external Reset signal which is used to externally control the device by forcing the device into a POR state. The RST_N signal input is active-low and connection is not required in most of the applications.

Figure 2-6 illustrates the timing diagram of the IS1678S/SM SoC when it is in the Reset (RST_N is set to active-low) state.

FIGURE 2-6:   RESET TIMING WAVEFORMS

Note 1:   Auto Pattern mode can use external Reset signal. For more details on the Auto Pattern mode, refer to **3.0 "Operating Modes"**.

2:   The RST_N state trigger must be greater than 63 ns.

3:   Manual pattern can use external Reset signal and Reset command. For more details on the Manual Pattern mode, refer to **3.0 "Operating Modes"** and "*IS1678 UART Command Set User Guide*".

4:   Time duration (350 ms) is for reference purpose only, the host MCU must check the status pins P0_4 and P1_5.

2.8   Reference Clock

The IS1678S/SM SoC is composed of an integrated crystal oscillation function. It requires a 16 MHz external crystal and two specified load capacitors to obtain a high quality system reference timer source. This function is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent load capacitance in mass production. The frequency trim is achieved by adjusting the crystal load capacitance through on-chip trim capacitors (C_{trim}) integrated in the chip.

The value of the trimming capacitance is around 200 fF (200×10^{-15} F) per LSb at 5-bit word. Therefore, the overall adjustable clock frequency is around ±40 kHz.

C_{trim} = 200fF*(1 to 31), capacitor on-chip and can be trimmed in the MP process.

C_{int} » 3pF, C_{int} is a sub-total capacitor value on the path, which is derived from the layout trace and chip pad.

$C_L = [(C_{L1}*C_{L2})/(C_{L1}+C_{L2})]+(C_{trim}/2)+C_{int}$

For example, if trim value is set as 16, then C_{trim} = 3.2 pF.

For a 16 MHz crystal, where C_L = 9 pF, then $C_{L1} = C_{L2}$ = 9.1 pF.

> **Note:**   For additional information on C_L selection, refer to the data sheet of the crystal.

Figure 2-7 illustrates the external crystal connection of the IS1678S/SM SoC with two load capacitors.

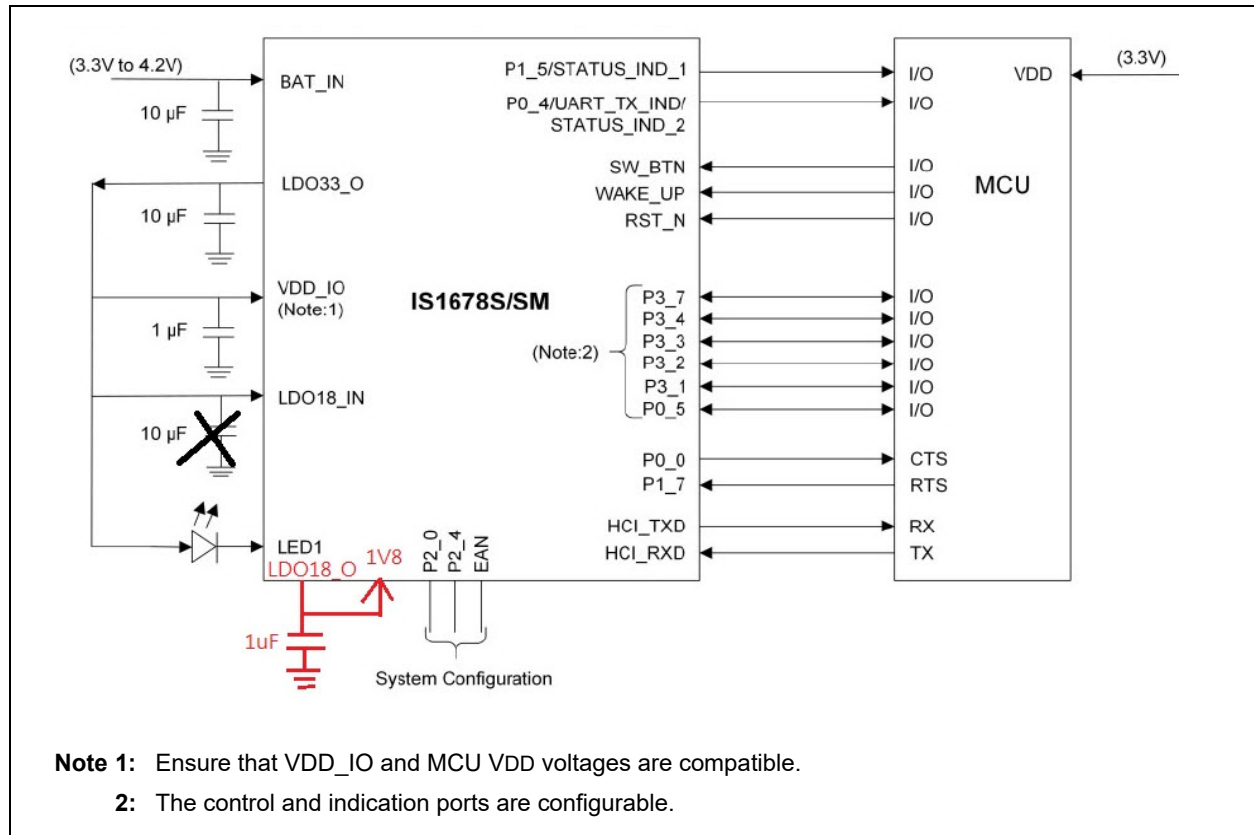**FIGURE 2-7:**   **EXTERNAL CRYSTAL WITH LOAD CAPACITORS**
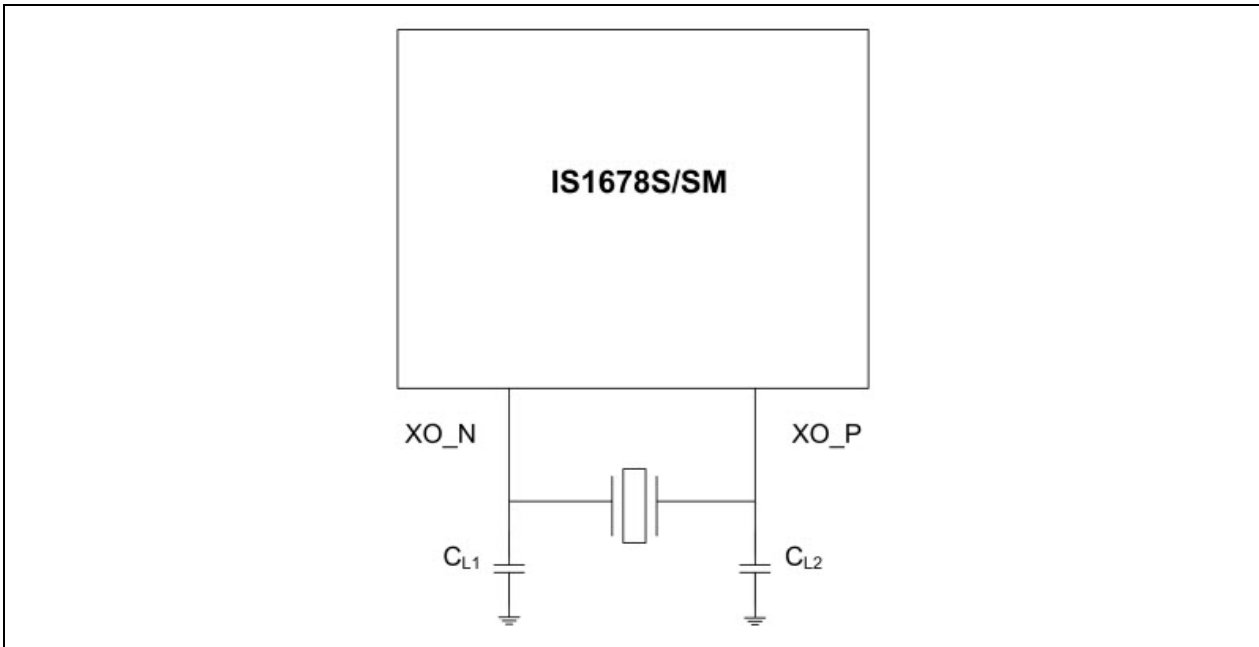
2.9 Host MCU Interface Over UART

Figure 2-8 illustrates a typical example of the UART interface with host MCU and power scheme using 3.3V to MCU VDD. Battery power is applied to the BAT_IN pin. The voltage can be routed from the LDO33_O pin to the VDD_IO pin and external circuitry including the MCU. This power scheme ensures that the IS1678S/SM and MCU I/O voltages are compatible.

> **Note:** The internal 3.3V LDO current source must not exceed a maximum value of 50 mA.

FIGURE 2-8: UART INTERFACE WITH HOST MCU

Note 1: Ensure that VDD_IO and MCU VDD voltages are compatible.

2: The control and indication ports are configurable.

2.10 LED Driver

The LED can be connected to the IS1678S/SM SoC and one dedicated LED driver controls the LED. The maximum sourcing current for the LED is 5 mA and it provides 16 options (configuration) to trim the brightness of the LED. The LED brightness can be configured using the UI tool, a Windows-based utility. Figure 2-9 illustrates the block diagram of the LED driver in the IS1678S/SM SoC.

The status indication of the LED (LED1) are as follows, and each status indication is a configurable flashing sequence:

• Standby
• Link Back
• Low Battery
• Inquiry
• Link
• Page

FIGURE 2-9: LED DRIVER
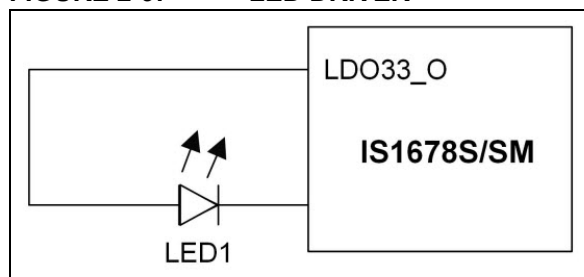
NOTES:

3.0   OPERATING MODES

The IS1678 SoC provides the option for the user to operate the SoC in two distinct modes:

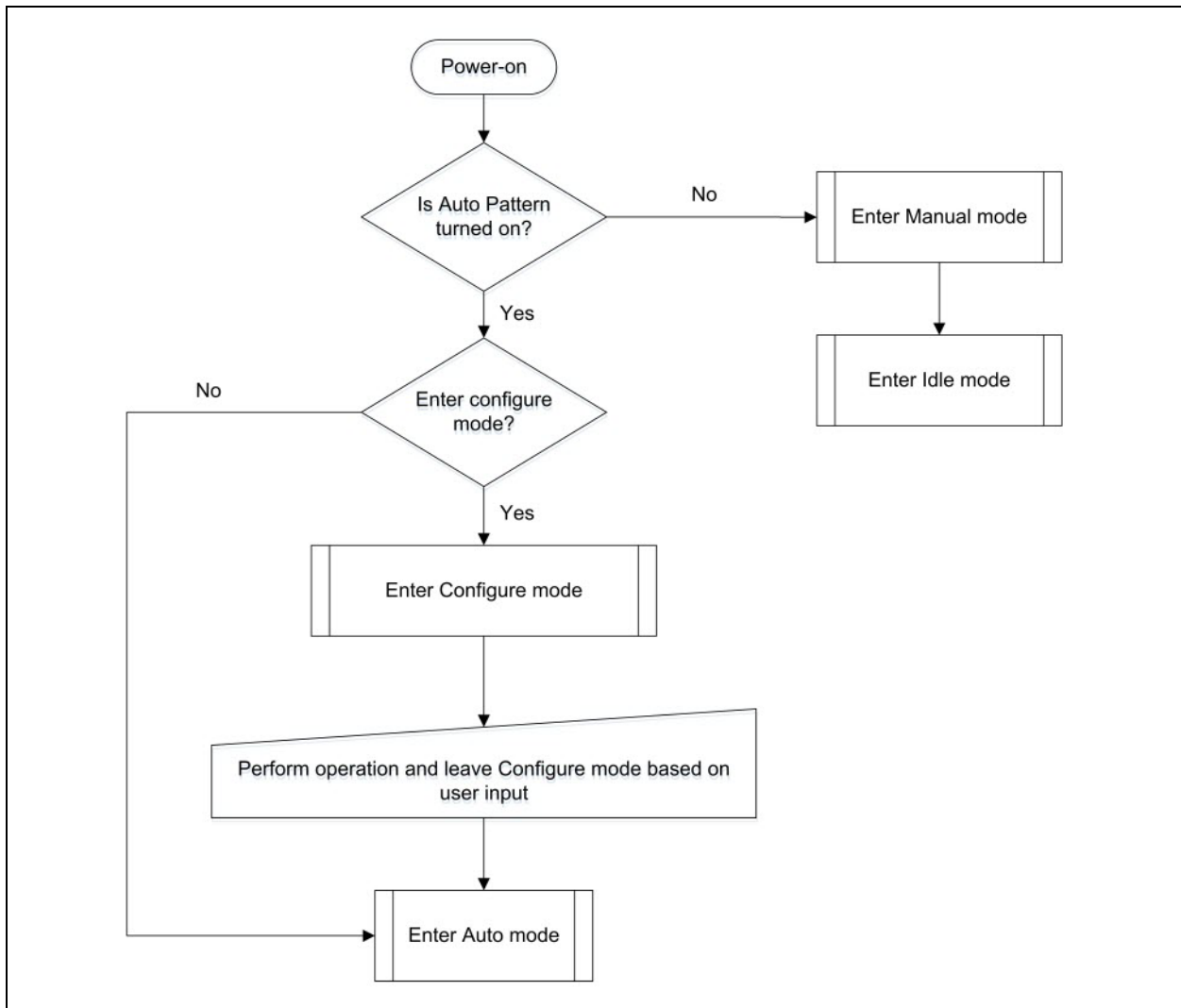• Auto Pattern mode
• Manual Pattern mode

The Auto Pattern mode and the Manual Pattern mode use different state machines. Users can operate the IS1678 SoC in either of these modes by setting the values in the EEPROM location. The IS1678 SoC is in Auto Pattern mode by default. To modify the EEPROM values, the SoC must be placed in the "Write EEPROM and Test mode" through the pins P2_0, P2_4 and EAN.

The UI tool provides an easy Windows Graphical User Interface (GUI) to set or modify the EEPROM settings on the IS1678 SoC.

Note: The UI tool is available for download from the Microchip web site at: www.microchip.com/IS1678.

Figure 3-1 illustrates the basic algorithm followed by the IS1678 SoC during startup, in deciding which state machine to be used for operation.

FIGURE 3-1:   OPERATING MODE CONFIGURATION
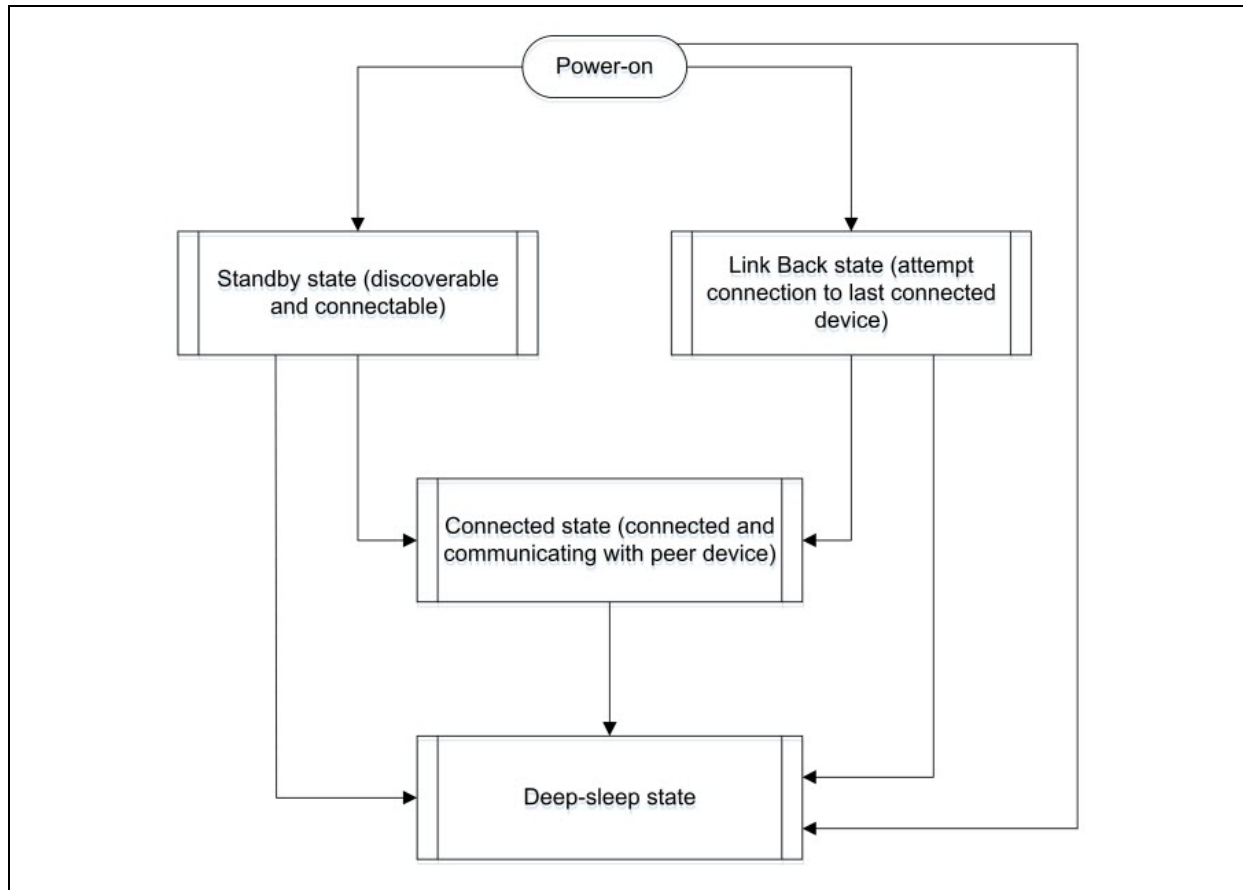
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3.1 Auto Pattern Mode

The Auto pattern mode is a state machine in which the Bluetooth related operations are automated. It is primarily used to connect the SoC to a peer device and create a data pipe with the peer device through the Transparent UART mode, thus providing a "cable replacement" solution. Also, the SoC provides the user to enter some configuration commands in the Auto Pattern mode. For more details on the list of configuration commands that can be used in Auto Pattern mode, refer to the "*IS1678 UART Command Set User Guide*".

Figure 3-2 illustrates the basic state machine in the Auto Pattern mode.

FIGURE 3-2: **AUTO PATTERN MODE**

To evaluate and test the IS1678 SoC in the Auto Pattern mode, download and install the Auto Pattern tool (Windows-based GUI emulation tool), which is available at Microchip web site. This tool implements the communication protocol for Auto Pattern mode. It also provides a fast and easy way to test the functions and options available in the Auto Pattern mode.

Note:	The Auto Pattern tool and "*IS1678 UART Command Set User Guide*" document, are available for download from the Microchip web site at: www.microchip.com/IS1678.

3.2 Manual Pattern

The Manual Pattern mode provides full control of the IS1678 SoC to the user, and the SoC operates only based on the commands from the user or host MCU. Figure 3-3 illustrates the state machine followed by the IS1678 SoC in the Manual Pattern mode.

FIGURE 3-3: **STATE CHANGES BY MCU IN MANUAL PATTERN**
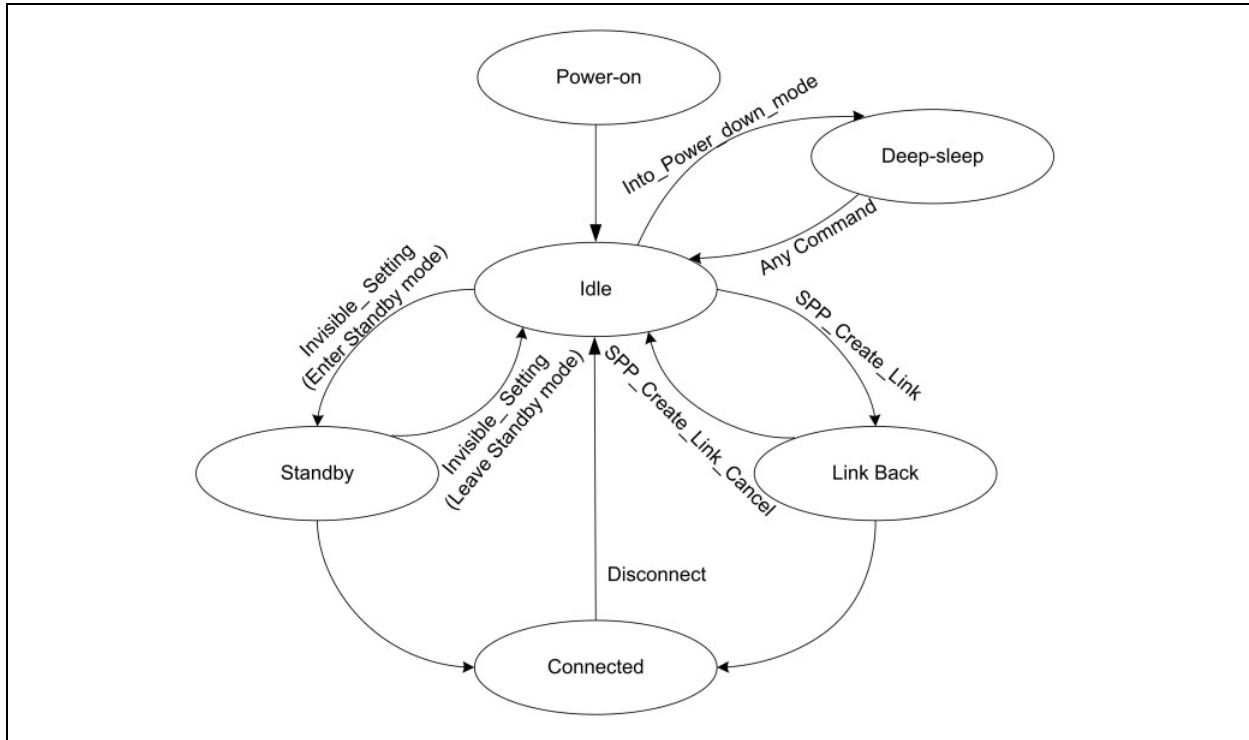
The Manual Pattern mode also allows the Transparent UART mode. There is a small difference in the protocols followed in the Manual Pattern mode and the Auto Pattern mode. For more details on the protocol differences, refer to the "*IS1678 UART Command Set User Guide*".

To evaluate and test the IS1678 SoC in Manual Pattern mode, download and install the Manual Pattern tool (Windows-based GUI emulation tool) which is available at Microchip web site. This tool implements the communication protocol for Manual Pattern mode. It also provides a fast and easy way to test the functions and options available in the Manual Pattern mode.

> **Note:** The Manual Pattern tool and "*IS1678 UART Command Set User Guide*" document, are available for download from the Microchip web site at:
> www.microchip.com/IS1678.

NOTES:

4.0   TRANSCEIVER

The IS1678S/SM SoC is designed and optimized for Bluetooth v2.4 GHz system. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock for synchronization with another device.

4.1   Transmitter

The internal power amplifier (PA) has a maximum output power of +4 dBm (+2 dBm typical). This is applied as an input to the Class 2 or Class 3 radios without external RF PA.

The transmitter performs IQ conversion to minimize the frequency drift, and it can exceed 12 dB power range with temperature compensation mechanism.

4.2   Receiver

The low-noise amplifier (LNA) operates with transmit/receive combined mode for single port application. It can save a pin on the package and without having an external Tx/Rx switch.

The ADC is used to sample the input analog signal and convert it into digital signal for de-modulator analysis. A channel filter has been integrated into the receiver channel before the ADC, which is used to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject image frequency for low-IF architecture. This filter for low-IF architecture is intended to reduce external Band Pass Filter (BPF) component for super heterodyne architecture.

The RSSI signal feed back to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

4.3   Synthesizer

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside, with a tunable internal LC tank that can reduce the variation for components. A crystal oscillator with an internal digital trimming circuit provides a stable clock for the synthesizer.

4.4   Modem

For Bluetooth 1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth 2.0 with EDR specification.

For Bluetooth 2.0 with EDR specification, EDR is introduced to provide data rates of 1 Mbps, 2 Mbps, and 3 Mbps. The BDR/EDR modes have fast transmission rates or high throughput.

The LE mode saves current consumption. This enhanced data rate modem meets EDR requirements of Bluetooth 2.0 with EDR specification. From the viewpoint of baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8 DPSK.

4.5   Adaptive Frequency Hopping (AFH)

The IS1678S/SM SoC has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose clear channel for the transceiver Bluetooth signal.

NOTES:

5.0   ELECTRICAL CHARACTERISTICS

This section provides an overview of the IS1678S/SM SoC electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the IS1678S/SM SoC are listed below. Exposure to the maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

Ambient temperature under bias...-20°C to +70°C

Storage temperature .... -40°C to +125°C

Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +3.6V

Voltage on any pin with respect to V_{SS} ....-0.3V to (V_{DD} + 0.3V)

Maximum output current sink by any I/O pin...12 mA

Maximum output current sourced by any I/O pin...12 mA

Note:	Stresses listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Table 5-1 through Table 5-8 provides the recommended operating conditions and the electrical specifications of the IS1678S/SM SoC.

TABLE 5-1: RECOMMENDED OPERATING CONDITIONS

Rating		Min.	Typical	Max.
Ambient Operating temperature range		-20ºC	+25ºC	+70ºC
Relative Humidity (Operating)		10%	—	90%
Relative Humidity (Storage)		10%	—	90%
ESD	HBM	—	±2KV	—
	MM	—	±200V	—
HTOL **(Note 1)**		—	1000 hrs	—
Supply voltage: BAT_IN		3.3V	—	4.2V
Supply voltage: VDD_IO		3.0V	3.3V	3.63V
Supply voltage: LDO18_IN		3.0V	3.3V	3.63V
Supply voltage: 1V8, VCC_RF, VDD_XO and AVDD_SAR		1.8V	1.9V	2.1V
SW_BTN		3.3V	—	4.2V
LED1		—	—	3.6V
Reset $V_{TH,res}$ threshold voltage		—	1.6V	—
V_{IL} input logic levels low		-0.3V	—	0.8V
V_{IH} input logic levels high		2.0V	—	3.6V
V_{OL} output logic levels low (I_{OL} = 12 mA)		—	—	0.4V
V_{OH} output logic levels high (I_{OH} = 12 mA)		2.4V	—	—
RF continuous Tx mode		—	—	43 mA
RF continuous Rx mode		—	—	37 mA

Note 1: HTOL life test condition: +125ºC, BAT_IN = 4.2V, LDO33_O = 3.3V, LDO18_O = 1.9V.

TABLE 5-2: 1.8V LDO ELECTRICAL PARAMETERS

Parameter	Min.	Typical	Max.	Unit
Operating Temperature	-20	—	+70	ºC
Output Current (V_{IN} = 3.0V/load regulation with 80mV drop)	—	100	—	mA
Quiescent Current (V_{in} < 3.0V)	—	13	—	µA

Note 1: With 1 µF capacitor at LDO18_O as the condition for IP verification.

2: Output voltage can be calibrated by using the MP tool.

TABLE 5-3: 3.3V LDO ELECTRICAL PARAMETERS

Parameter	Min.	Typical	Max.	Unit
Operating Temperature	-20	—	+70	ºC
Output Current (V_{IN} = 3.6V/load regulation with 100 mV drop)	—	100	—	mA
Quiescent Current (V_{IN} = 3.6V)	—	150	—	µA

Note 1: With 10 µF capacitor at LDO33_O as the condition for IP verification.

2: Output voltage can be calibrated by using the MP tool.

TABLE 5-4:   PMU LDO ELECTRICAL PARAMETERS

Parameter	Min.	Typical	Max.	Unit
Operating Temperature	-20	—	+70	ºC
Output Current (V_{IN} = 3.6V/load regulation with 0.3 mV drop)	—	100	—	µA
Quiescent Current (V_{IN} = 3.6V)	—	120	—	µA

Note 1:   With 1 µF capacitor at PMULDO_O as the condition for IP verification.

2:   Output voltage can be calibrated by using the MP tool.

TABLE 5-5:   SAR-ADC AND BATTERY VOLTAGE DETECTOR

Parameter	Min.	Typical	Max.	Unit
Operating Temperature	-20	—	+70	ºC
AVDD_SAR power supply	—	1.8	—	V
SAR_BAT detection **(Note 1)**	3.3	—	4.2	V
Resolution	—	10	—	bit
Operating Current (including bandgap)	—	—	1	mA
Deep-sleep Current	—	—	1	µA

Note 1:   SAR_BAT is connected with BAT_IN internally for battery voltage detection.

TABLE 5-6:   INTENSITY CONTROLLABLE DRIVER

Parameter	Min.	Typical	Max.	Unit
Operating Temperature	-20	—	+70	ºC
Open-drain Voltage	—	—	3.6	V
Current Step	—	0.3	—	mA
Programmable Current Range	0	—	5	mA
Intensity control	—	16	—	step
Power Down Open-drain Current	—	—	1	µA
Deep-sleep Current	—	—	1	µA

TABLE 5-7:   POWER CONSUMPTION CLASSIC

Test Condition	Current (avg.) (mA)	Remarks
Standby mode	2.543	—
Deep-sleep mode	0.187	—
Connected + Sniff, Master (no data)	0.541	No data was transmitted Sniff interval = 500 ms
Connected + Sniff, Slave (no data)	0.551	No data was transmitted Sniff interval = 500 ms
Data, Master	10.67	(Data transmitted at 115200 bps; block size = 500)
Data, Slave	14.87	(Data transmitted at 115200 bps; block size = 500)

Note: The classic BR/EDR and UART_RX_IND functions are enabled.

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TABLE 5-8: POWER CONSUMPTION ENERGY

Test Condition	Current (avg.) (mA)	Remarks
Deep-sleep mode	0.13	—
LE fast advertising	1.21	LE fast advertising interval = 100 ms
	0.88	LE fast advertising interval = 160 ms
	0.48	LE fast advertising interval = 500 ms
	1.72	LE fast advertising interval = 100 ms + Beacon 100 ms
	0.62	LE fast advertising interval = 500 ms + Beacon 500 ms
Reduced Power advertising	0.39	LE Reduced Power advertising interval = 961 ms
	1.00	LE Reduced Power advertising interval = 961 ms + Beacon 100 ms
	0.51	LE Reduced Power advertising interval = 961 ms + Beacon 500 ms
Connected (No data)	0.39	Connection interval = 1500 ms
	0.43	Connection interval = 600 ms
Connected (iPhone 6 to IC)	0.45	Connection interval = 500 ms
	0.60	Connection interval = 200 ms
Connected (IC to iPhone 6)	6.6	Connection interval = 500 ms
	7.0	Connection interval = 200 ms

Note: Low Energy, RX_IND function is enabled.

6.0   RADIO CHARACTERISTICS

Table 6-1 provides the transmitter performance characteristics of the IS1678S/SM SoC.

TABLE 6-1:   TRANSMITTER PERFORMANCE

Basic Data Rate	Min.	Typical	Max.	Bluetooth Specification	Unit
BDR power	—	2	4	-6 to +4	dBm
EDR (2M/3M) power	—	0	4	-6 to +4	
LE power	—	2	4	-20 to +10	

Note 1: The RF Transmit power can be calibrated during production by using the MP tool and the MT8852 Bluetooth test equipment.

2: Test condition: VCC_RF = 1.80V, temperature = +25ºC.

Table 6-2 provides the receiver performance characteristics of the IS1678S/SM SoC.

TABLE 6-2:   RECEIVER PERFORMANCE

Basic Data Rate	Min.	Typical	Max.	Bluetooth Specification	Unit
BDR Sensitivity	—	-90	—	≤ -70	dBm
EDR 2M Sensitivity	—	-90	—		
EDR 3M Sensitivity	—	-82	—		
LE Sensitivity	—	-92	—		

Note: Test condition: VCC_RF = 1.80V, temperature = +25ºC.

NOTES:

7.0 PACKAGE INFORMATION

7.1 Package Marking Information

Figure 7-1 illustrates the package marking information
of the IS1678S/SM SoC.

FIGURE 7-1: **IS1678S/SM SOC PACKAGE MARKING INFORMATION**

40 -Lead QFN (6x6x0.9 mm)

iSSC
XXXXXXXXXX
XXXXXXXXXX
YYWWNNN

iSSC
IS1678S
203 (e3)
1512KT8

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

7.2 Package Details

The following figure illustrates the package details of the IS1678S/SM SoC.

FIGURE 7-2: **IS1678S/SM SOC PACKAGE DETAILS**

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.9	1.00
STAND OFF		A1	0	---	0.05
MOLD THICKNESS		A2	---	---	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.23	0.3
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	4.3	4.5	4.72
	Y	K	4.3	4.5	4.72
LEAD LENGTH		L	0.3	0.38	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

7.3   Footprint Dimensions

The following figure illustrates the footprint dimensions
of the IS1678S/SM SoC.

FIGURE 7-3:   IS1678S/SM SOC FOOTPRINT DIMENSIONS
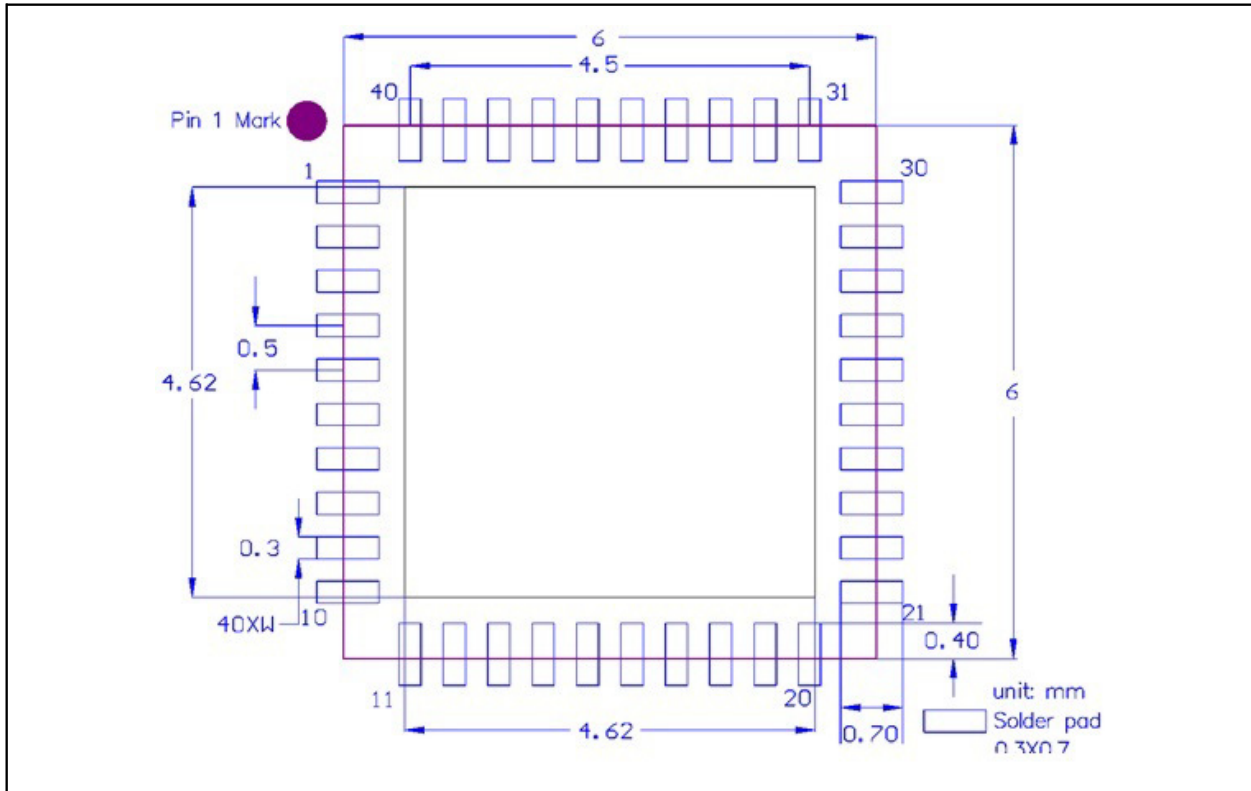
NOTES:

8.0 REFLOW PROFILE AND STORAGE CONDITION

This chapter describes reflow profiles and stencil information of the IS1678 SoC, see Figure 8-1 and Figure 8-2.

8.1 Stencil of SMT Assembly Suggestion

8.1.1 STENCIL TYPE AND THICKNESS

• Laser cutting
• Stainless steel
• Thickness: 0.5 mm pitch, thickness more than 0.15 mm

8.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD

• Aspect ratio (width/thickness) is more than 1.5
• Aperture shape
  - The stencil aperture is designed to match the pad size on the PCB
  - Oval-shape opening is used to get the optimum paste release
  - Rounded corners to minimize the clogging
  - Positive taper walls (5° tapering) with the bottom opening larger than the top opening

8.1.3 APERTURE DESIGN FOR THERMAL PAD

• Small multiple openings are used instead of one big opening, refer Figure 8-1
• 60% to 80% solder paste coverage
• Rounded corners to minimize clogging
• Positive taper walls (5° tapering) with the bottom opening larger than the top opening, see Figure 8-2

FIGURE 8-1:   REFLOW PROFILE

Do not recommend Coverage 91%

Recommend Coverage 77%

Recommend Coverage 65%
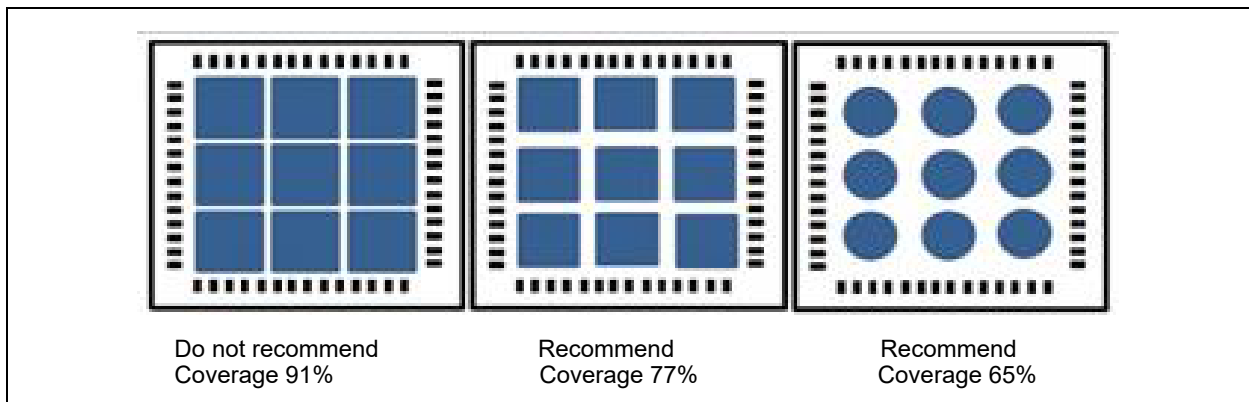
FIGURE 8-2:   STENCIL TYPE
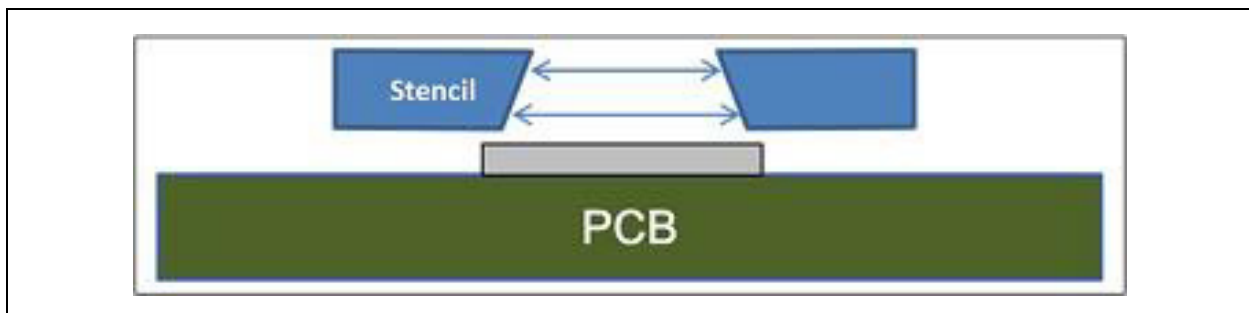
8.2   Reflow Profile

Figure 8-3 illustrates the reflow profile, and the following are specific features of the reflow profile:

- Standard condition: IPC/JEDEC J-STD-020
- Preheat: +150ºC to +200ºC for 60 to 120 seconds
- Average ramp-up rate (+217 ℃ to peak): +3 ℃ /sec max
- Temperature maintained above +217ºC: 60 to 150 seconds

- Time within +5ºC of actual peak temperature: 30 to 40 seconds
- Peak temperature: +260ºC with +5/0ºC tolerance
- Ramp-down rate (peak to +217ºC): +6ºC/sec max
- Time within +25ºC to peak temperature: 8 minutes max
- Cycle interval: 5 minutes

FIGURE 8-3:   REFLOW PROFILE
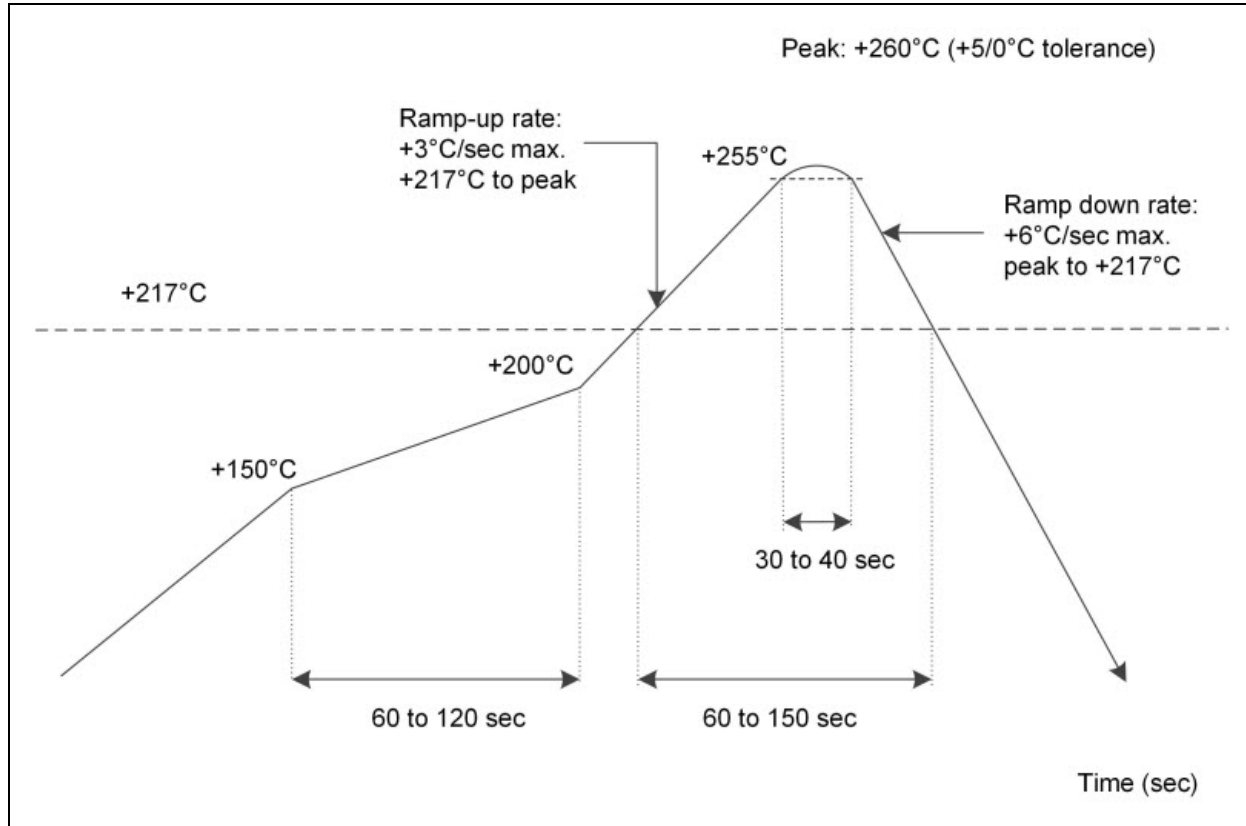
8.3 Storage Condition

Users must follow these specific storage conditions for the IS1678 SoC.

- Calculated shelf life in the sealed bag: 24 months at <+40ºC and <90% relative humidity (RH).
- Once the sealed bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, that is <+30ºC/60% RH.

NOTES:

9.0   ORDERING INFORMATION

Table 9-1 provides the ordering information for the IS1678S/SM SoC.

TABLE 9-1:   ORDERING INFORMATION

Device	Bluetooth Version	Package	Order Number
IS1678SM	Bluetooth 4.2, Flash version	QFN 40 Lead, 6x6x0.9 mm^3, 0.5 mm pitch	IS1678SM-151
IS1678S	Bluetooth 4.2, ROM version	QFN 40 Lead, 6x6x0.9 mm^3, 0.5 mm pitch	IS1678S-152

Note: The IS1678S/SM SoC can be purchased through a Microchip representative. Go to Microchip web site http://www.microchip.com/ for the ordering information.

NOTES:

APPENDIX A: REFERENCE CIRCUIT

Figure 1 and Figure 2 illustrate the reference schematic for the IS1678S/SM
SoC.

FIGURE A-1:   IS1678S/SM SOC REFERENCE CIRCUIT

IS1678
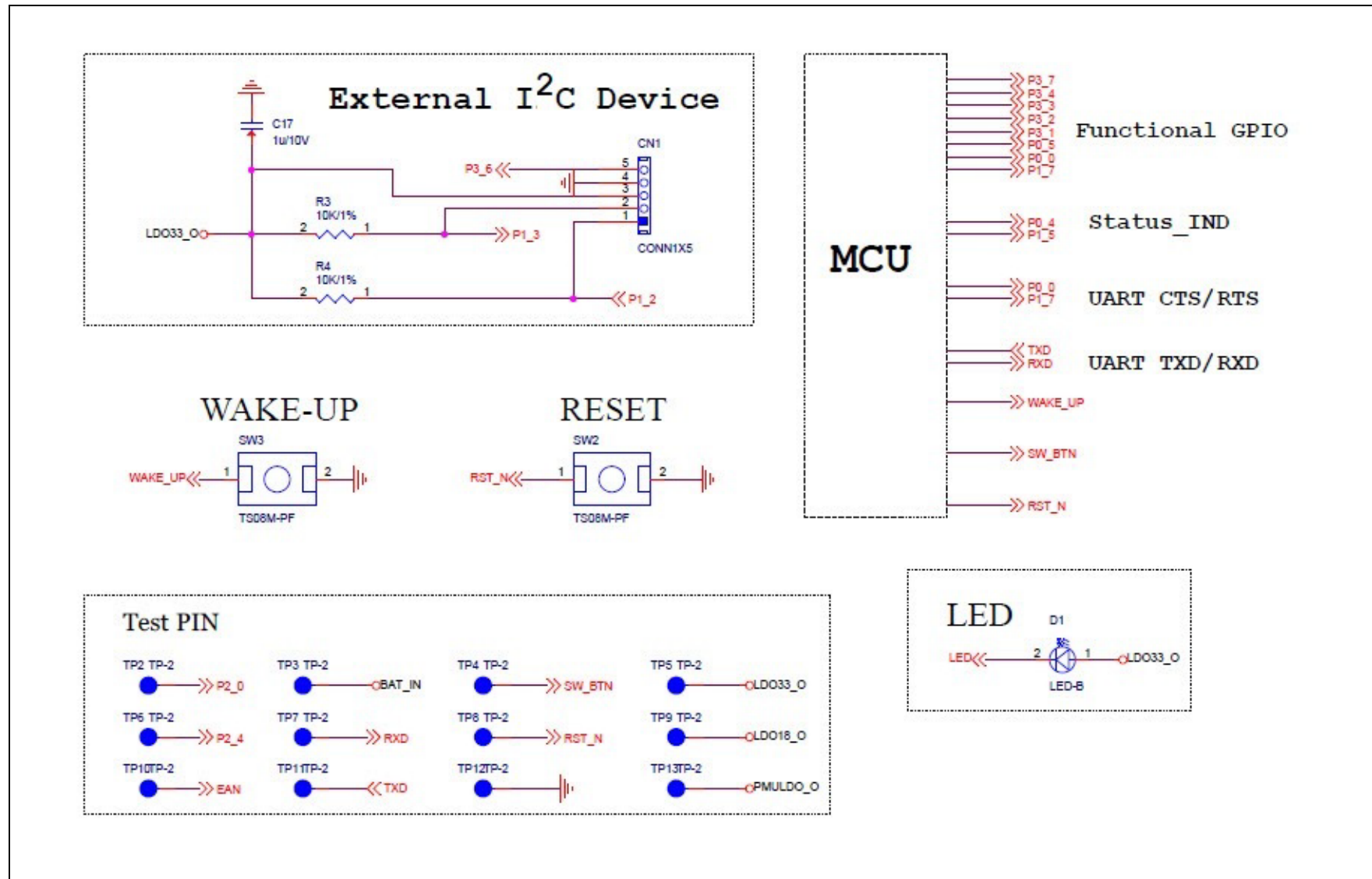
APPENDIX B: REVISION HISTORY

B.1   Revision A (January 2016)

This is the initial released version of this document.

B.2   Revision B (March 2018)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

TABLE B-1:   MAJOR SECTION UPDATES

Section	Update Description
"Data Throughput"	Updated KBps.
1.0 "System Overview"	Updated Table 1-1.
2.0 "Application Information"	Added Table 2-3. Updated Table 2-2, Figure 2-8 and Figure 2-9.
3.0 "Operating Modes"	Updated this section.
7.0 "Package Information"	Deleted **7.4 "Package Information"**.
8.0 "Reflow Profile and Storage Condition"	Updated **8.3 "Storage Condition"**.

B.3   Revision C (December 2020)

Added Figure 7-2 in **7.0 "Package Information"**.

NOTES:

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