International
IOR Rectifier
AN INFINEON TECHNOLOGIES COMPANY

IRS2007(S,M)PBF

200-V half-bridge gate driver IC with V_{CC} & V_{BS} UVLO

Features

- Gate drive supplies up to 20 V per channel
- Undervoltage lockout for V_{CC}, V_{BS}
- 3.3 V, 5 V , 15 V input logic compatible
- Tolerant to negative transient voltage
- Designed for use with bootstrap power supplies
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High-side output in phase with HIN input
- Low-side output out of phase with $\overline{\text{LIN}}$ input
- -40°C to 125°C operating range
- 2 kV HBM ESD
- RoHS compliant

Product Summary

V_{OFFSET}	≤ 200 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typ.)	290 mA & 600 mA
t_{ON} & t_{OFF} (typ.)	160 ns & 150 ns
Deadtime (typ.)	520 ns

Description

The IRS2007 is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 200 V. Propagation delays are matched to simplify the HVIC's use in high frequency applications.

Package Options

8-Lead SOIC

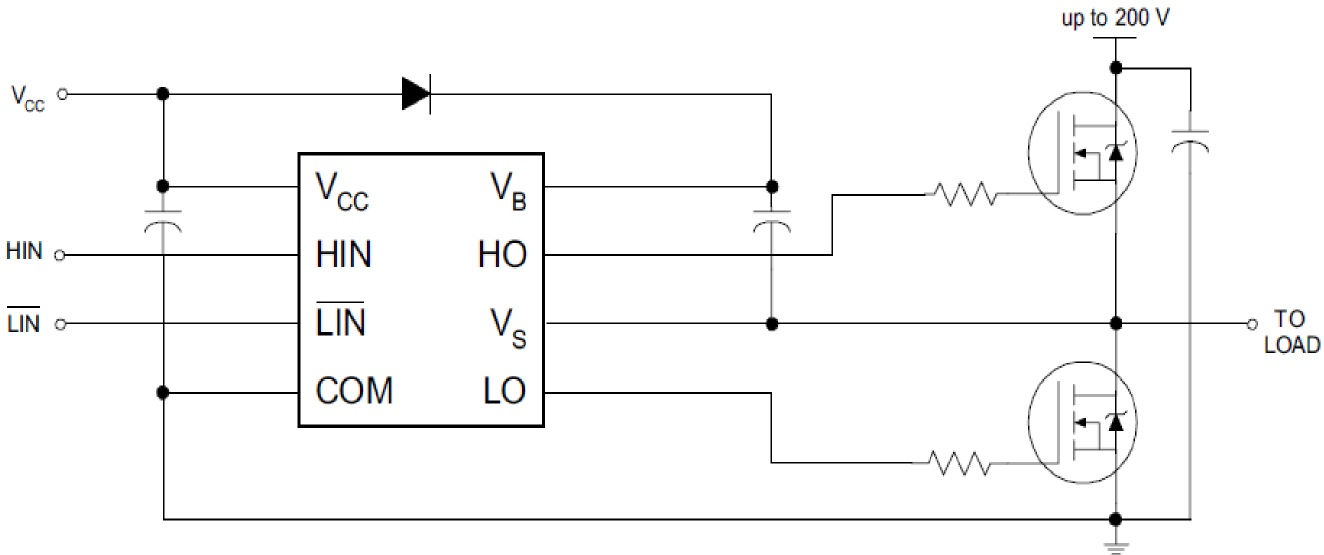
16-Lead MLPQ 4x4
(without 2 leads)

Typical Applications

- Appliance motor drives, Stepper motor, Servo drives
- Micro inverter drives
- General purpose three phase inverters
- Light electric vehicles (e-bikes, e-scooters, e-toys)
- Wireless Charging
- General battery driven applications

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRS2007S	8-Lead SOIC	Tape and Reel	2500	IRS2007STRPBF
		Tube/Bulk	95	IRS2007SPBF
IRS2007M	14-Lead MLPQ 4x4	Tape and Reel	3000	IRS2007MTRPBF

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer tour Application Notes & DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_{CC}	Low side supply voltage		-0.3	25†	V
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		COM - 0.3	V_{CC} + 0.3	
V_B	High-side floating well supply voltage		-0.3	225	
V_S	High-side floating well supply return voltage		V_B- 25	V_B + 0.3	
V_{HO}	Floating gate drive output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low-side output voltage		COM - 0.3	V_{CC} + 0.3	
COM	Power ground		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable V_S offset supply transient relative to COM		—	50	V/ns
P_D	Package power dissipation @ T_A ≤+25ºC	8-Lead SOIC	—	0.625	W
		14-Lead MLPQ 4x4	—	2.08	
Rth_{JA}	Thermal resistance, junction to ambient	8-Lead SOIC	—	200	ºC/W
		14-Lead MLPQ 4x4	—	36	
T_J	Junction temperature		—	150	ºC
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are tested at 25 V.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15V.

Symbol	Definition	Min	Max	Units
V_{CC}	Low-side supply voltage	10	20	V
V_{IN}	Logic input voltage	0	V_{CC}	
V_B	High-side floating well supply voltage	V_S + 10	V_S + 20	
V_S	High-side floating well supply offset voltage†	COM - 8†	200	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{LO}	Low-side output voltage	COM	V_{CC}	
T_A	Ambient temperature	-40	125	ºC

† Logic operation for VS of –8 V to 200 V. Logic state held for V_S of –8 V to –V_{BS}. Please refer to Design Tip DT97-3 for more details.

Static Electrical Characteristics

(V_{CC} - COM) = (V_B - V_S) = 15V. T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

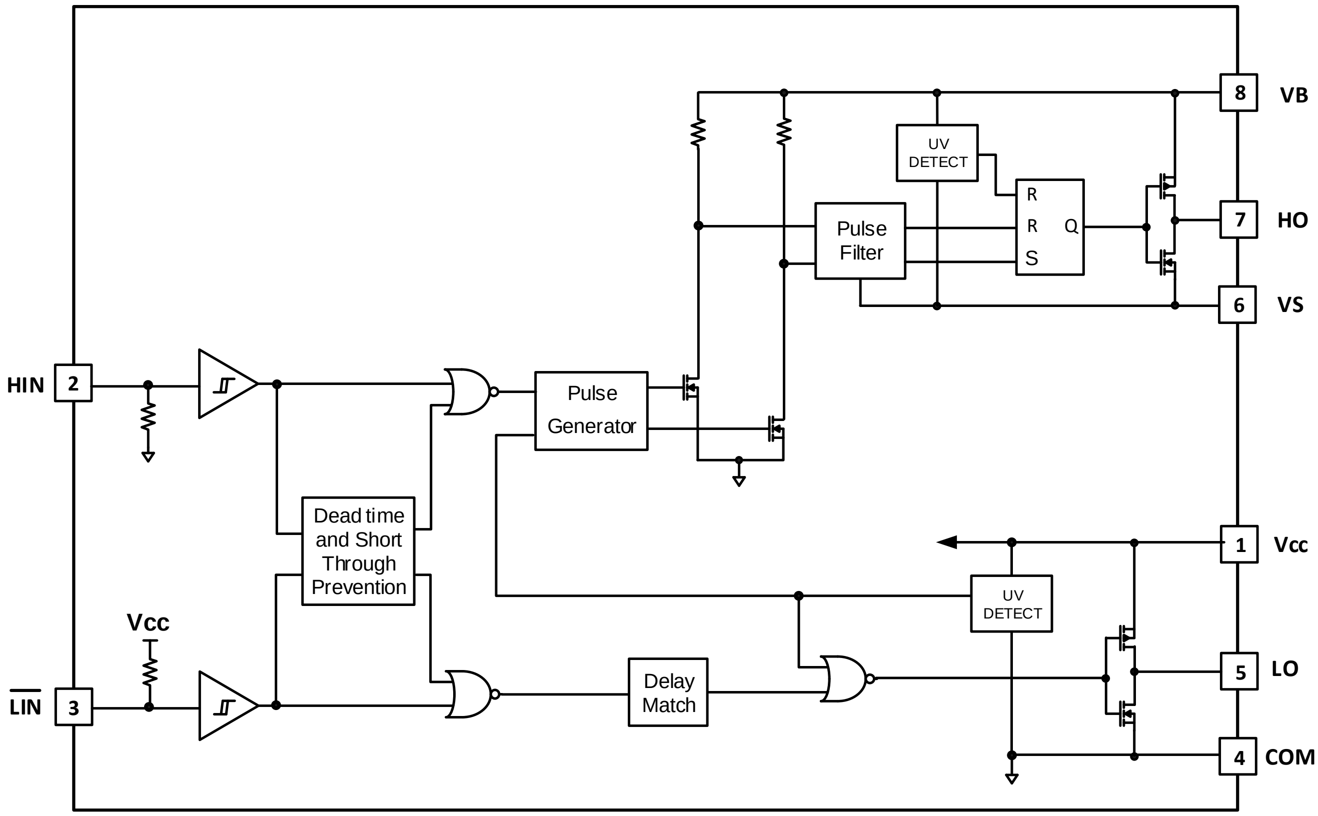
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.4	8.2	9		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	—	0.7	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	—	0.7	—		
I_{LK}	High-side floating well offset supply leakage	—	—	50	µA	V_B = V_S = 200V
I_{QBS}	Quiescent V_{BS} supply current	—	45	75		All inputs are in the off state
I_{QCC}	Quiescent V_{CC} supply current	—	300	520		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	—	0.05	0.2	V	I_O = 2 mA
V_{OL}	Low level output voltage drop, V_O	—	0.02	0.1		
I_{o+}	Output high short circuit pulsed current	200	290	—	mA	V_O = 0V, V_{IN} = V_{IH} PW ≤ 10µs
I_{o-}	Output low short circuit pulsed current	420	600	—		V_O = 15V, V_{IN} = V_{IL} PW ≤ 10µs
V_{IH}	Logic "1" (HIN) & Logic "0" ($\overline{LIN}$) input voltage	2.5	—	—	V	Vcc=10V to 20V
V_{IL}	Logic "0" (HIN) & Logic "1" ($\overline{LIN}$) input voltage	—	—	0.8		
I_{IN+}	Logic "1" Input bias current	—	3	10	µA	HIN = 5V, $\overline{LIN}$= 0V
I_{IN-}	Logic "0" Input bias current	—	—	5		HIN = 0V, $\overline{LIN}$= 5V

Dynamic Electrical Characteristics

V_{CC} = V_B = 15V, V_S = COM, T_A = 25°C, and C_L = 1000pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	—	160	220	ns	V_S = 0V or 200V
t_{OFF}	Turn-off propagation delay	—	150	220		
t_R	Turn-on rise time	—	70	170		V_S = 0V
t_F	Turn-off fall time	—	30	90		
MT	Delay matching time (t_{ON}, t_{OFF})	—	—	50		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MDT	Deadtime matching time ($DT_{LO/HO}$ – $DT_{HO/LO}$)	—	—	30		

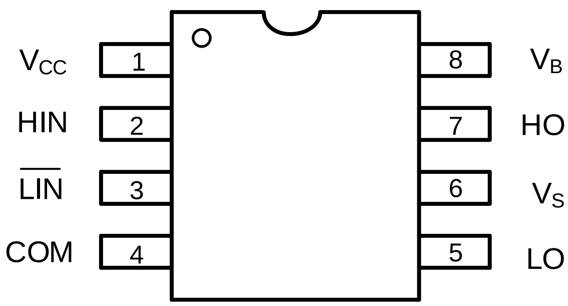
Functional Block Diagram



Lead Definitions

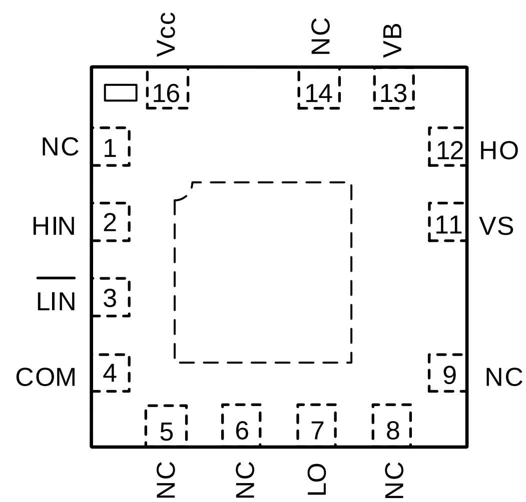
Symbol	Description
Vcc	Low-side and logic supply voltage
VB	High-side gate drive floating supply
VS	High voltage floating supply return
HIN	Logic inputs for high-side gate driver output (HO), in phase
$\overline{\text{LIN}}$	Logic inputs for low-side gate driver output (LO), out of phase
HO	High-side driver output
LO	Low-side driver output
COM	Low-side gate drive return

Lead Assignments



8-Lead SOIC

IRS2007S



16-Lead MLPQ 4x4
(without 2 leads)

IRS2007M

Application Information and Additional Details

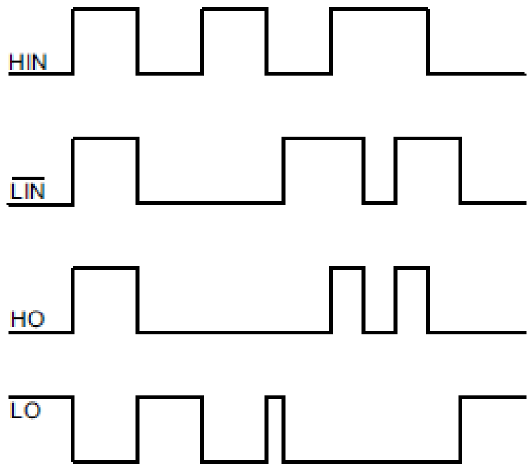


Figure 1. Input/Output Timing Diagram

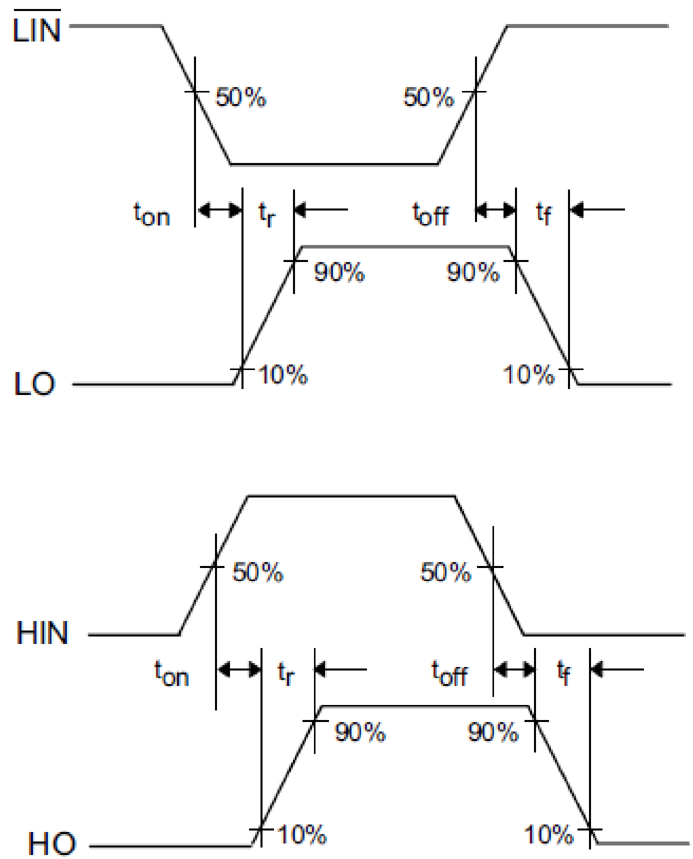


Figure 2. Switching Time Waveform Definitions

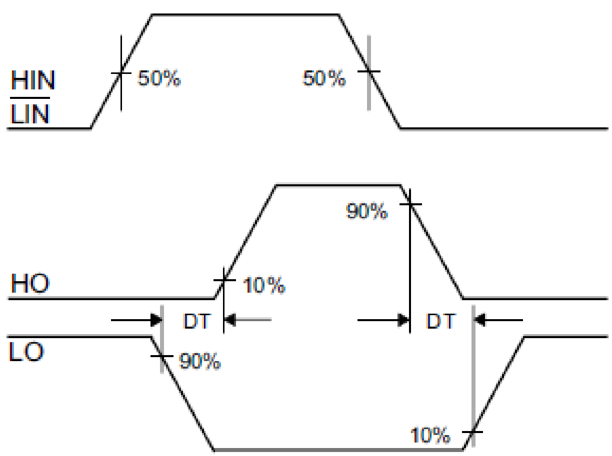


Figure 3. Deadtime Waveform Definitions

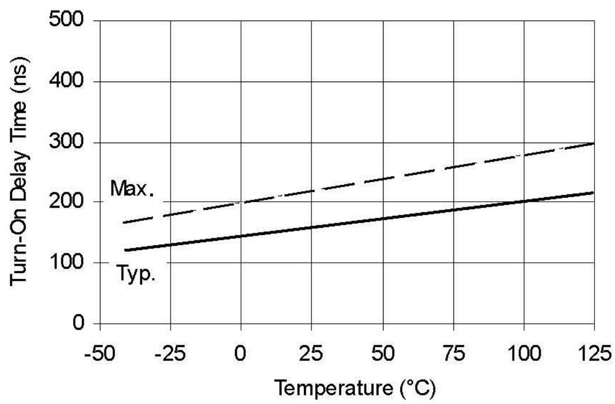


Figure 4A. Turn-On Time vs. Temperature

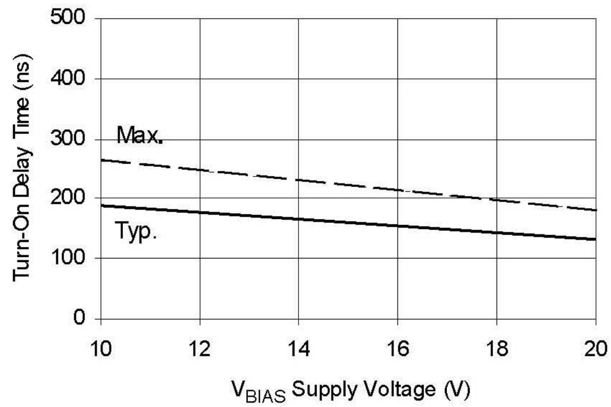


Figure 4B. Turn-On Time vs. Supply Voltage

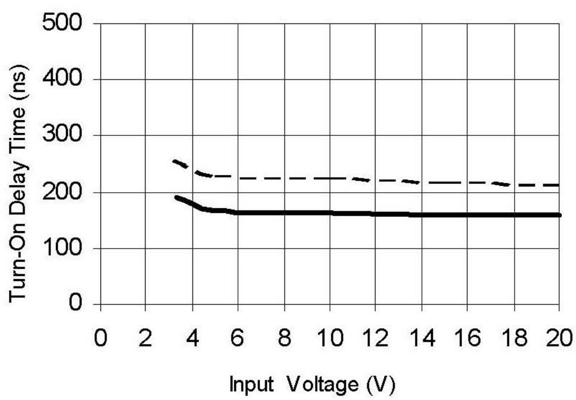


Figure 4C. Turn-On Time vs. Input Voltage

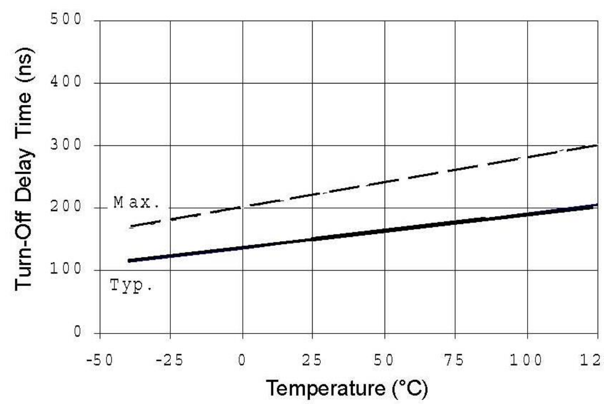


Figure 5A. Turn-Off Time vs. Temperature

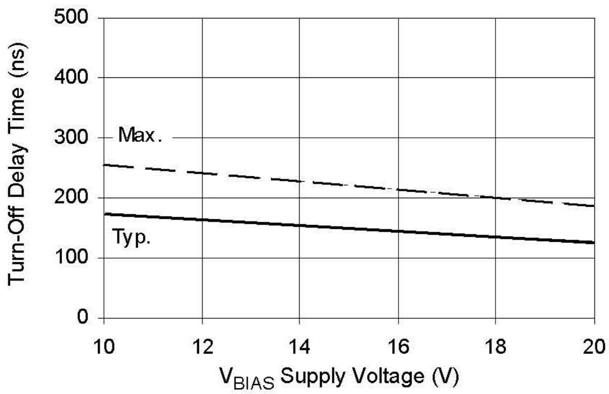


Figure 5B. Turn-Off Time vs. Supply Voltage

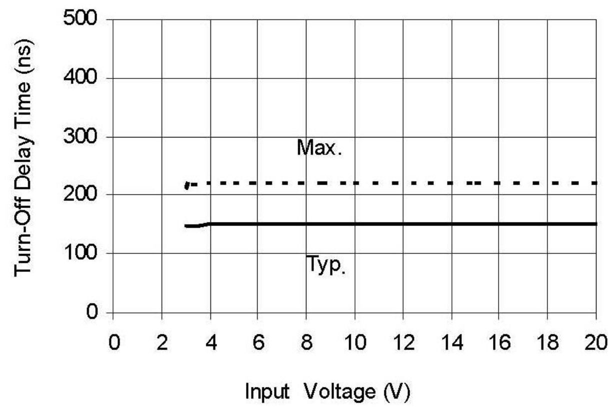


Figure 5C. Turn-Off Time vs. Input Voltage

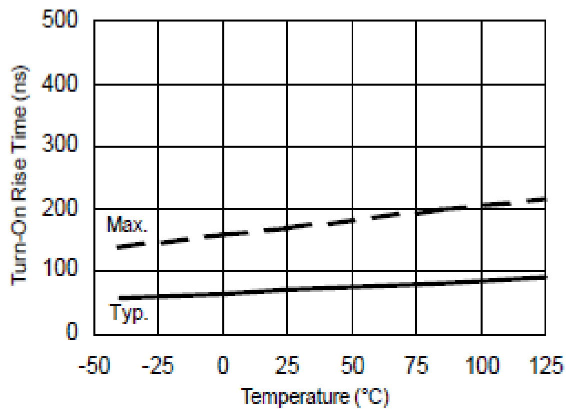


Figure 6A. Turn-On Rise Time vs. Temperature

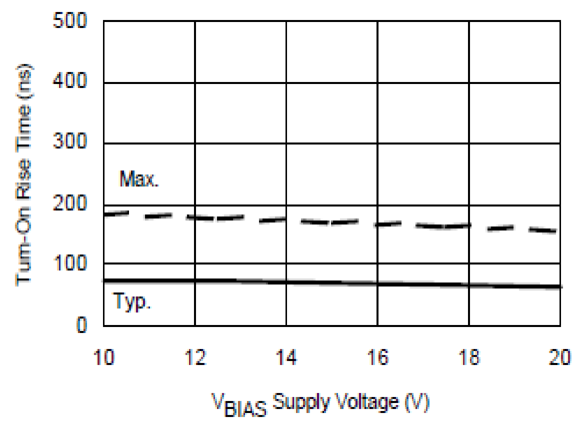


Figure 6B. Turn-On Rise Time vs. Voltage

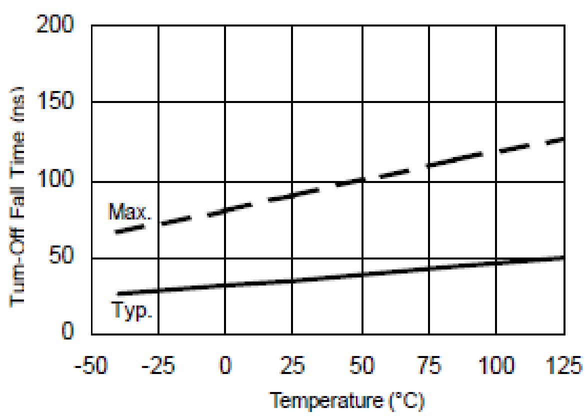


Figure 7A. Turn-Off Fall Time vs. Temperature

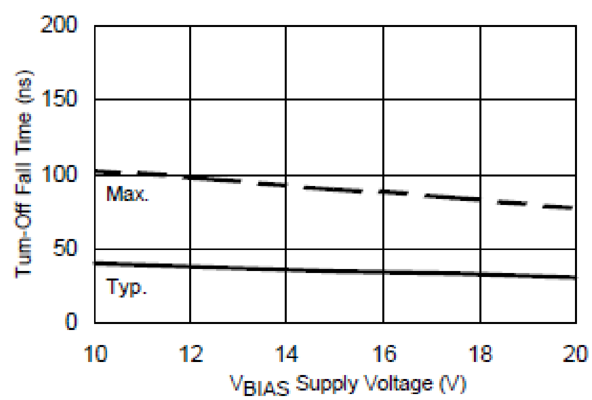


Figure 7B. Turn-Off Fall Time vs. Voltage

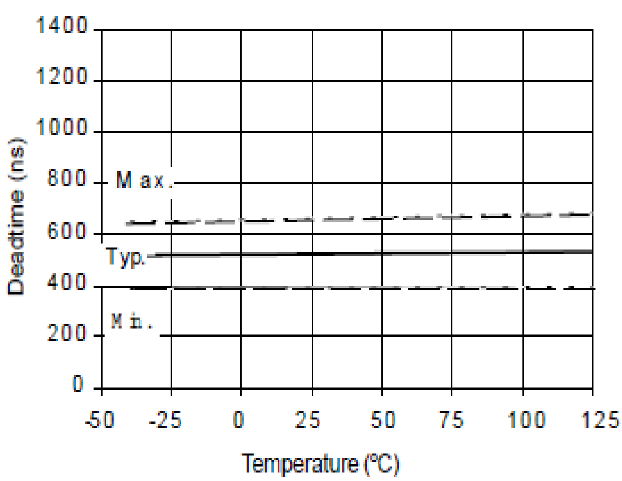


Figure 8A. Deadtime vs. Temperature

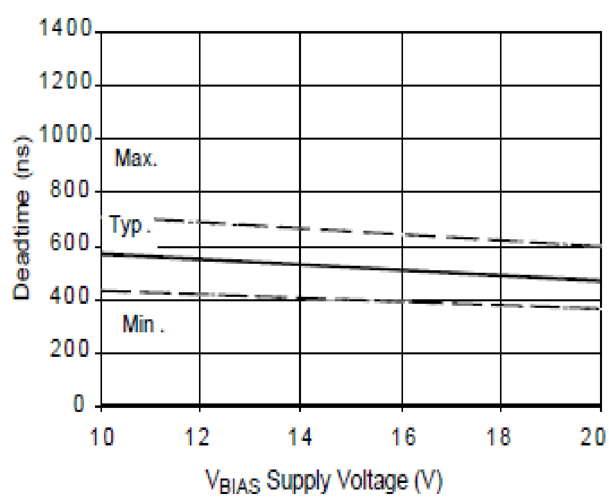


Figure 8A. Deadtime vs. Voltage

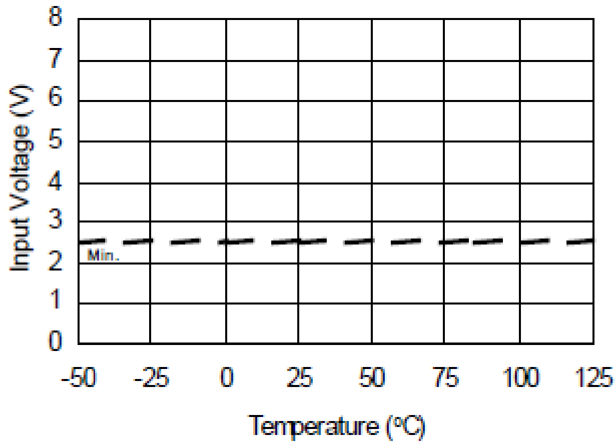


Figure 9A. Logic "1"(HIN) & Logic "0"($\overline{\text{LIN}}$) Input Voltage vs. Temperature

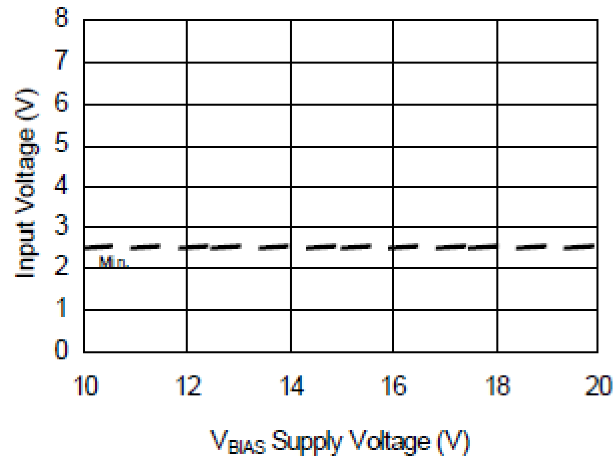


Figure 9B. Logic "1"(HIN) & Logic "0"($\overline{\text{LIN}}$) Input Voltage vs. Voltage

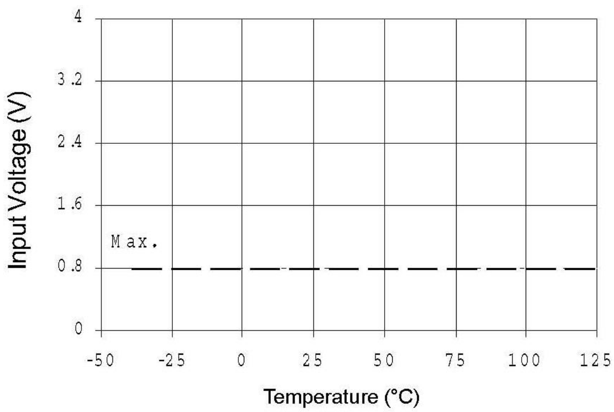


Figure 10A. Logic "0"(HIN) & Logic "1"($\overline{\text{LIN}}$) Input Voltage vs. Temperature

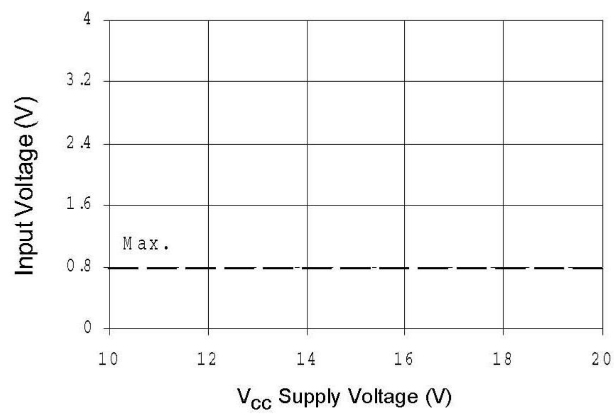


Figure 10B. Logic "0"(HIN) & Logic "1"($\overline{\text{LIN}}$) Input Voltage vs. Voltage

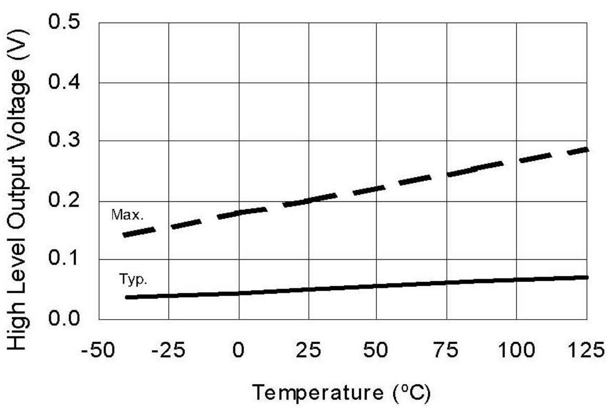


Figure 11A. High Level Output Voltage vs. Temperature

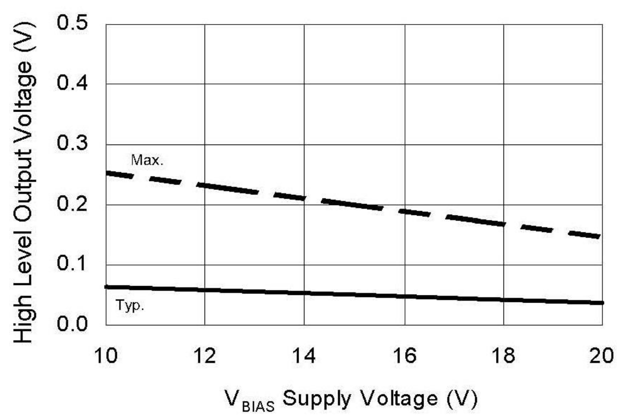


Figure 11B. High Level Output Voltage vs. Supply Voltage

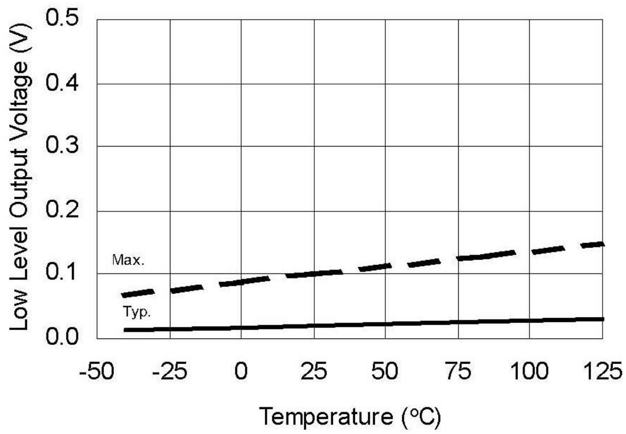


Figure 12A. Low Level Output Voltage vs. Temperature

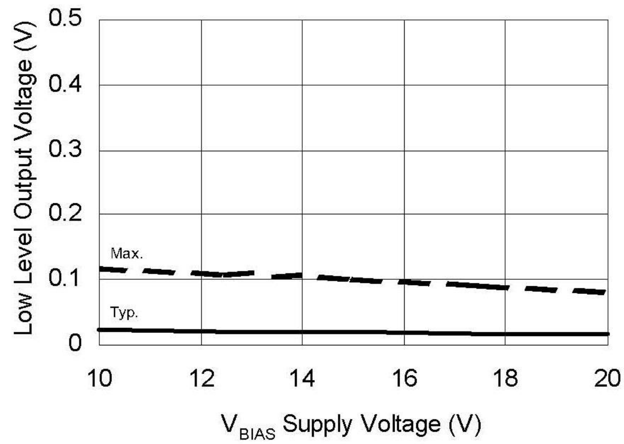


Figure 12B. Low Level Output Voltage vs. Supply Voltage

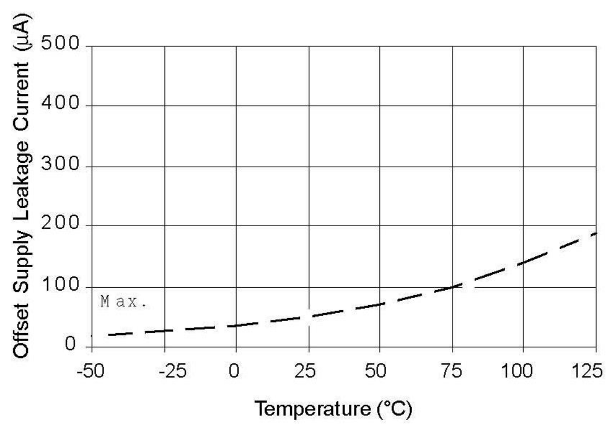


Figure 13A. Offset Supply Current vs. Temperature

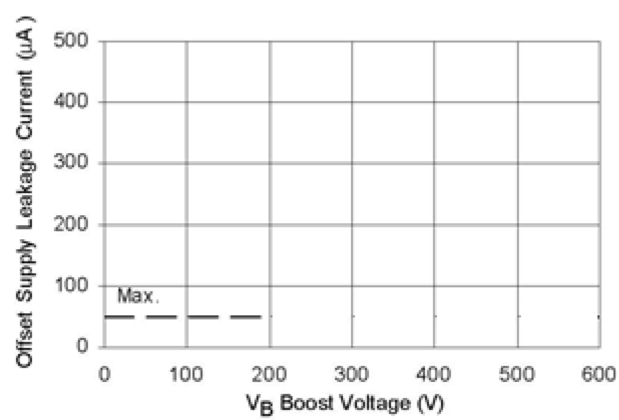


Figure 13B. Offset Supply Current vs. Voltage

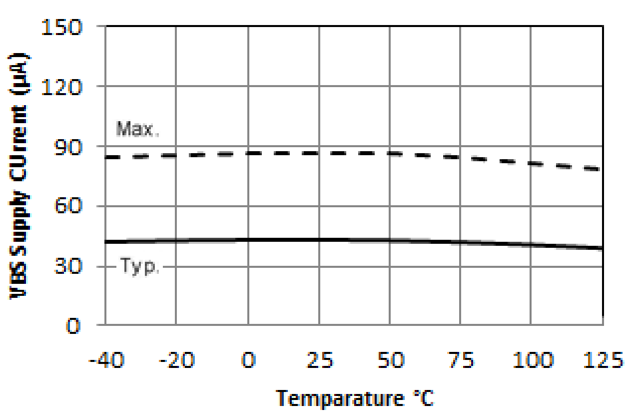


Figure 14A. V_{BS} Supply Current vs. Temperature

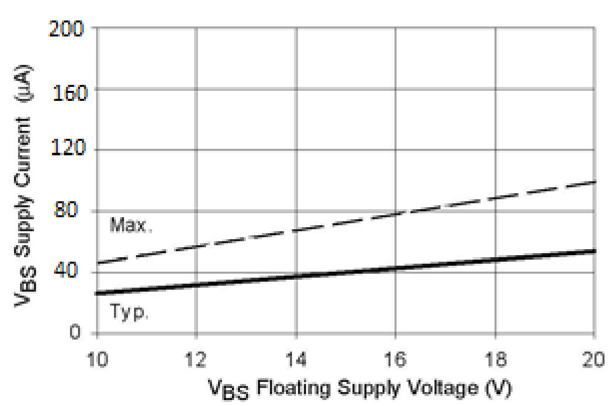


Figure 14B. V_{BS} Supply Current vs. Voltage

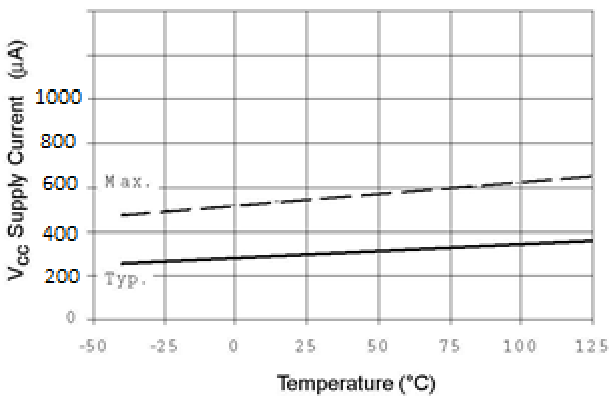


Figure 15A. V_{CC} Supply Current vs. Temperature

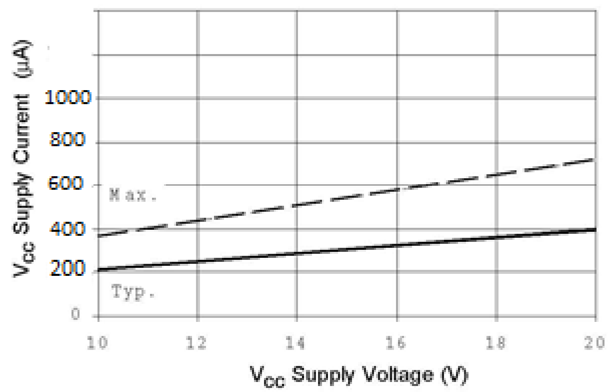


Figure 15B. V_{CC} Supply Current vs. Voltage

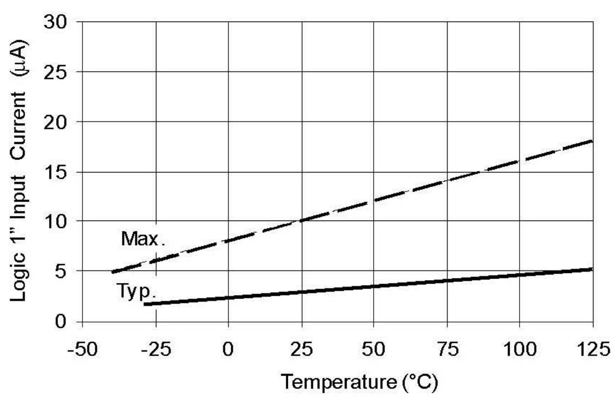


Figure 16A. Logic “1” Input Current vs. Temperature

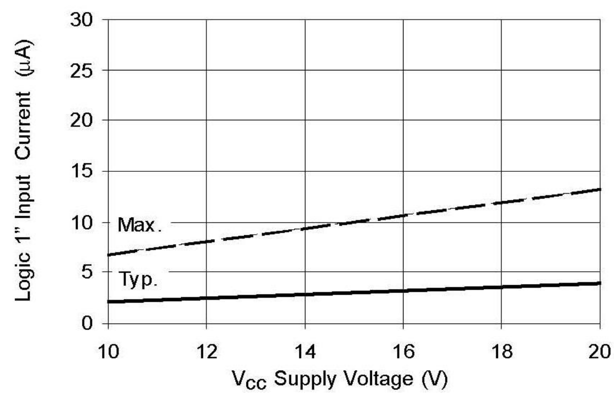


Figure 16B. Logic “1” Input Current vs. Voltage

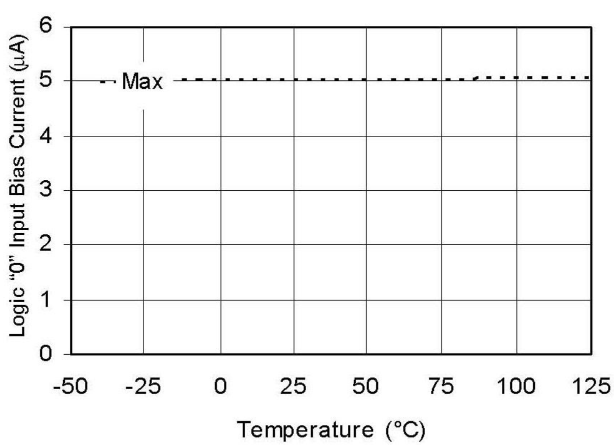


Figure 17A. Logic “0” Input Bias Current

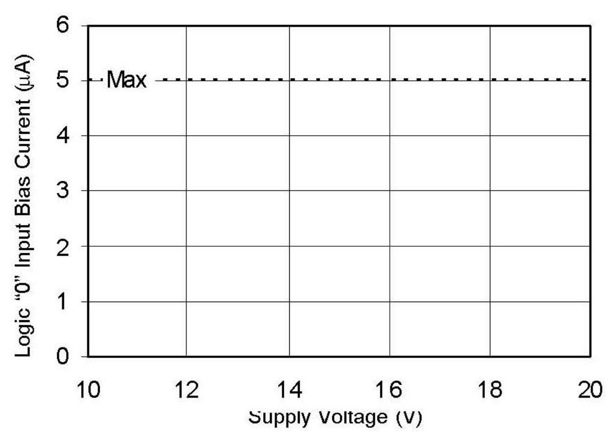


Figure 17B. Logic “0” Input Bias Current

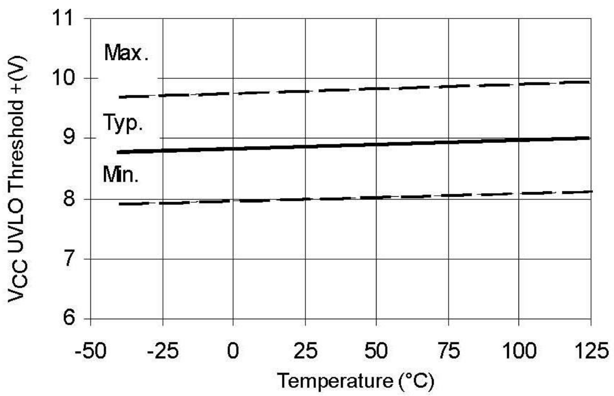


Figure 18A. $V_{CC}\backslash V_{BS}$ Undervoltage Threshold(+) vs. Temperature

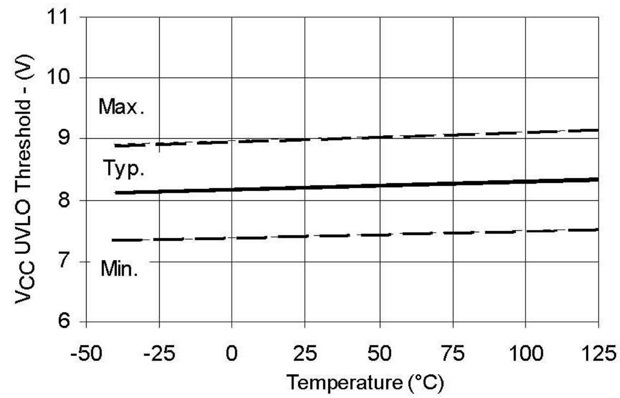


Figure 18B. $V_{CC}\backslash V_{BS}$ Undervoltage Threshold(-) vs. Temperature

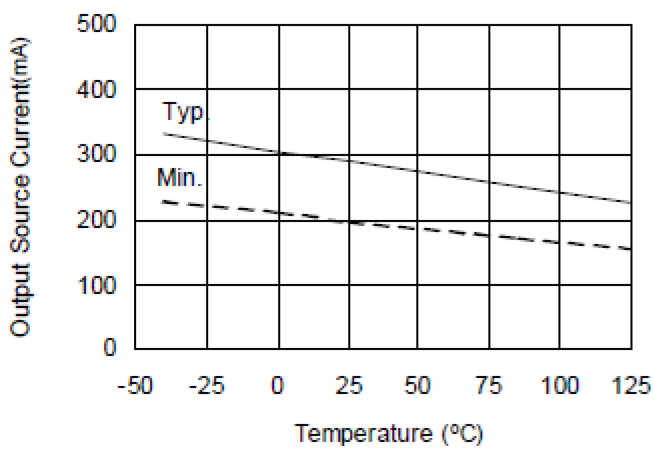


Figure 19A. Output Source Current vs. Temperature

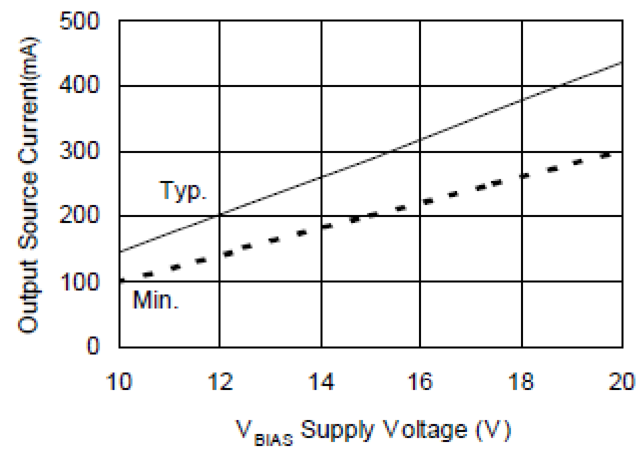


Figure 19B. Output Source Current vs. Supply Current

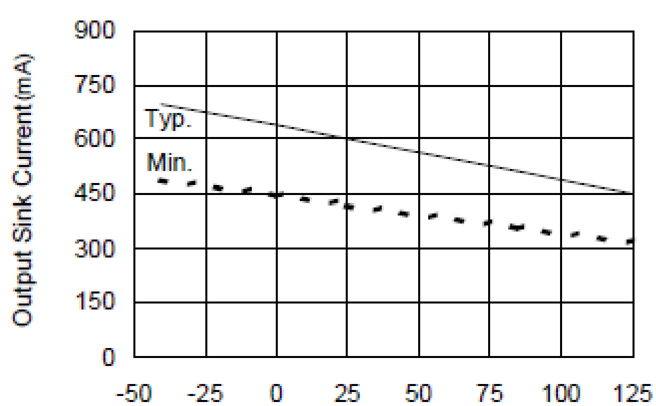


Figure 20A. Output Sink Current vs. Temperature

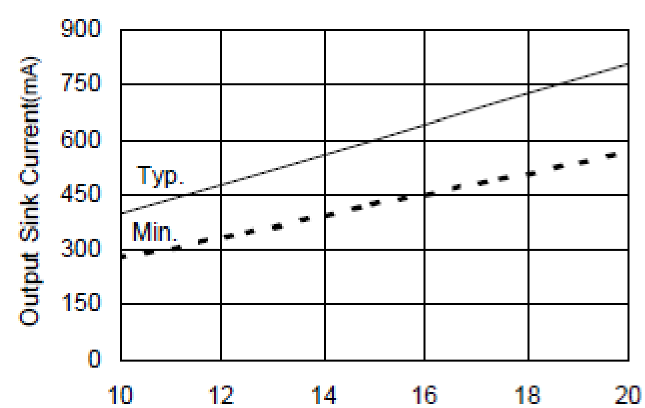
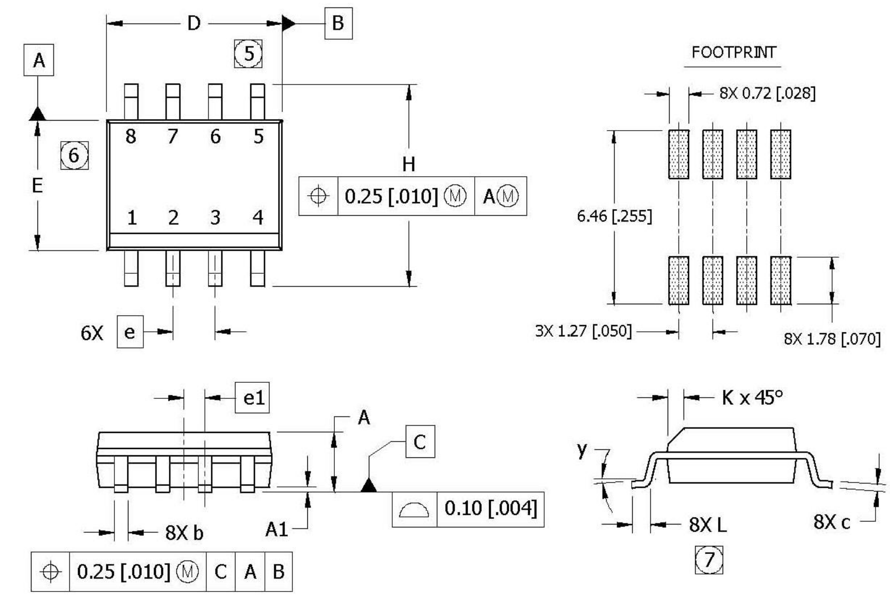


Figure 20B. Output Sink Current vs. Supply Voltage

Package Details: 8-Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

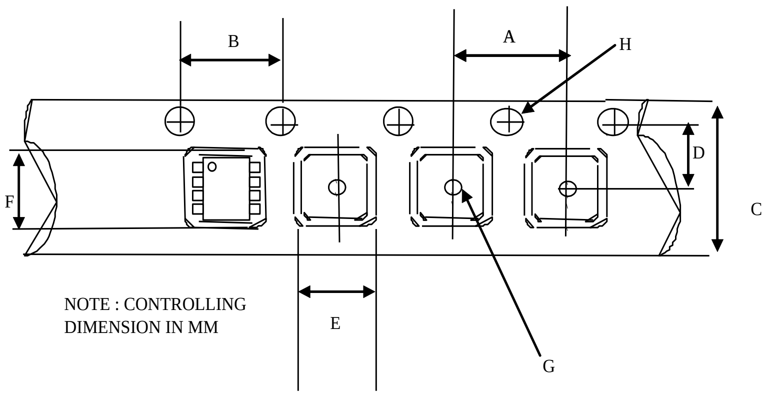
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

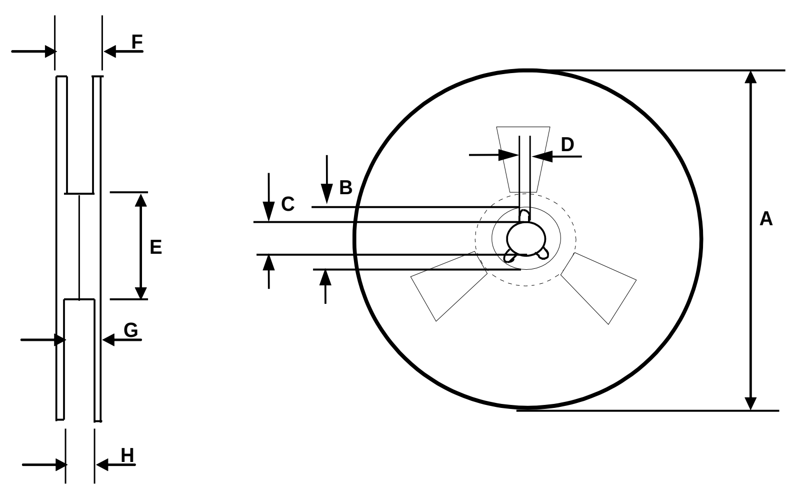
8 Lead SOIC

Tape and Reel Details: 8-Lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

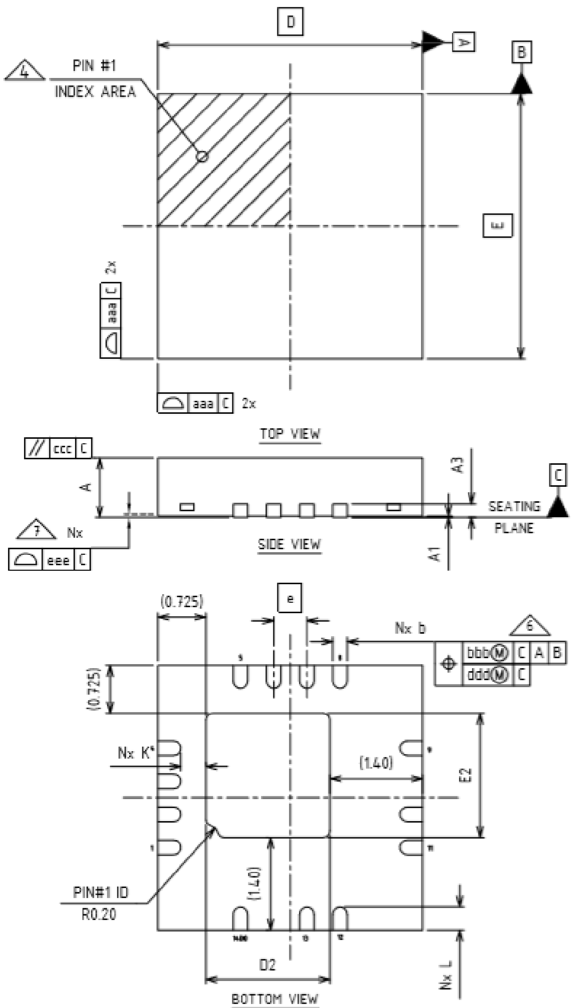
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Package Details: 14-Lead MLPQ 4x4



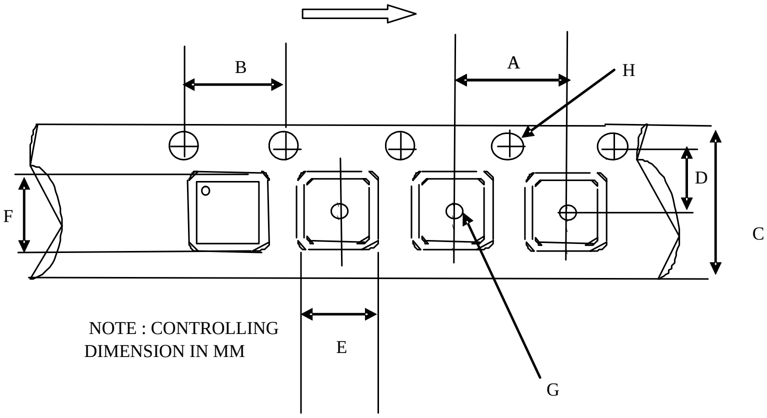
NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on each D and E side respectively.
6. Dimension b applies to the metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metalization.

Dimension Table

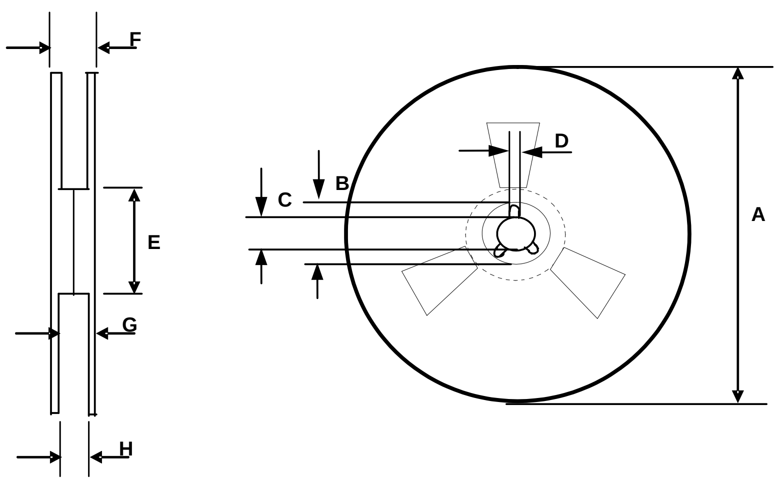
Symbol \ Thickness	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref	---	
b	0.18	0.25	0.30	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	1.725	1.875	1.975	
E2	1.725	1.875	1.975	
K	0.20	---	---	
L	0.25	0.35	0.45	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		14		3
ND		SEE FIGURE		5
NE				
NOTES		1, 2		

Tape and Reel Details: 14-Lead MLPQ 4x4



CARRIER TAPE DIMENSION FOR MLPQ4x4

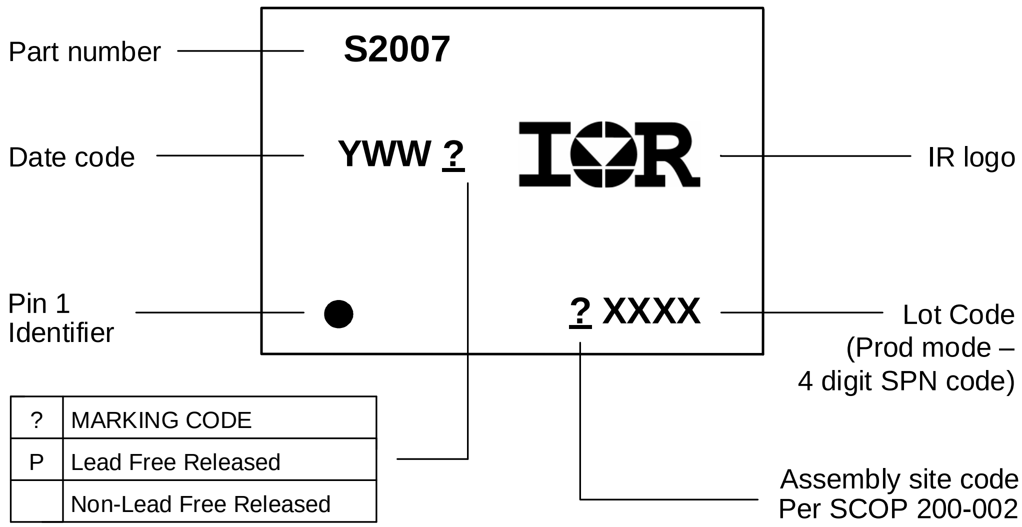
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.358
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.461	0.484
D	5.45	5.55	0.215	0.219
E	4.25	4.45	0.168	0.176
F	4.25	4.45	0.168	0.176
G	1.50	n/a	0.069	n/a
H	1.50	1.60	0.069	0.063



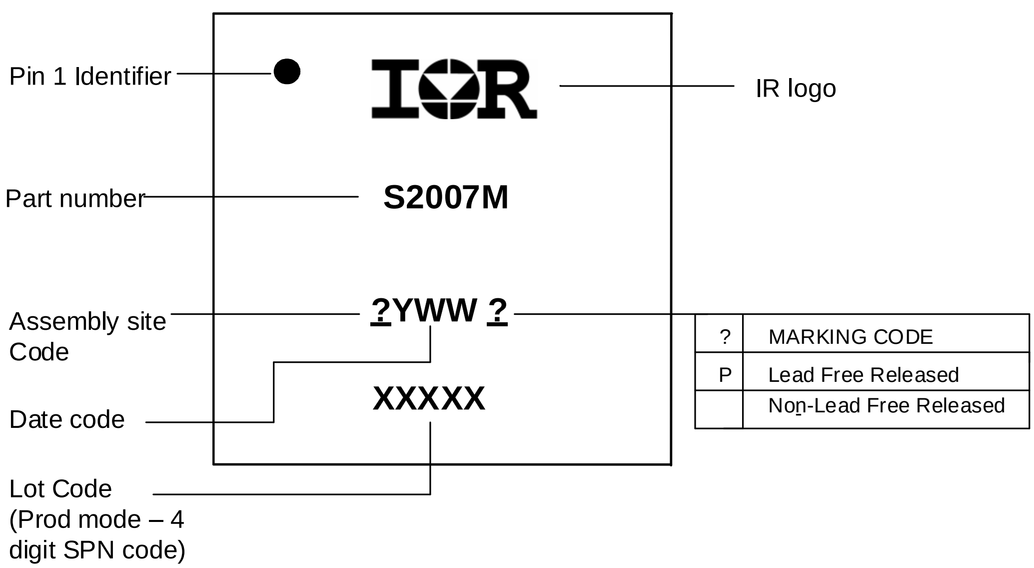
REEL DIMENSIONS FOR MLPQ4x4

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



8-Lead SOIC8
IRS2007SPBF



14-Lead MLPQ 4x4
IRS2007MPBF

Qualification Information†

Qualification Level		Industrial†	
		Comments: This family of ICs is qualified according to relevant tests of JEDEC47/22/20. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		8 Lead SOIC	MSL2††, 260°C (per IPC/JEDEC J-STD-020)
		14-Lead MLPQ 4x4	
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)	
	Machine Model	Class A (per EIA/JEDEC standard EIA/JESD22-A115)	
IC Latch-Up Test		Class I (per JESD78)	
RoHS Compliant		Yes	

† According to IR Qualification Requirements for IC products.
†† Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

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