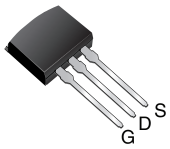
IRLZ14S, IRLZ14L, SiHLZ14S, SiHLZ14L

Vishay Siliconix

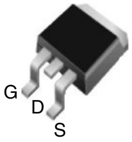
Power MOSFET

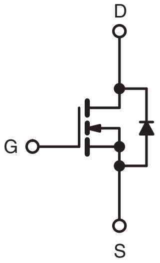
PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	V_{GS} = 5 V	0.20
Q_g (Max.) (nC)	8.4	
Q_{gs} (nC)	3.5	
Q_{gd} (nC)	6.0	
Configuration	Single	

I²PAK (TO-262)



D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Advanced Process Technology
- Surface Mount (IRLZ14S, SiHLZ14S)
- Low-Profile Through-Hole (IRLZ14L, SiHLZ14L)
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC

RoHS* COMPLIANT

HALOGEN FREE Available

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extermely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRLZ44L, SiHLZ44L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D²PAK (TO-263)	D²PAK (TO-263)	D²PAK (TO-263)	I²PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHLZ14S-GE3	SiHLZ14STRL-GE3[a]	SiHLZ14STRR-GE3[a]	-
Lead (Pb)-free	IRLZ14SPbF	-	IRLZ14STRRPbF[a]	IRLZ14LPbF
	SiHLZ14S-E3	-	SiHLZ14STR-E3	SiHLZ14L-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage[e]			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5 V	T_C = 25 °C	I_D	10	A
		T_C = 100 °C		7.2	
Pulsed Drain Current[a, e]			I_{DM}	40	
Linear Derating Factor				0.29	W/°C
Single Pulse Avalanche Energy[b, e]			E_{AS}	68	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	43	W
	T_A = 25 °C			3.7	
Peak Diode Recovery dV/dt[c, e]			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

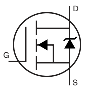
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 790 µH, R_g = 25 Ω, I_{AS} = 10 A (see fig. 12).
c. $I_{SD} \leq 10$ A, dI/dt ≤ 90 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
d. 1.6 mm from case.
e. Uses IRLZ14, SiHLZ14 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB Mount)[a]	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = 250 μA		60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.07	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V		-	-	25	μA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 150 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 5 V	I_D = 6.0 A[b]	-	-	0.2	Ω
		V_{GS} = 4 V	I_D = 5.0 A[b]	-	-	0.28	
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 6.0 A		3.5	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	400	-	pF
Output Capacitance	C_{oss}			-	170	-	
Reverse Transfer Capacitance	C_{rss}			-	42	-	
Total Gate Charge	Q_g	V_{GS} = 5 V	I_D = 10 A, V_{DS} = 48 V, see fig. 6 and 13[b]	-	-	8.4	nC
Gate-Source Charge	Q_{gs}			-	-	3.5	
Gate-Drain Charge	Q_{gd}			-	-	6.0	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 10 A, R_g = 12 Ω, R_D = 2.8 Ω, see fig. 10[b]		-	9.3	-	ns
Rise Time	t_r			-	110	-	
Turn-Off Delay Time	$t_{d(off)}$			-	17	-	
Fall Time	t_f			-	26	-	
Internal Source Inductance	L_S	Between lead, and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	10	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	40	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 10 A, V_{GS} = 0 V[b]		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 10 A, dI/dt = 100 A/μs[b]		-	93	130	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	340	650	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

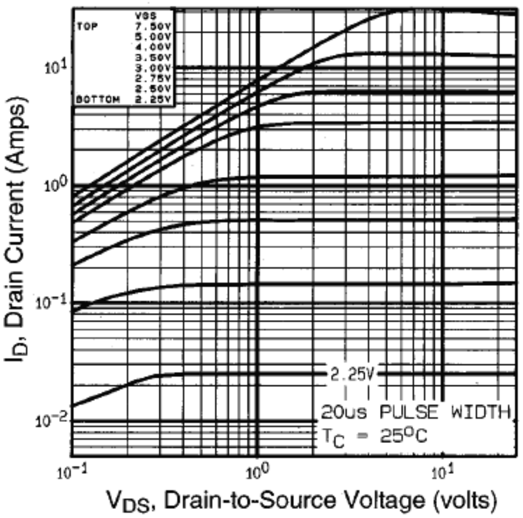


Fig. 1 - Typical Output Characteristics

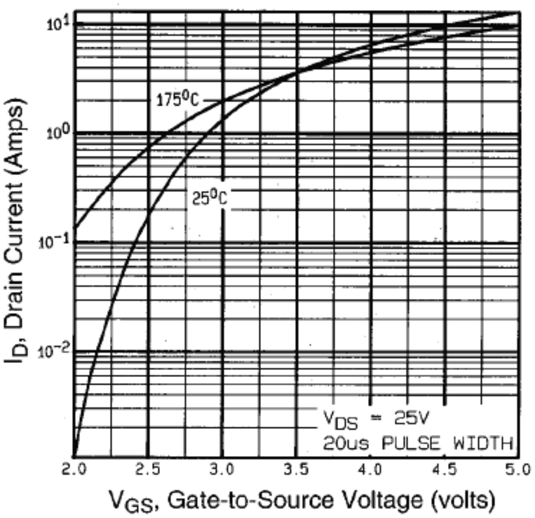


Fig. 3 - Typical Transfer Characteristics

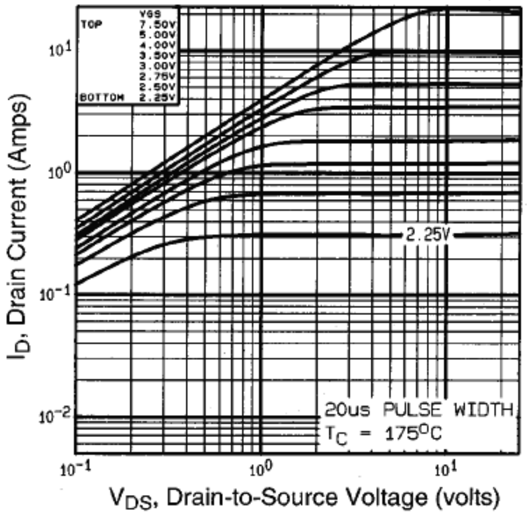


Fig. 2 - Typical Output Characteristics

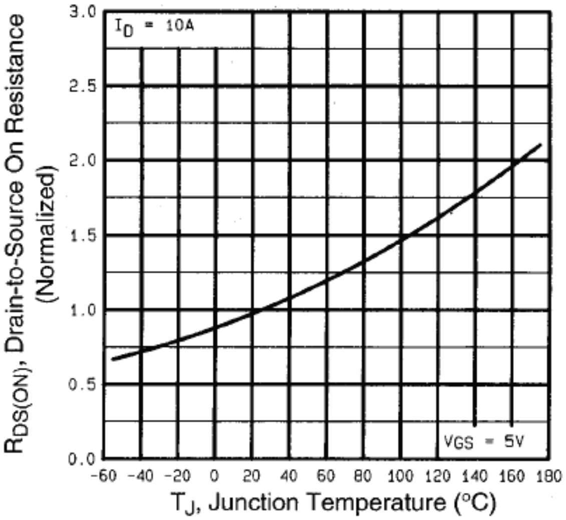


Fig. 4 - Normalized On-Resistance vs. Temperature

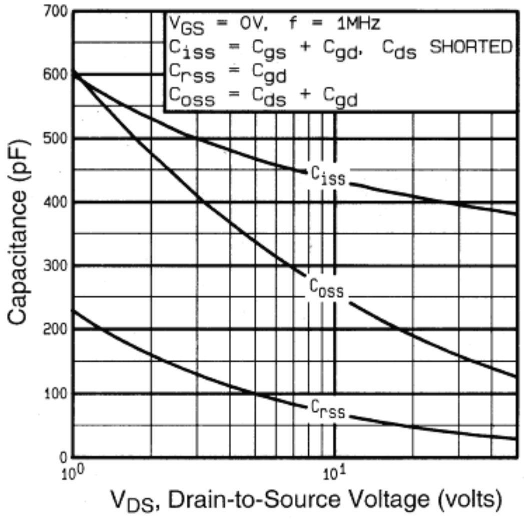


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

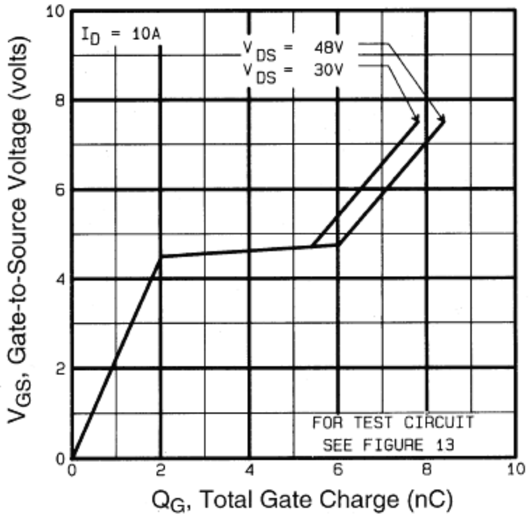


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

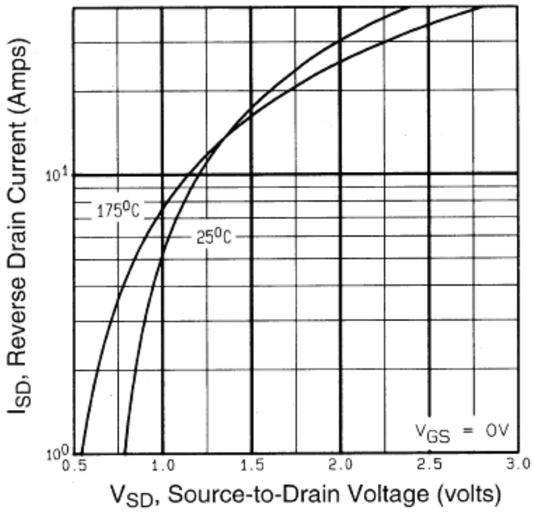


Fig. 7 - Typical Source-Drain Diode Forward Voltage

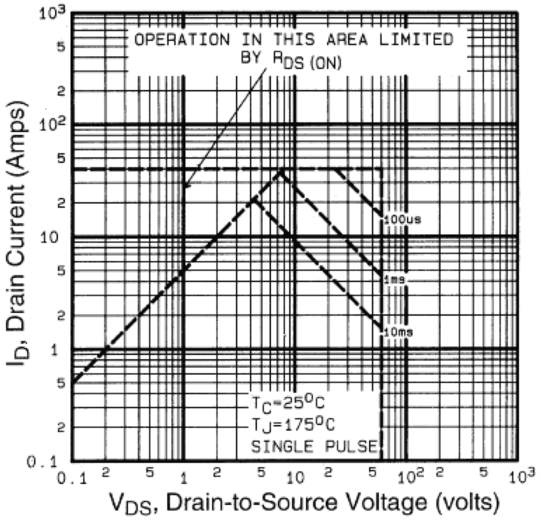


Fig. 8 - Maximum Safe Operating Area

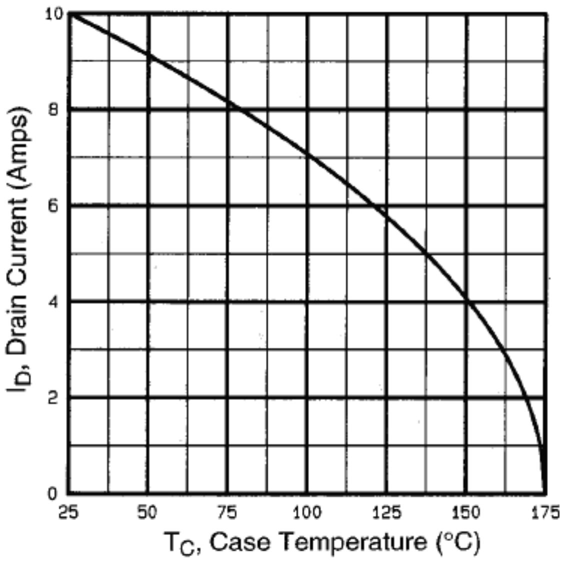


Fig. 9 - Maximum Drain Current vs. Case Temperature

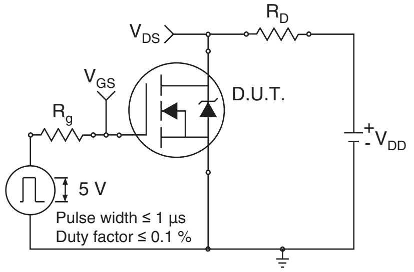


Fig. 10a - Switching Time Test Circuit

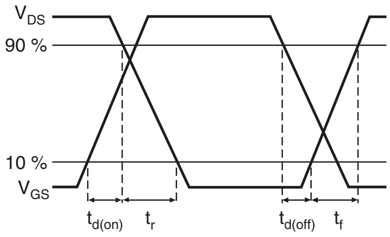


Fig. 10b - Switching Time Waveforms

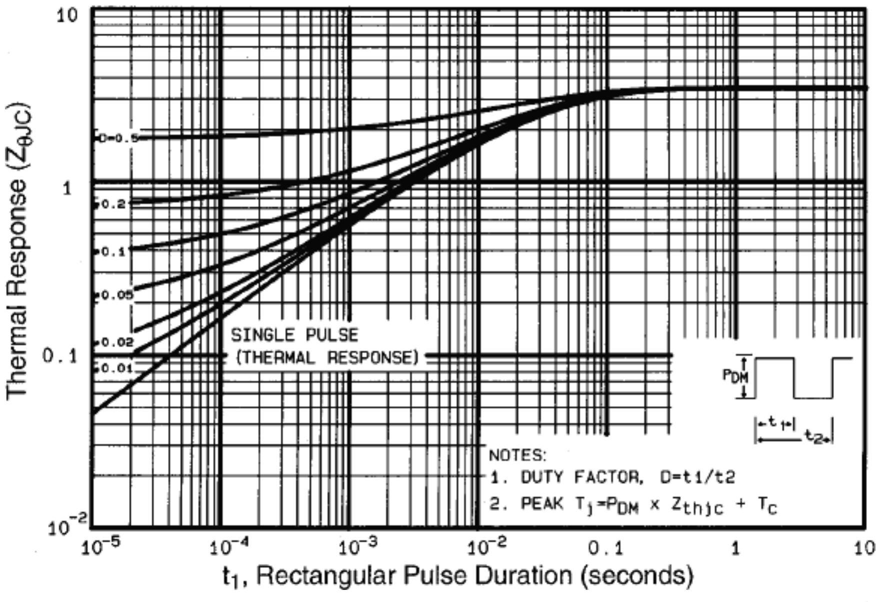


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

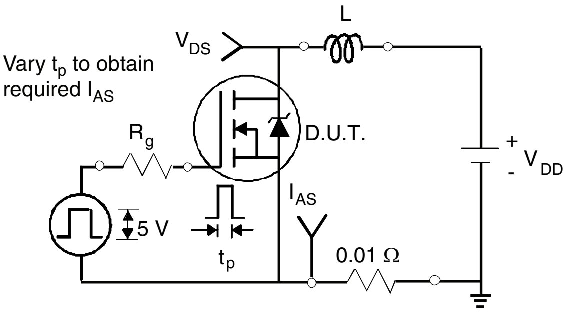


Fig. 12a - Unclamped Inductive Test Circuit

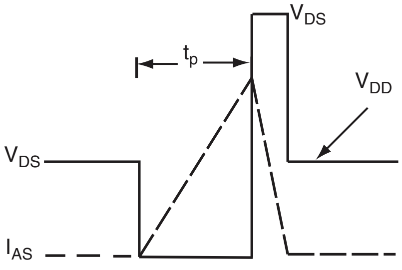


Fig. 12b - Unclamped Inductive Waveforms

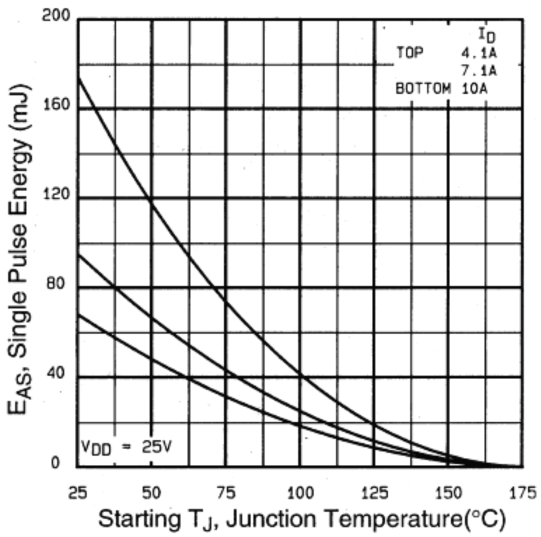


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

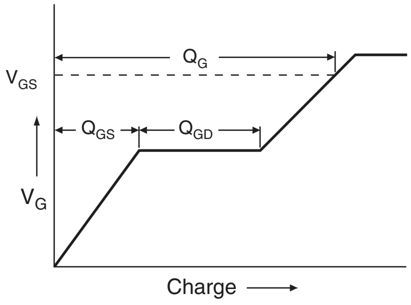


Fig. 13a - Basic Gate Charge Waveform

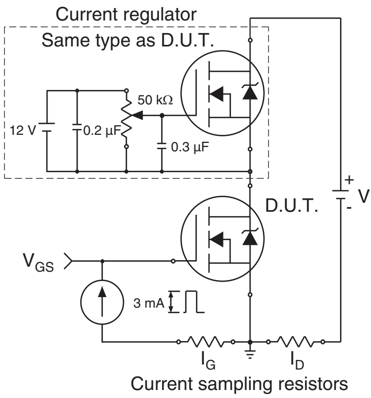
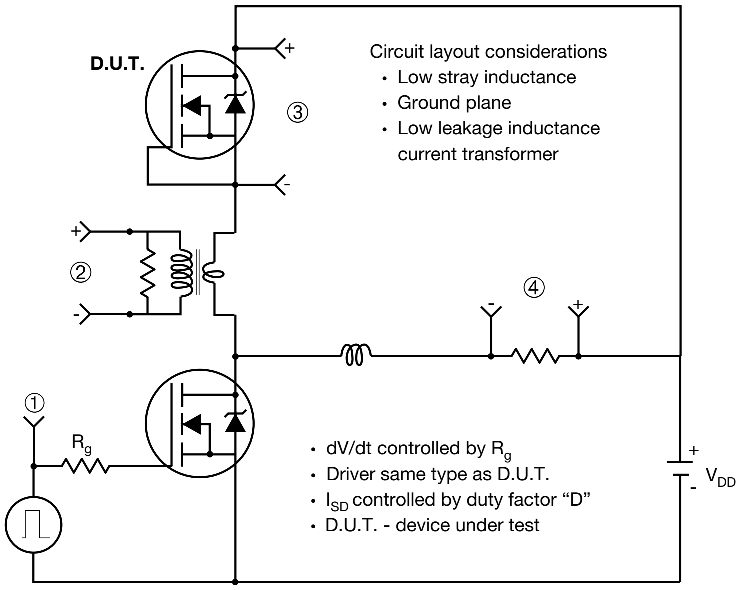


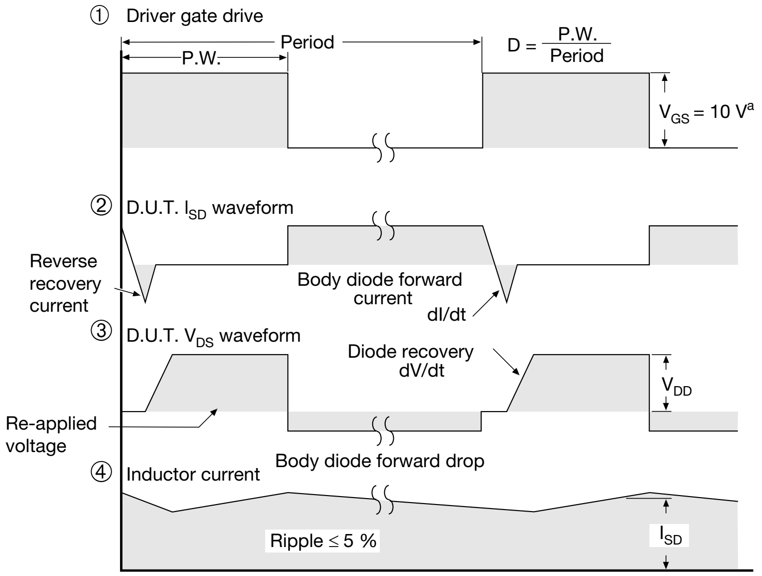
Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Circuit layout considerations
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

- dV/dt controlled by R_g
- Driver same type as D.U.T.
- I_{SD} controlled by duty factor “D”
- D.U.T. - device under test



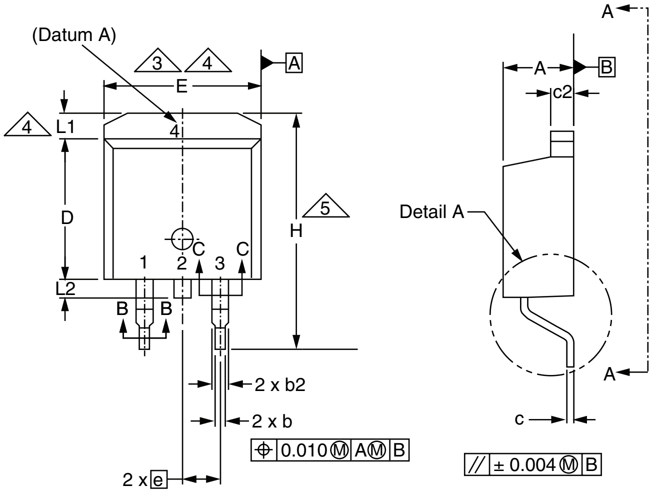
Note

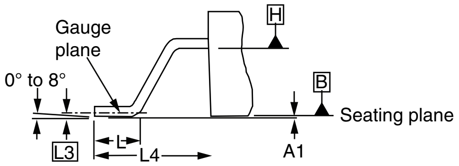
a. $V_{GS} = 5\ V$ for logic level devices

Fig. 14 - For N-Channel

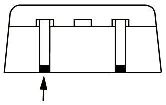
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?90414.

TO-263AB (HIGH VOLTAGE)

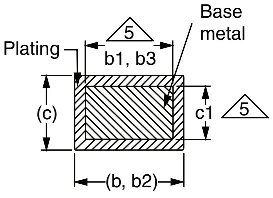




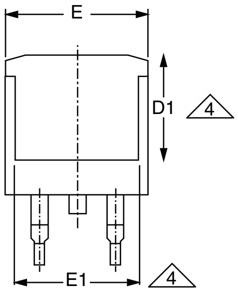
Detail "A"
Rotated 90° CW
scale 8:1



Lead tip



Section B - B and C - C
Scale: none



View A - A

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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