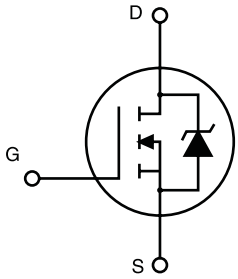
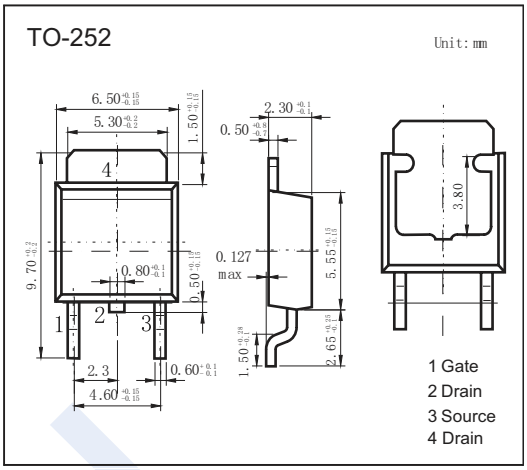
N-Channel MOSFET

IRLR3410

■ Features

- V_{DS} = 100V; I_D = 17A
- $R_{DS(ON)} \leqslant 0.105\Omega$ (V_{GS} = 10V)
- Logic Level Gate Drive
- Ultra Low On-Resistance
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated





■ Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±16	
Continuous Drain Current, V_{GS} @ 10V	Tc=25℃	I_D	17	A
	Tc=100℃		12	
Pulsed Drain Current ①⑤		I_{DM}	60	
Power Dissipation	Tc=25℃	P_D	79	W
Linear Derating Factor			0.53	W/℃
Single Pulse Avalanche Energy ②⑤		E_{AS}	150	mJ
Avalanche Current ①⑤		I_{AR}	9	A
Repetitive Avalanche Energy ①⑤		E_{AR}	7.9	mJ
Peak Diode Recovery dv/dt ③		dv/dt	5	V/ns
Thermal Resistance.Junction- to-Case		R_{thJC}	1.9	℃/W
Thermal Resistance.Junction- to-Ambient (PCB mount) ⑦		R_{thJA}	50	
Thermal Resistance.Junction- to-Ambient		R_{thJA}	110	
Soldering Temperature, for 10 seconds			300(1.6mm from case)	℃
Junction Temperature		T_J	175	
Storage Temperature Range		T_{stg}	-55 to 175	

N-Channel MOSFET

IRLR3410

■ Electrical Characteristics Ta = 25℃ (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25℃, I_D=1mA		0.122		V/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V			25	μA
		V_{DS}=80V, V_{GS}=0V, T_J=150℃			250	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±16V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A ④			0.105	Ω
		V_{GS}=5V, I_D=10A ④			0.125	
		V_{GS}=4V, I_D=9A ④			0.155	
Forward Transconductance	g_{FS}	V_{DS}=25V, I_D=9A ⑤	7.7			S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz, See Fig. 5 ⑤		800		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			90		
Internal Drain Inductance	L_D	Between lead, 6mm (0.25in.) from package and center or die contact		4.5		nH
Internal Source Inductance	L_S			7.5		
Total Gate Charge	Q_g	V_{GS}=5V, V_{DS}=80V, I_D=9A, See Fig. 6 and 13 ④⑤			34	nC
Gate Source Charge	Q_{gs}				4.8	
Gate Drain Charge	Q_{gd}				20	
Turn-On DelayTime	$t_{d(on)}$	V_{DD}=50V, I_D=9A, R_G=6Ω, V_{GS}=5V, R_D=5.5Ω, See Fig. 10 ④⑤		7.2		ns
Turn-On Rise Time	t_r			53		
Turn-Off DelayTime	$t_{d(off)}$			30		
Turn-Off Fall Time	t_f			26		
Body Diode Reverse Recovery Time	t_{rr}	T_J=25℃, I_F= 9A, di/dt= 100A/μs ④⑤			210	
Body Diode Reverse Recovery Charge	Q_{rr}				1100	nC
Body-Diode Continuous Source Current	I_S				17	A
Body-Diode Pulsed Source Current ①⑤	I_{SM}				60	
Diode Forward Voltage	V_{SD}	I_S=9A,V_{GS}=0V ④			1.3	V
Body Diode Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD}=25V, starting T_J=25°C, L=3.1mH, R_G=25Ω, I_{AS}=9A. (See Figure 12)

③ I_{SD}≤ 9.0A, di/dt ≤540A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤175°C

④ Pulse width ≤ 300μs; duty cycle≤ 2%

⑤ Uses IRL530N data and test conditions

⑥ When mounted on 1" square PCB (FR-4 or G-10 Material).

■ Marking

Marking	IRLR3410

N-Channel MOSFET

IRLR3410

■ Typical Characterisitics

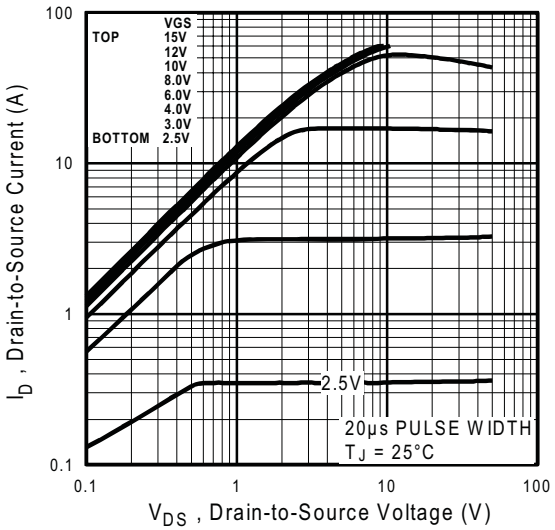


Fig 1. Typical Output Characteristics

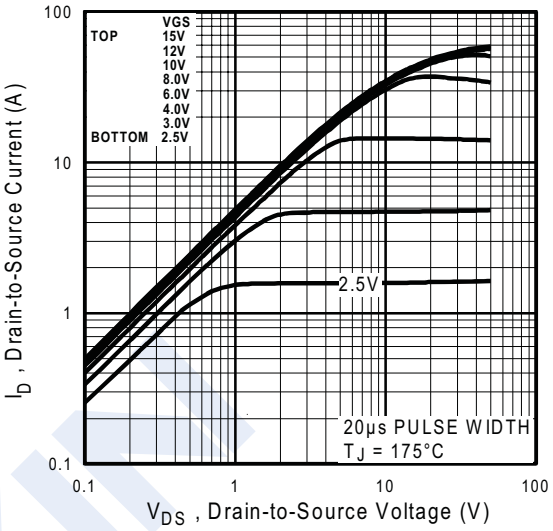


Fig 2. Typical Output Characteristics

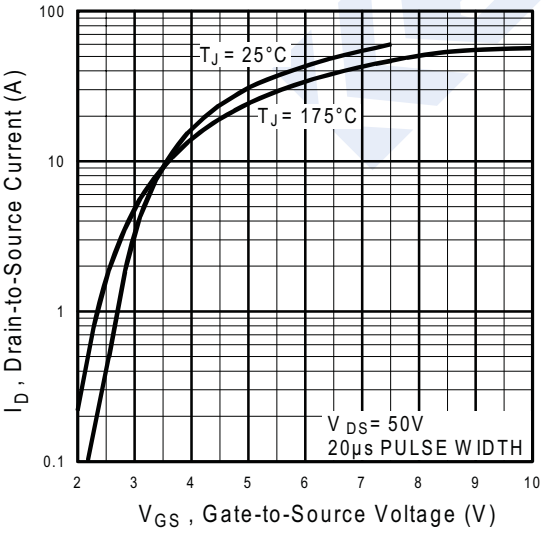


Fig 3. Typical Transfer Characteristics

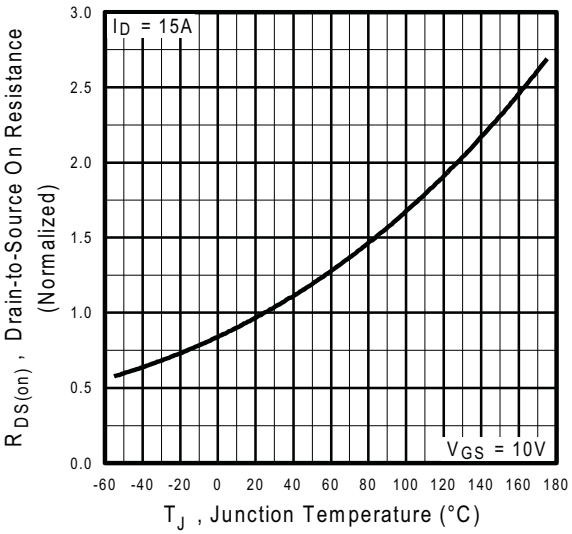


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel MOSFET

IRLR3410

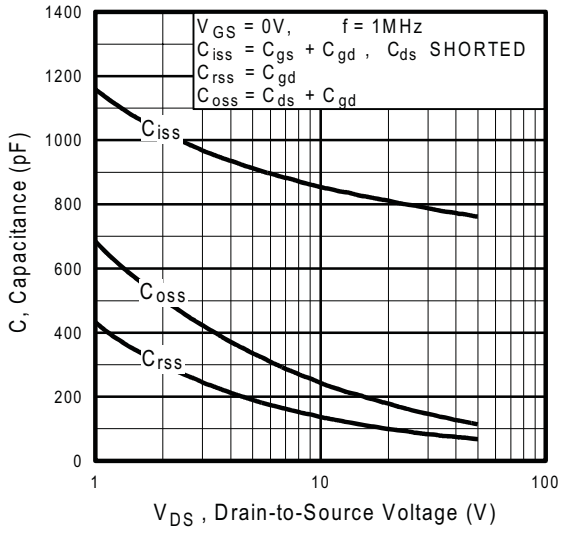


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

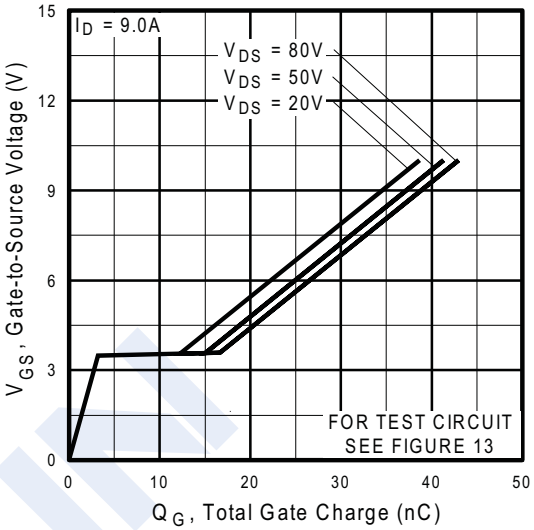


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

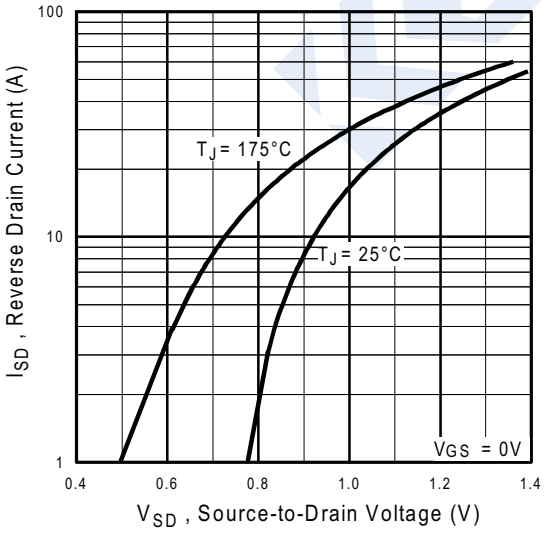


Fig 7. Typical Source-Drain Diode Forward Voltage

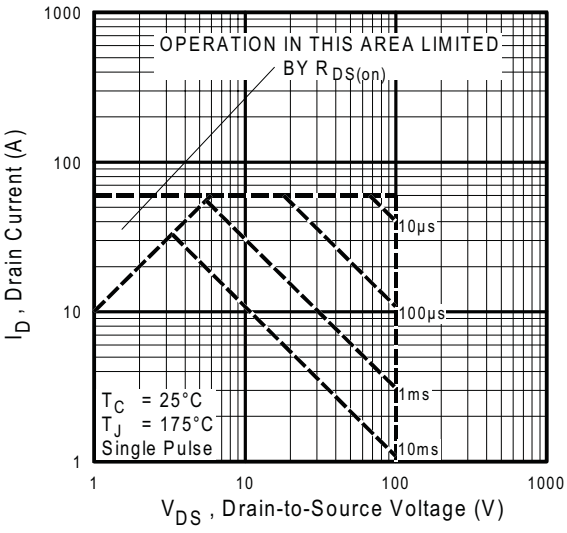


Fig 8. Maximum Safe Operating Area

N-Channel MOSFET

IRLR3410

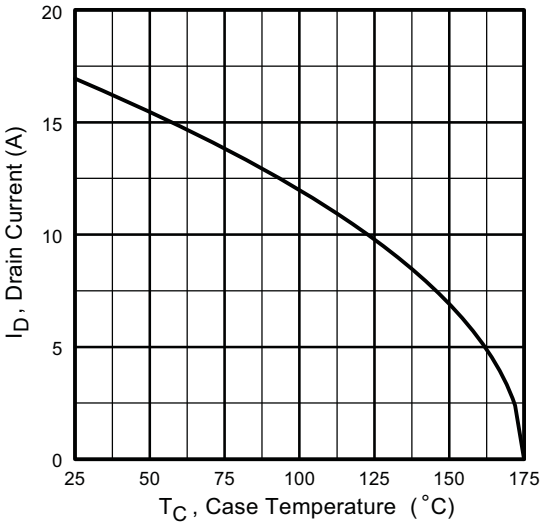


Fig 9. Maximum Drain Current Vs. Case Temperature

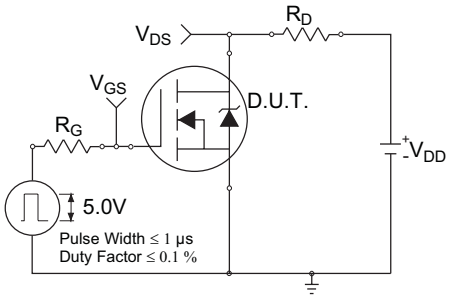


Fig 10a. Switching Time Test Circuit

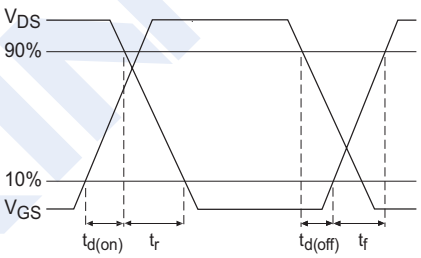


Fig 10b. Switching Time Waveforms

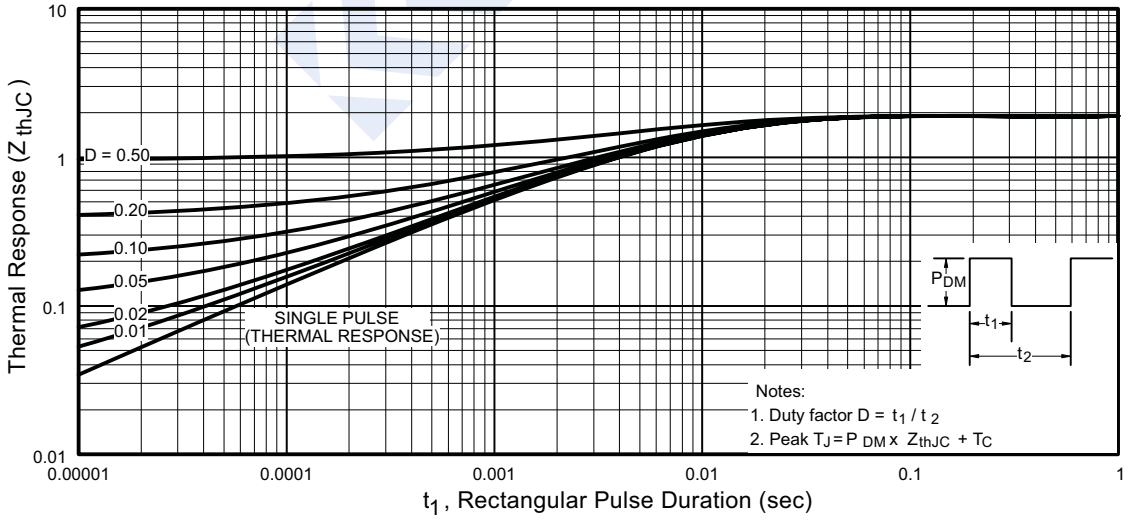


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

N-Channel MOSFET

IRLR3410

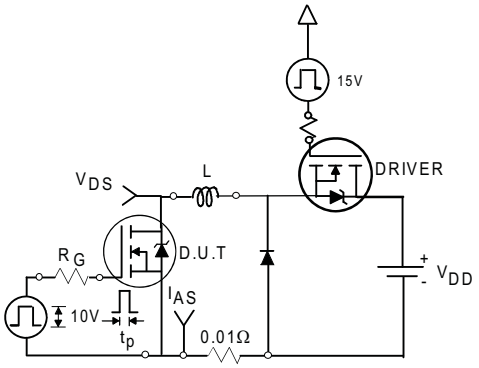


Fig 12a. Unclamped Inductive Test Circuit

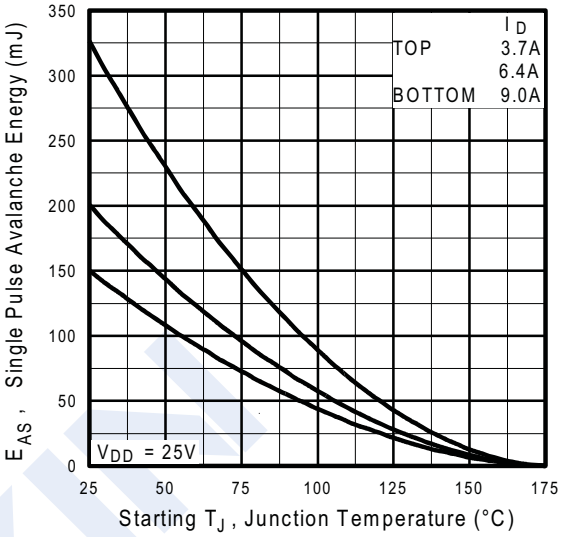


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

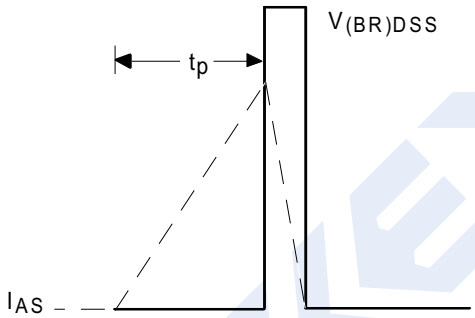


Fig 12b. Unclamped Inductive Waveforms

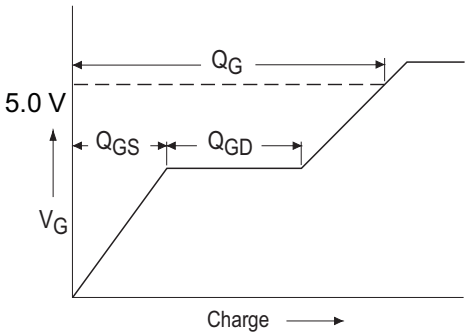


Fig 13a. Basic Gate Charge Waveform

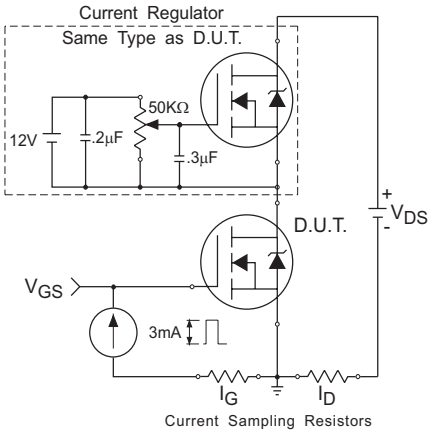
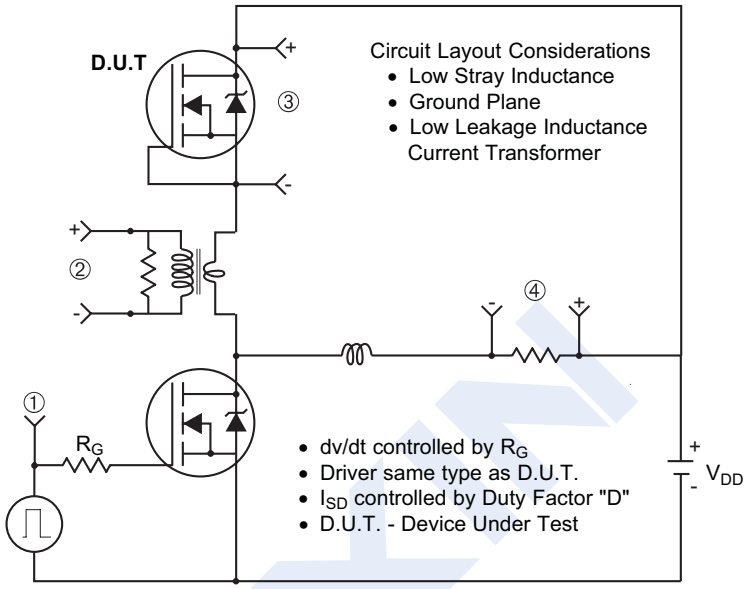


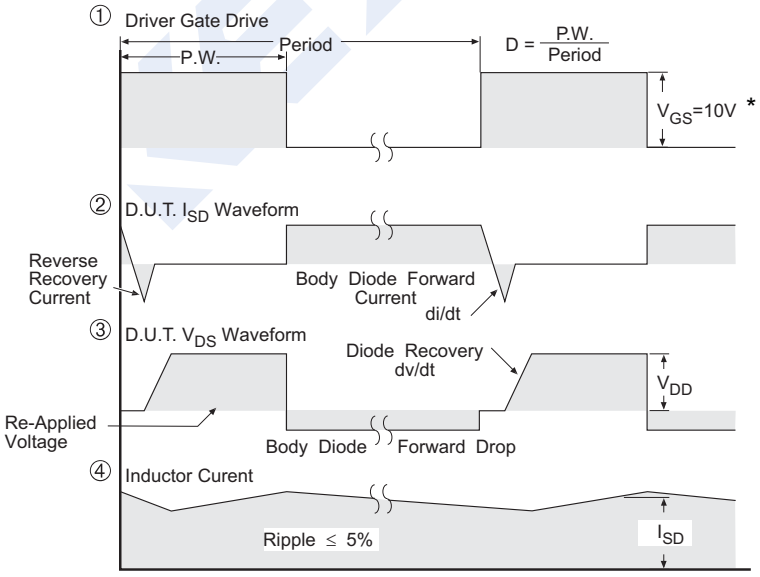
Fig 13b. Gate Charge Test Circuit

N-Channel MOSFET

IRLR3410

■ Peak Diode Recovery dv/dt Test Circuit





* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS