

FEATURES

- ◆ Avalanche Rugged Technology
- ◆ Rugged Gate Oxide Technology
- ◆ Lower Input Capacitance
- ◆ Improved Gate Charge
- ◆ Extended Safe Operating Area
- ◆ Lower Leakage Current: 10 μ A (Max.) @ $V_{DS} = 100V$
- ◆ Lower $R_{DS(on)}$: 0.101 Ω (Typ.)

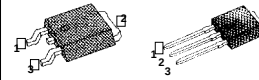
$$BV_{DSS} = 100 V$$

$$R_{DS(on)} = 0.12\Omega$$

$$I_D = 13 A$$

D-PAK

I-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	13	A
	Continuous Drain Current ($T_C=100^\circ C$)	8	
I_{DM}	Drain Current-Pulsed (1)	45	A
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (2)	225	mJ
I_{AR}	Avalanche Current (1)	13	A
E_{AR}	Repetitive Avalanche Energy (1)	4.6	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	6.5	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.5	W
	Total Power Dissipation ($T_C=25^\circ C$)	46	W
	Linear Derating Factor	0.37	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.7	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount).

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Rev. B

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	100	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.1	--	V/°C	$I_D=250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	1.0	--	2.0	V	$V_{DS}=5V, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-100	nA	$V_{GS}=-20V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	$V_{DS}=100V$
		--	--	100	μA	$V_{DS}=80V, T_C=150^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.12	Ω	$V_{GS}=5V, I_D=6.5A$ (4)
g_{fs}	Forward Transconductance	--	10.1	--	S	$V_{DS}=40V, I_D=6.5A$ (4)
C_{iss}	Input Capacitance	--	580	755	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	140	175		
C_{rss}	Reverse Transfer Capacitance	--	60	75		
$t_{d(on)}$	Turn-On Delay Time	--	10	30	ns	$V_{DD}=50V, I_D=14A,$ $R_G=6\Omega$ See Fig 13 (4) (5)
t_r	Rise Time	--	11	30		
$t_{d(off)}$	Turn-Off Delay Time	--	29	70		
t_f	Fall Time	--	15	40		
Q_g	Total Gate Charge	--	16.9	24	nC	$V_{DS}=80V, V_{GS}=5V,$ $I_D=14A$ See Fig 6 & Fig 12 (4) (5)
Q_{gs}	Gate-Source Charge	--	2.7	--		
Q_{gd}	Gate-Drain (. Miller.) Charge	--	9.7	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	13	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current (1)	--	--	45		
V_{SD}	Diode Forward Voltage (4)	--	--	1.5	V	$T_J=25^\circ\text{C}, I_S=13A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	109	--	ns	$T_J=25^\circ\text{C}, I_F=14A$
Q_{rr}	Reverse Recovery Charge	--	0.41	--	μC	$di_F/dt=100A/\mu s$ (4)

Notes;

- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2) $L=2\text{mH}$, $I_{AS}=13A$, $V_{DD}=25V$, $R_G=27\Omega$, Starting $T_J=25^\circ\text{C}$
- (3) $I_{SD} \leq 14A$, $di/dt \leq 350A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
- (4) Pulse Test: Pulse Width = 250 μs , Duty Cycle $\leq 2\%$
- (5) Essentially Independent of Operating Temperature

N-CHANNEL POWER MOSFET

IRLR/U130A

Fig 1. Output Characteristics

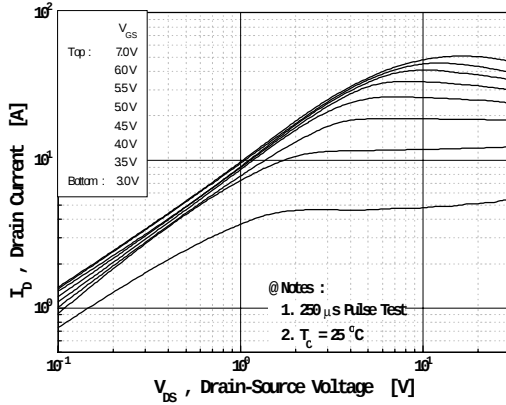


Fig 2. Transfer Characteristics

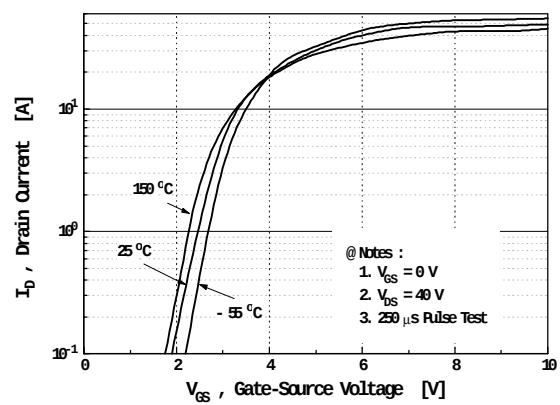


Fig 3. On-Resistance vs. Drain Current

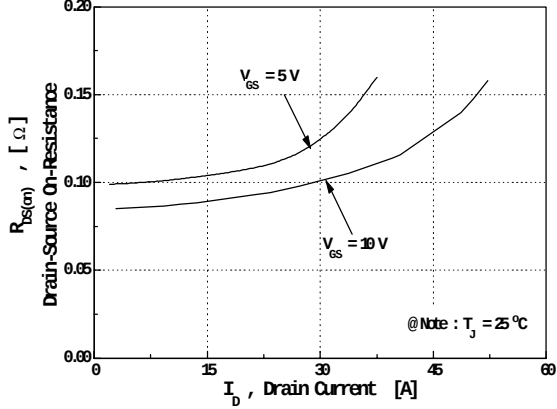


Fig 4. Source-Drain Diode Forward Voltage

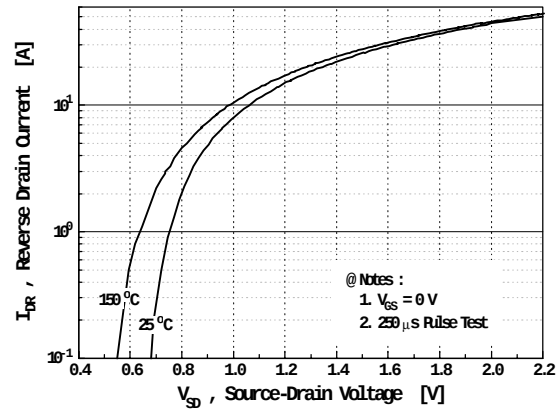


Fig 5. Capacitance vs. Drain-Source Voltage

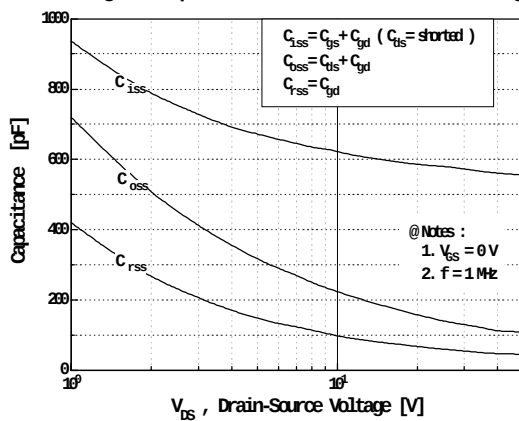


Fig 6. Gate Charge vs. Gate-Source Voltage

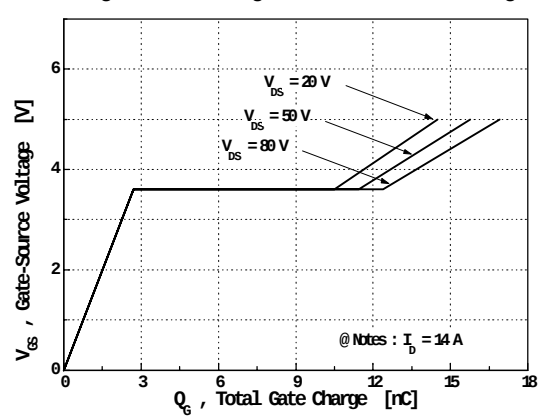


Fig 7. Breakdown Voltage vs. Temperature

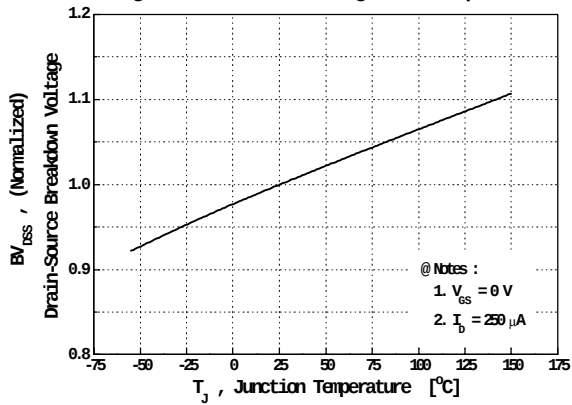


Fig 8. On-Resistance vs. Temperature

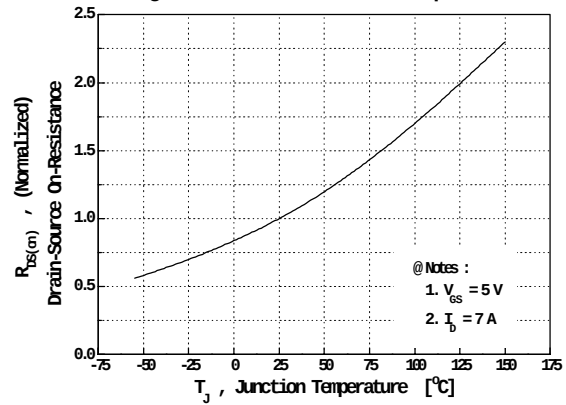


Fig 9. Max. Safe Operating Area

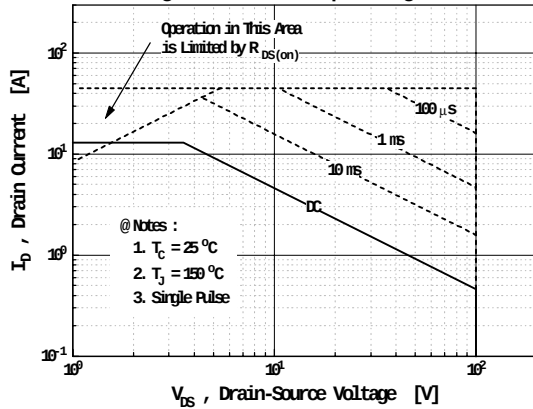


Fig 10. Max. Drain Current vs. Case Temperature

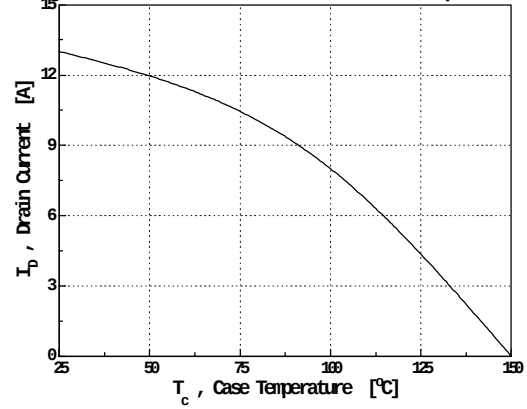
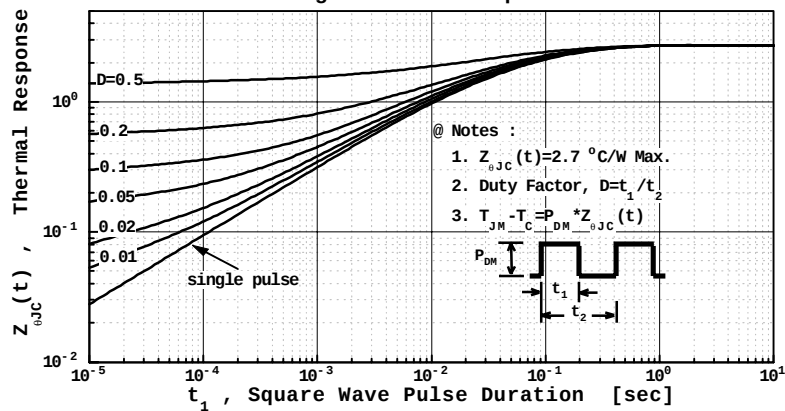
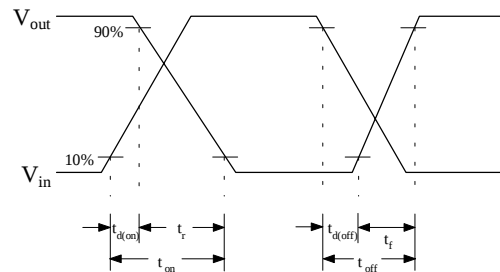
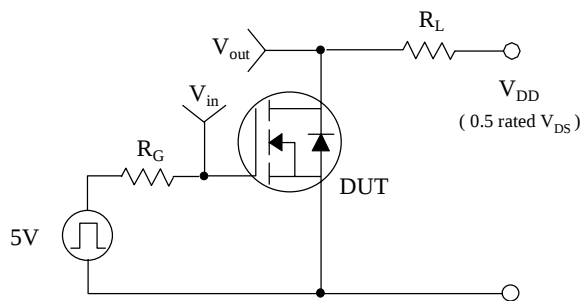


Fig 11. Thermal Response



The diagram shows a current regulator circuit. A 12V DC source is connected to a network of components: a 200nF capacitor, a 50kΩ resistor, and a 300nF capacitor. A MOSFET, labeled "Same Type as DUT", has its gate connected to the node between the 50kΩ resistor and the 300nF capacitor. The drain of this MOSFET is connected to the drain of the DUT MOSFET. The source of the DUT MOSFET is connected to a node between two resistors, R_1 and R_2 . The gate of the DUT MOSFET is connected to a terminal labeled V_{GS} . The source of the DUT MOSFET is also connected to a terminal labeled "Current Sampling (I_G) Resistor". The drain of the DUT MOSFET is connected to a terminal labeled "Current Sampling (I_D) Resistor". A 3mA current source is shown injecting current into the I_G terminal. The circuit is powered by a V_{DS} source connected to the drain of the DUT MOSFET and the I_D terminal.



Vary t_p to obtain required peak I_D

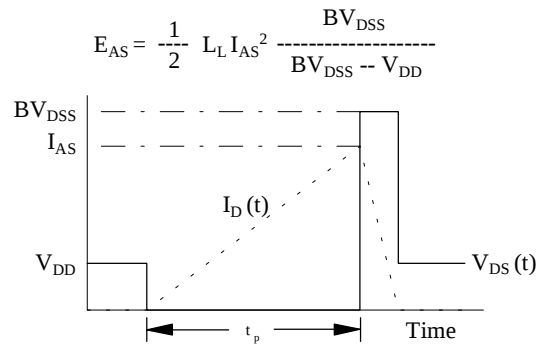
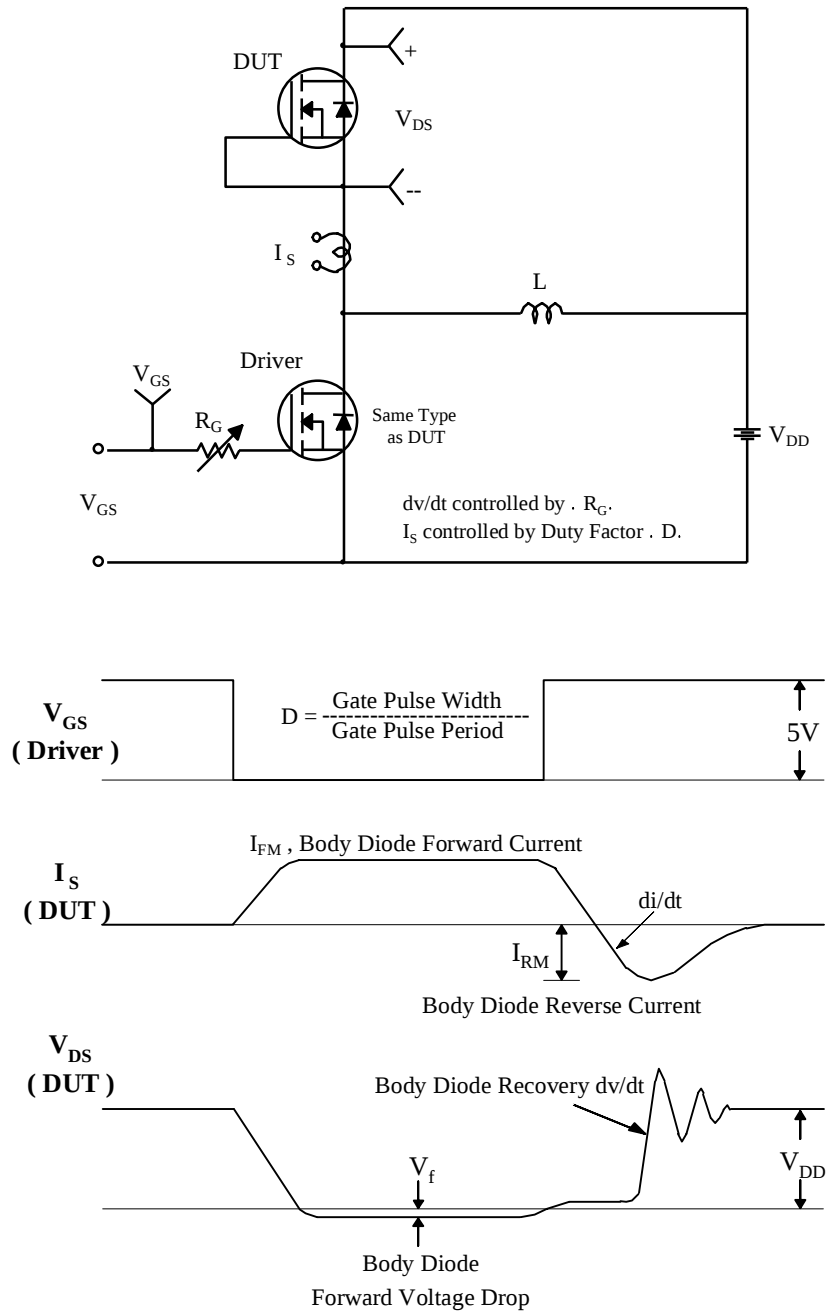


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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Technical drawing of a 2-pin connector showing dimensions in millimeters (mm). The drawing includes a front view, a side view, and a detail view of the pin.

Front View Dimensions:

- Overall width: 6.60 ± 0.20
- Pin spacing: 5.34 ± 0.30
- Pin width: 0.70 ± 0.20
- Pin height: 0.80 ± 0.20
- Pin diameter: $\phi 0.76 \pm 0.10$
- Pin length: 2.30 TYP [2.30 ± 0.20]
- Pin thickness: 0.60 ± 0.20
- Pin height (from base): 2.70 ± 0.20
- Pin height (from base): 6.10 ± 0.20
- Pin height (from base): 9.50 ± 0.30

Side View Dimensions:

- Overall height: 2.30 ± 0.10
- Pin height: 0.50 ± 0.10
- Pin diameter: $\phi 0.55$
- Pin length: 0.89 ± 0.10
- Pin height (from base): 0.91 ± 0.10
- Pin height (from base): 1.02 ± 0.20
- Pin height (from base): 1.02 ± 0.20
- Pin height (from base): 2.30 ± 0.20

Detail View Dimensions:

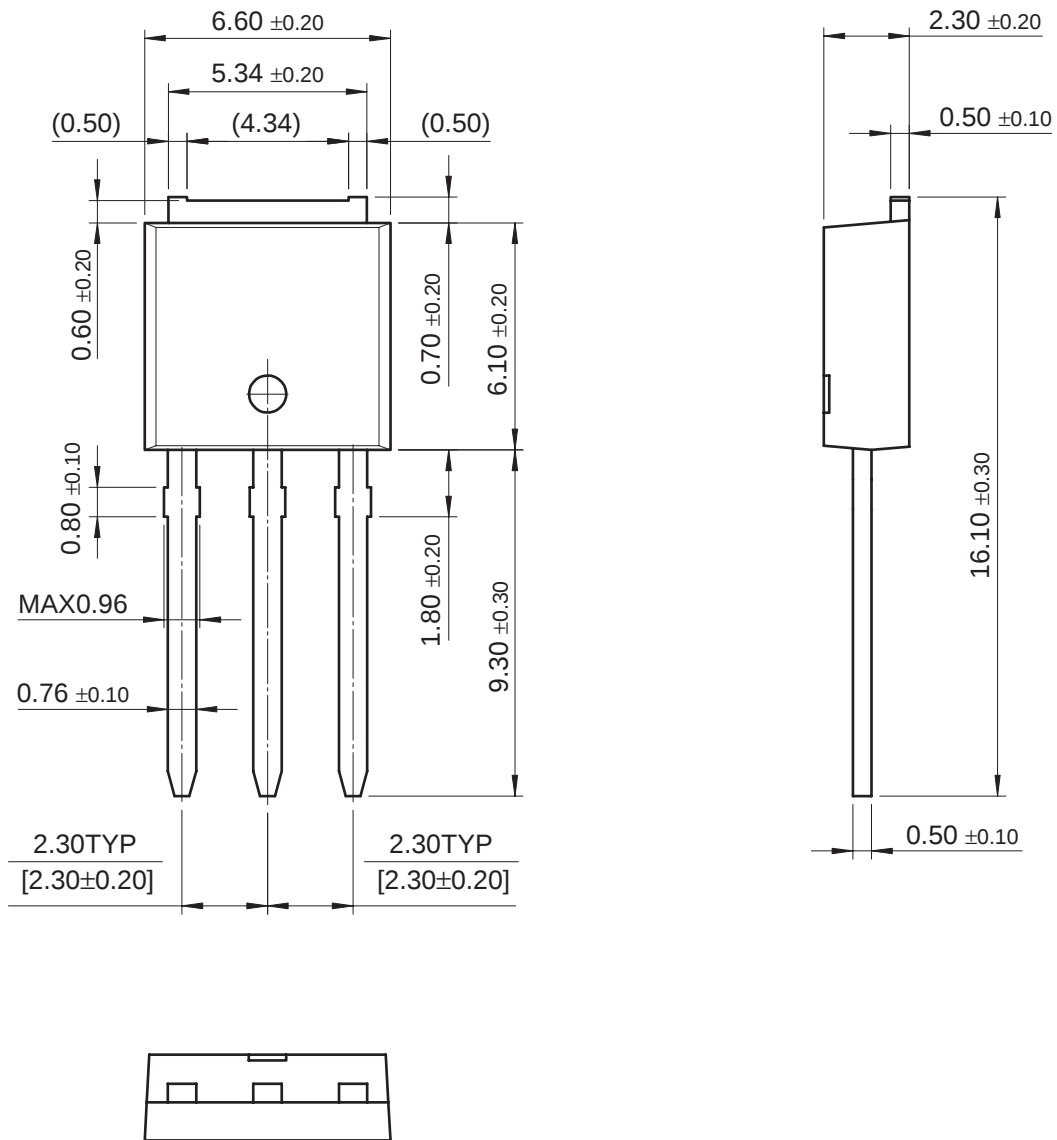
- Overall width: 6.60 ± 0.20
- Pin spacing: 5.34
- Pin width: 0.70
- Pin height: 0.90
- Pin length: 1.00
- Pin diameter: $\phi 0.76 \pm 0.10$
- Pin height (from base): 2.70 ± 0.20
- Pin height (from base): 6.10 ± 0.20
- Pin height (from base): 9.50 ± 0.30
- Pin thickness: 0.60 ± 0.20
- Pin height (from base): 2.70 ± 0.20
- Pin height (from base): 6.10 ± 0.20
- Pin height (from base): 9.50 ± 0.30

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IPAK Package Dimensions



IPAK (FS PKG CODE AL)



Dimensions in Millimeters

September 1999, Rev B

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