

IRL640SPbF

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS}=4V$ & $5V$
- Fast Switching
- Lead-Free

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

Absolute Maximum Ratings

Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 5.0 V	17
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 5.0 V	11
I_{DM}	Pulsed Drain Current ①	68
P_D @ $T_C = 25^\circ C$	Power Dissipation	125
P_D @ $T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	3.1
	Linear Derating Factor	1.0
	Linear Derating Factor (PCB Mount)**	0.025
V_{GS}	Gate-to-Source Voltage	± 10
E_{AS}	Single Pulse Avalanche Energy ②	580
I_{AR}	Avalanche Current ①	10
E_{AR}	Repetitive Avalanche Energy ①	13
dv/dt	Peak Diode Recovery dv/dt ③	5.0
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D=1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18 0.27	Ω	$V_{GS}=5.0V$, $I_D=10A$ ④ $V_{GS}=4.0V$, $I_D=8.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
g_{fs}	Forward Transconductance	16	—	—	S	$V_{DS}=50V$, $I_D=10A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25 250	μA	$V_{DS}=200V$, $V_{GS}=0V$ $V_{DS}=160V$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS}=-10V$
Q_g	Total Gate Charge	—	—	66	nC	$I_D=17A$
Q_{gs}	Gate-to-Source Charge	—	—	9.0	nC	$V_{DS}=160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	38	nC	$V_{GS}=5.0V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—	ns	$V_{DD}=100V$
t_r	Rise Time	—	83	—	ns	$I_D=17A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—	ns	$R_G=4.6\Omega$
t_f	Fall Time	—	52	—	ns	$R_D=5.7\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—	nH	
C_{iss}	Input Capacitance	—	1800	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	400	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	120	—	pF	$f=1.0MHz$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	68	A	
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}$, $I_S=17A$, $V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	310	470	ns	$T_J=25^\circ\text{C}$, $I_F=17A$
Q_{rr}	Reverse Recovery Charge	—	3.2	4.8	μC	$di/dt=100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

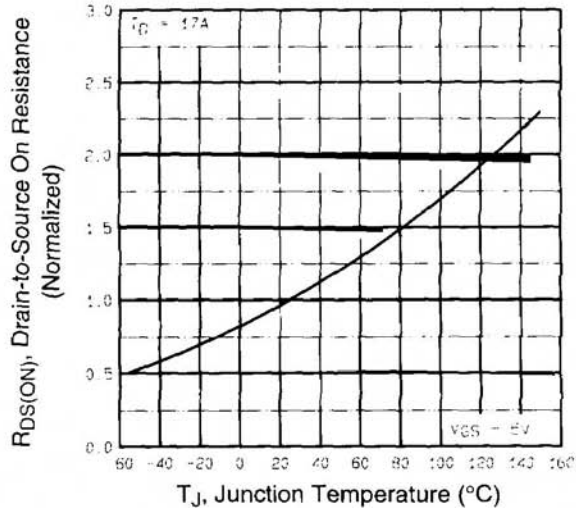
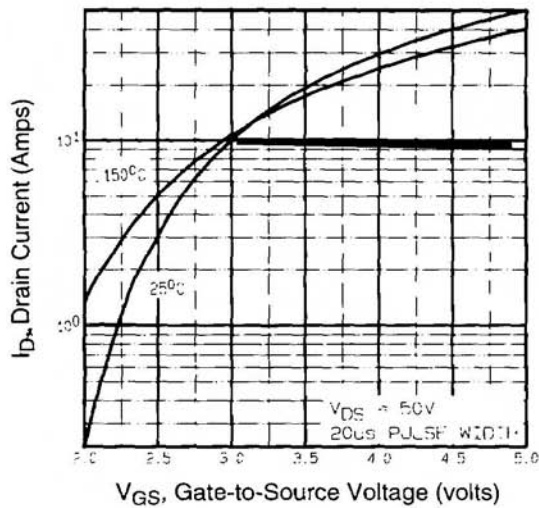
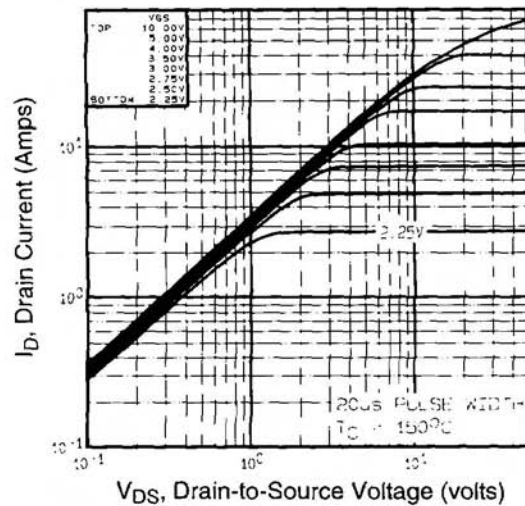
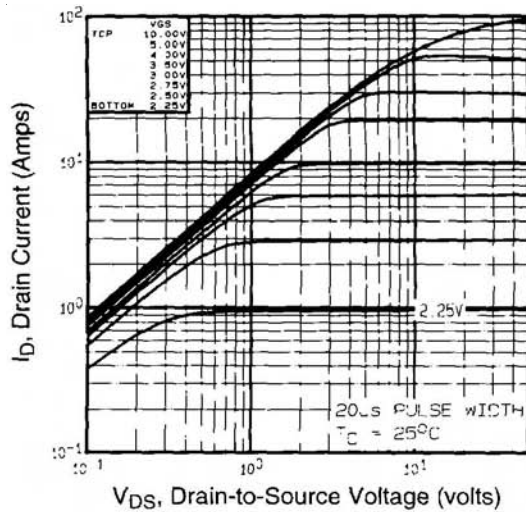
Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

③ $I_{SD} \leq 17A$, $di/dt \leq 150A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

② $V_{DD}=50V$, starting $T_J=25^\circ\text{C}$, $L=3.0mH$, $R_G=25\Omega$, $I_{AS}=17A$ (See Figure 12)

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



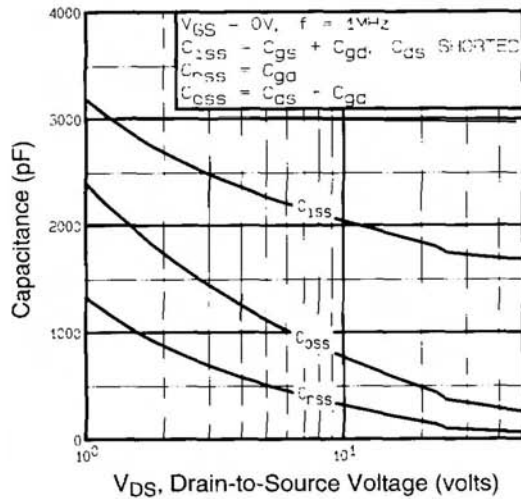


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

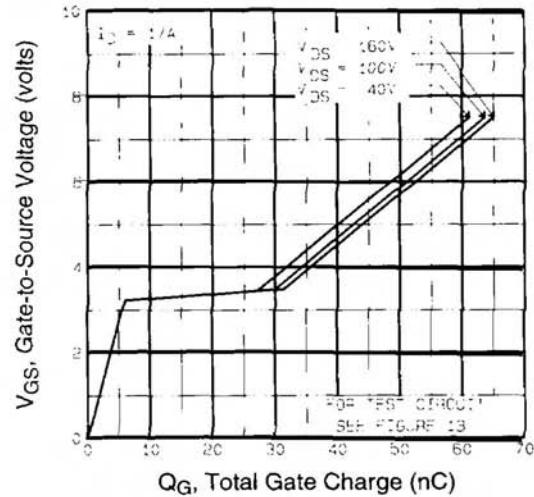


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

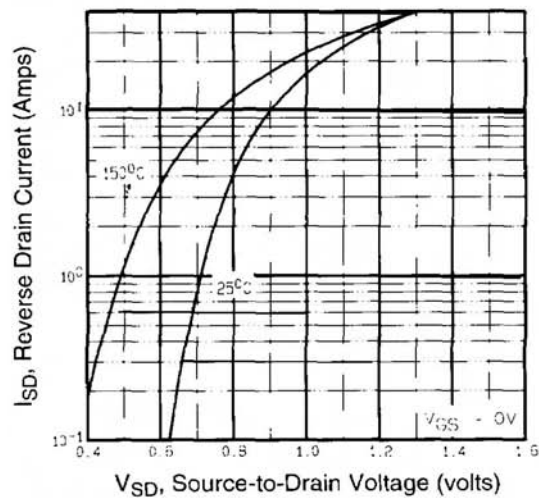


Fig 7. Typical Source-Drain Diode Forward Voltage

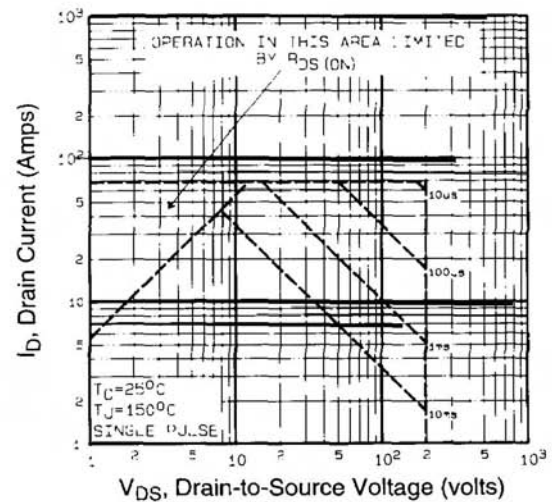


Fig 8. Maximum Safe Operating Area

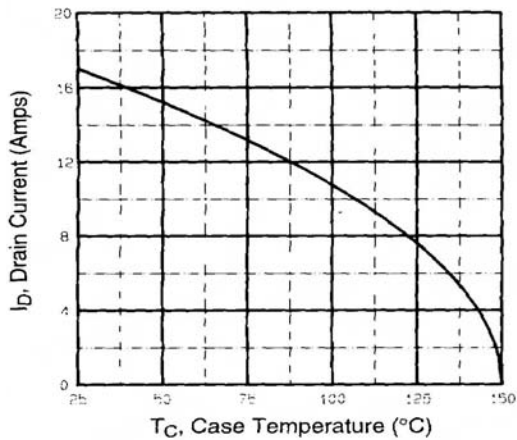


Fig 9. Maximum Drain Current Vs. Case Temperature

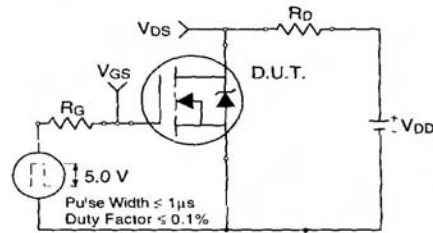


Fig 10a. Switching Time Test Circuit

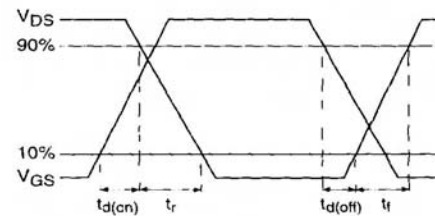


Fig 10b. Switching Time Waveforms

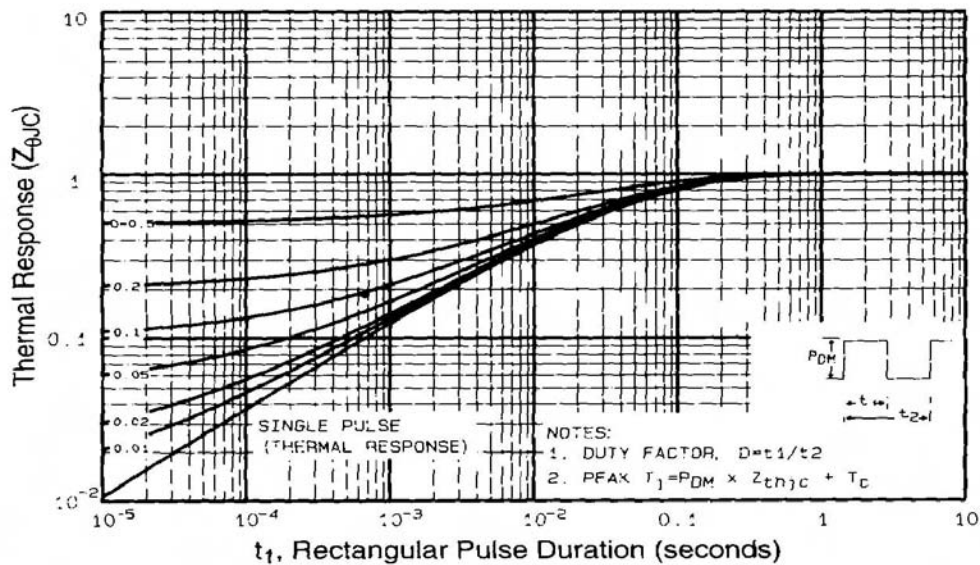


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

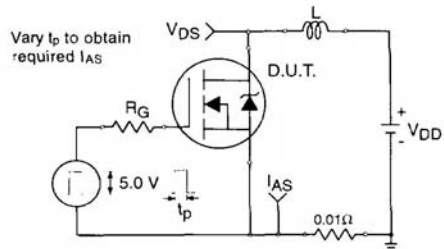


Fig 12a. Unclamped Inductive Test Circuit

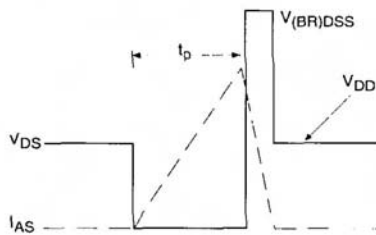


Fig 12b. Unclamped Inductive Waveforms

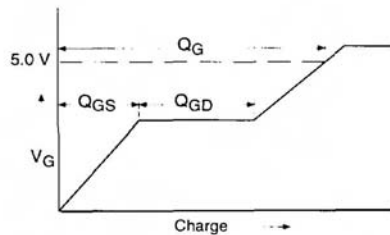


Fig 13a. Basic Gate Charge Waveform

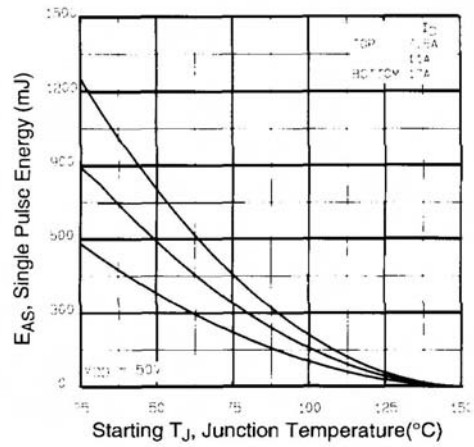


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

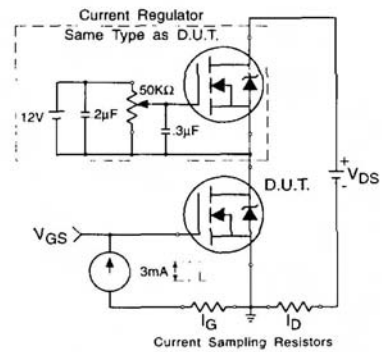
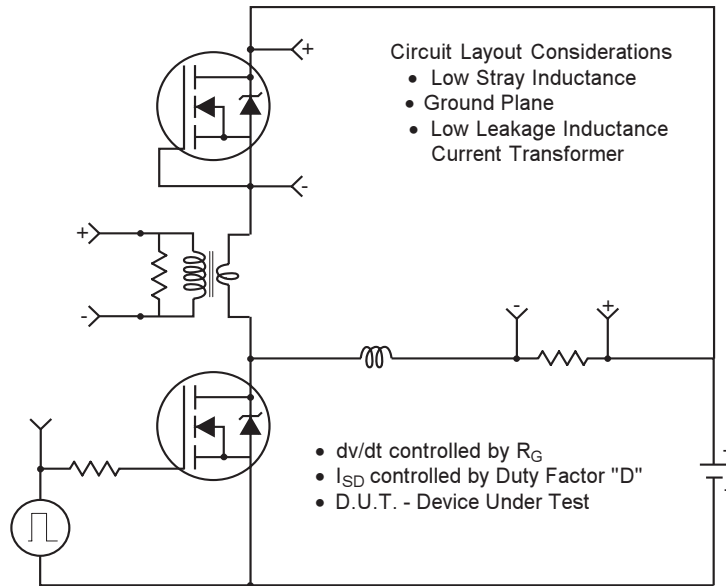


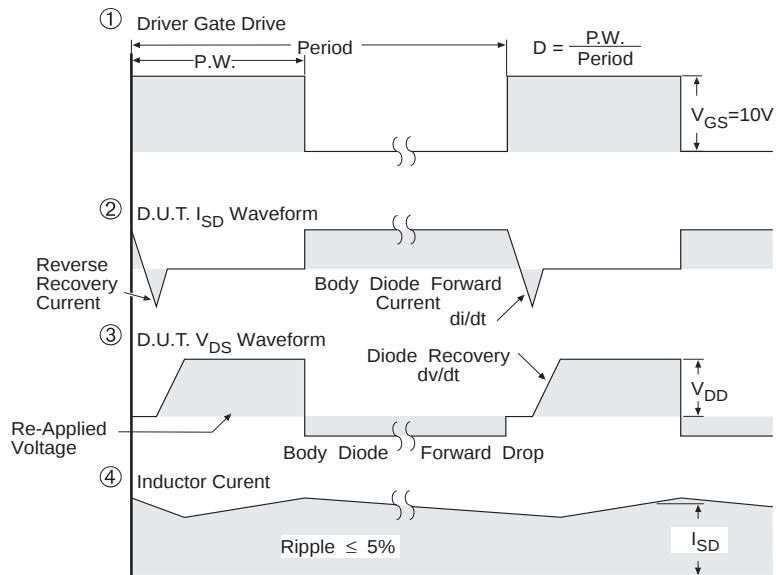
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14 For N Channel HEXFETS

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Dimensions are shown in millimeters (inches)



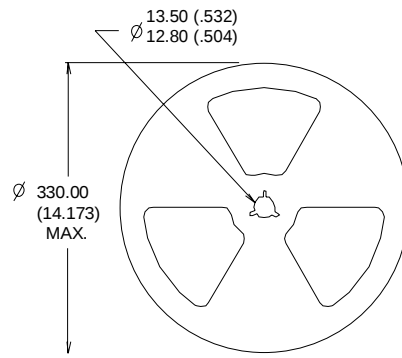
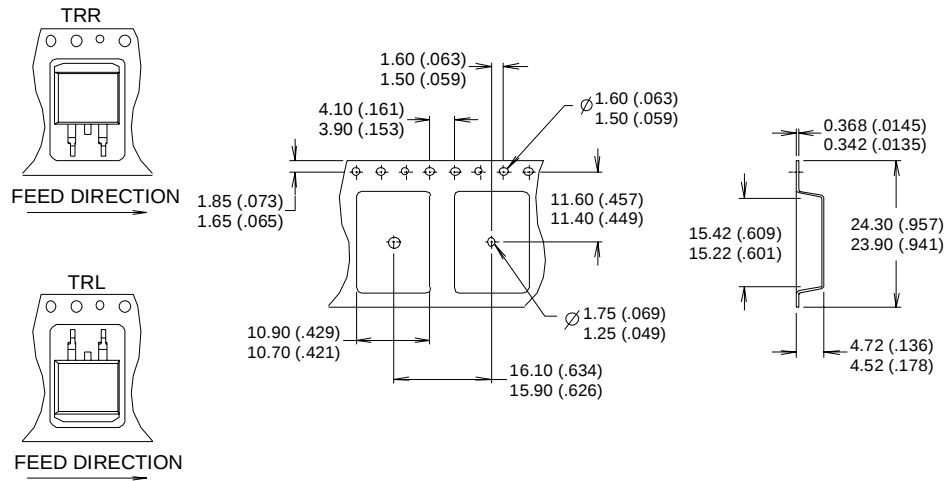
• PART DEPENDENT.

5. CONTROLLING DIMENSION: INCH.

DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A = ASSEMBLY SITE CODE

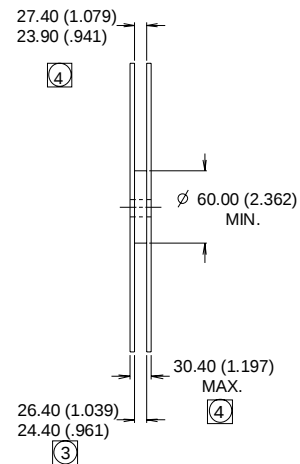
D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Data and specifications subject to change without notice.