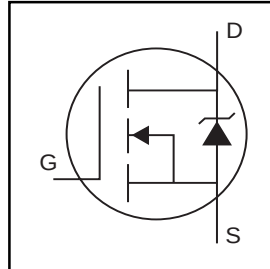


- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching

Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters in the PC environment. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

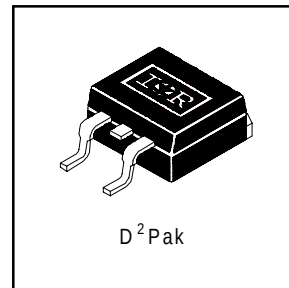
The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



$$V_{DS} = 20V$$

$$R_{DS(on)} = 0.016W$$

$$I_D = 48A$$

D²Pak

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ ⑤	48	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ ⑤	30	
I_{DM}	Pulsed Drain Current ①⑤	190	
$P_D @ T_C = 25^\circ C$	Power Dissipation	69	W
	Linear Derating Factor	0.56	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
V_{GSM}	Gate-to-Source Voltage (Start Up Transient, $t_p = 100\mu s$)	14	V
E_{AS}	Single Pulse Avalanche Energy②⑤	270	mJ
I_{AR}	Avalanche Current①	29	A
E_{AR}	Repetitive Avalanche Energy①	6.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{JC}	Junction-to-Case	—	1.8	°C/W
R_{JA}	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$DV_{(BR)DSS}/DT_J$	Breakdown Voltage Temp. Coefficient	—	0.029	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.019	W	$V_{GS} = 4.5V, I_D = 29A$ ④
		—	—	0.016		$V_{GS} = 7.0V, I_D = 29A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	28	—	—	S	$V_{DS} = 16V, I_D = 29A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 10V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	43	nC	$I_D = 29A$
Q_{gs}	Gate-to-Source Charge	—	—	12		$V_{DS} = 16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	13		$V_{GS} = 4.5V$, See Fig. 6 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	9.8	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	100	—		$I_D = 29A$
$t_{d(off)}$	Turn-Off Delay Time	—	63	—		$R_G = 9.5W, V_{GS} = 4.5V$
t_f	Fall Time	—	82	—		$R_D = 0.3W$ ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	2000	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	800	—		$V_{DS} = 15V$
C_{rss}	Reverse Transfer Capacitance	—	290	—		$f = 1.0\text{MHz}$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	48	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	190		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 29A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	68	100	ns	$T_J = 25^\circ\text{C}, I_F = 29A$
Q_{rr}	Reverse Recovery Charge	—	130	190	nC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25^\circ\text{C}$, $L = 0.64\text{mH}$
 $R_G = 25W, I_{AS} = 29A$.

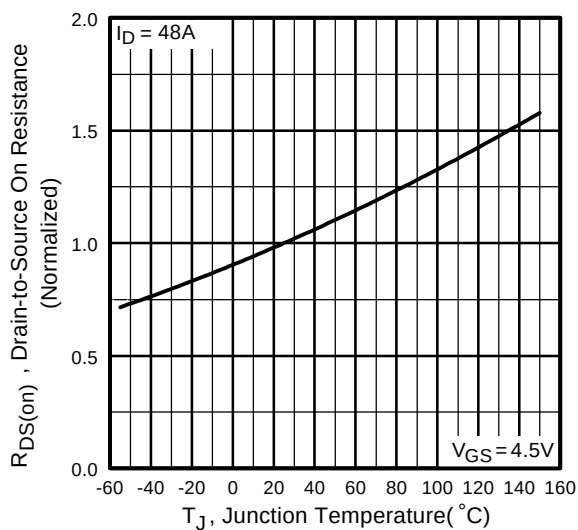
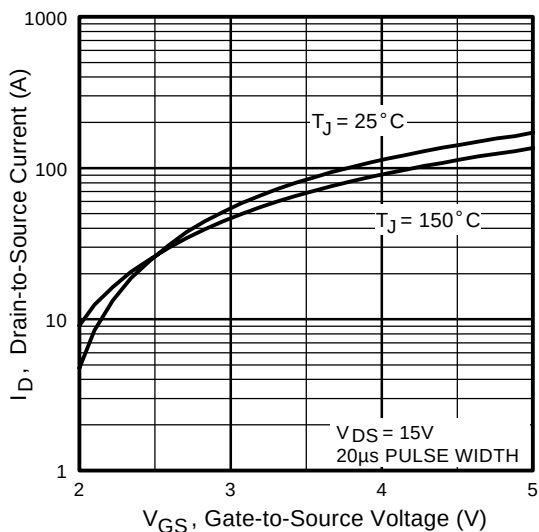
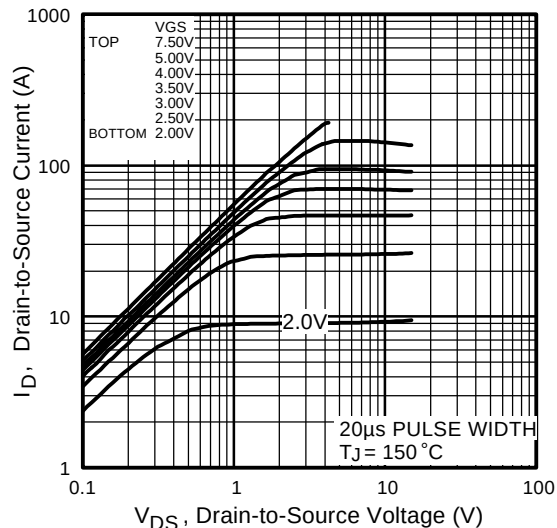
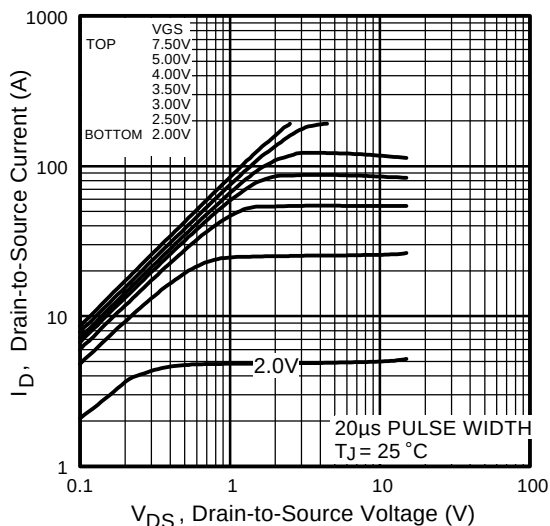
③ $I_D \leq 29A, di/dt \leq 63A/\mu s, V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ Uses IRL3202 data and test conditions

** When mounted on FR-4 board using minimum recommended footprint.

For recommended footprint and soldering techniques refer to application note #AN-994.



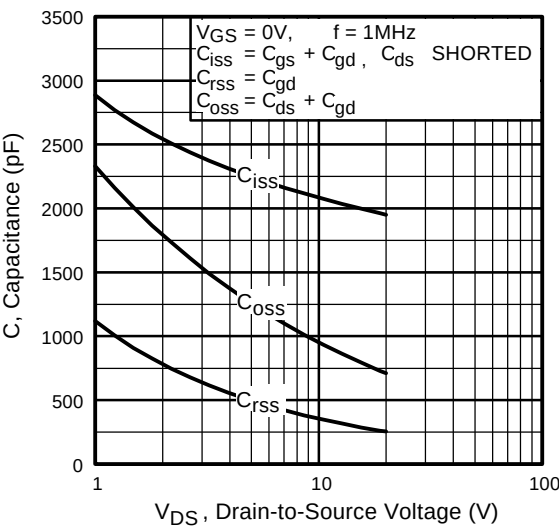


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

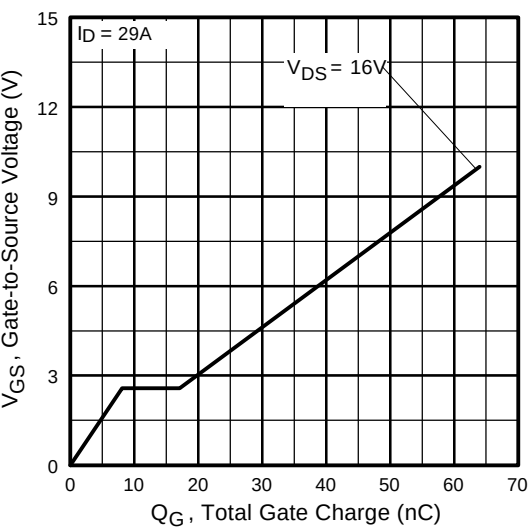


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

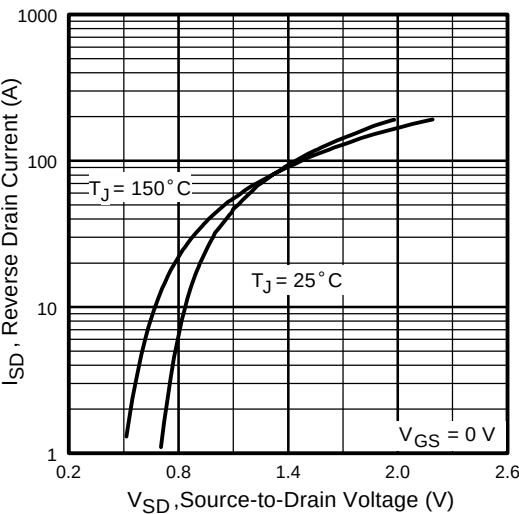


Fig 7. Typical Source-Drain Diode Forward Voltage

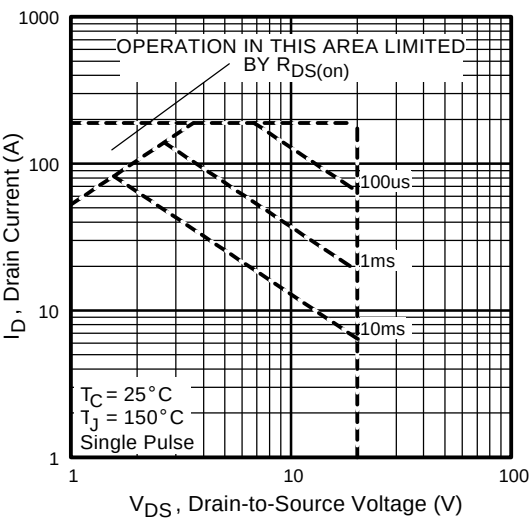


Fig 8. Maximum Safe Operating Area

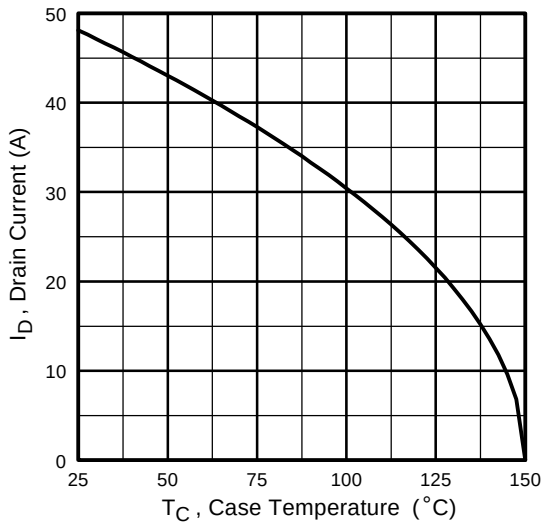


Fig 9. Maximum Drain Current Vs. Case Temperature

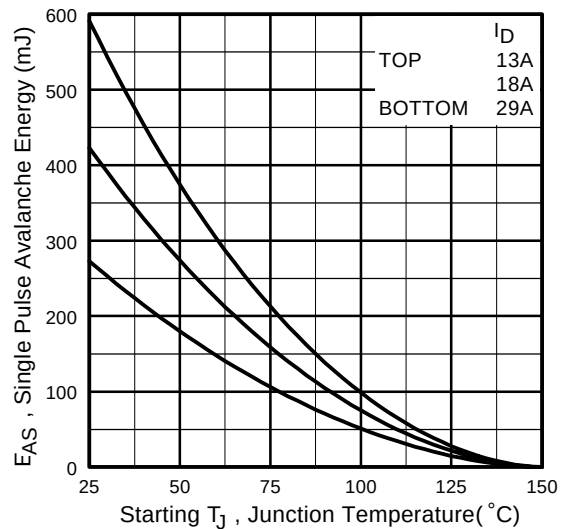


Fig 10. Maximum Avalanche Energy Vs. Drain Current

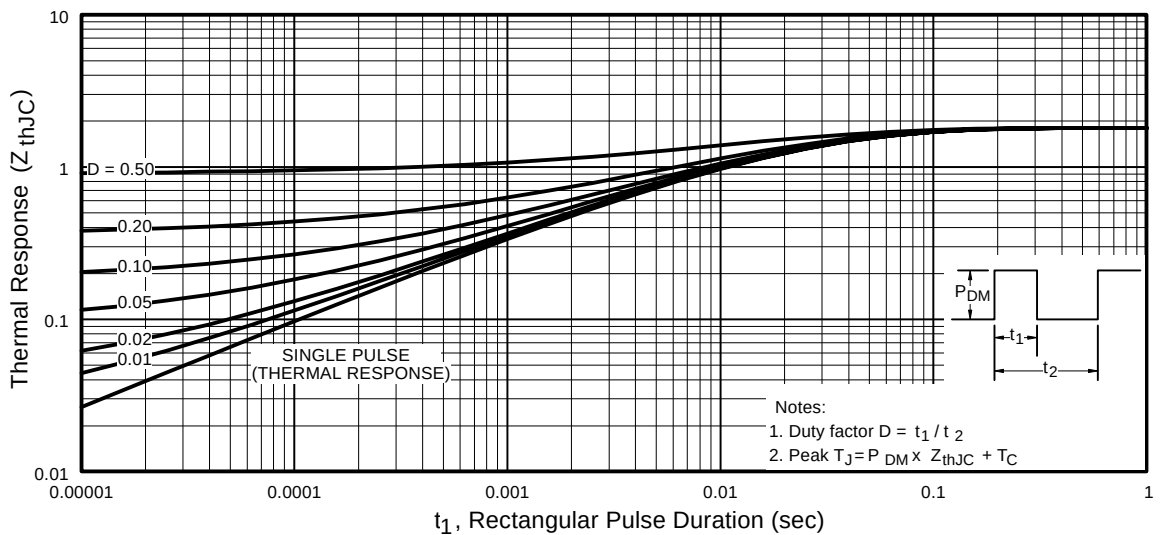


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

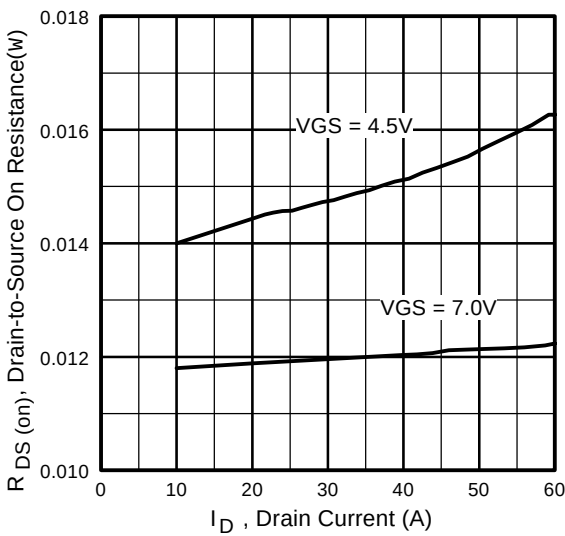


Fig 12. On-Resistance Vs. Drain Current

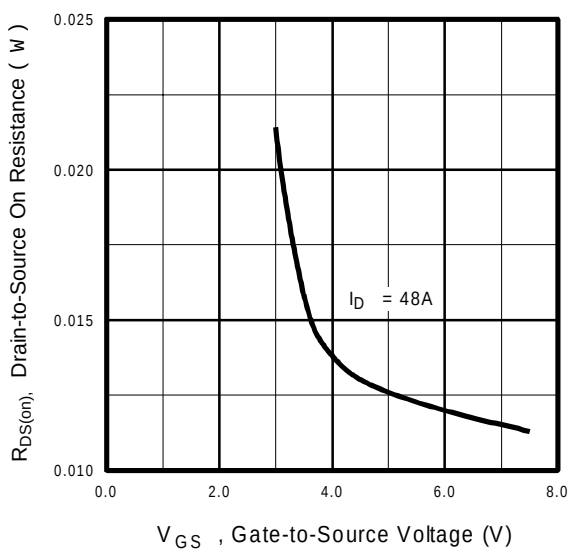
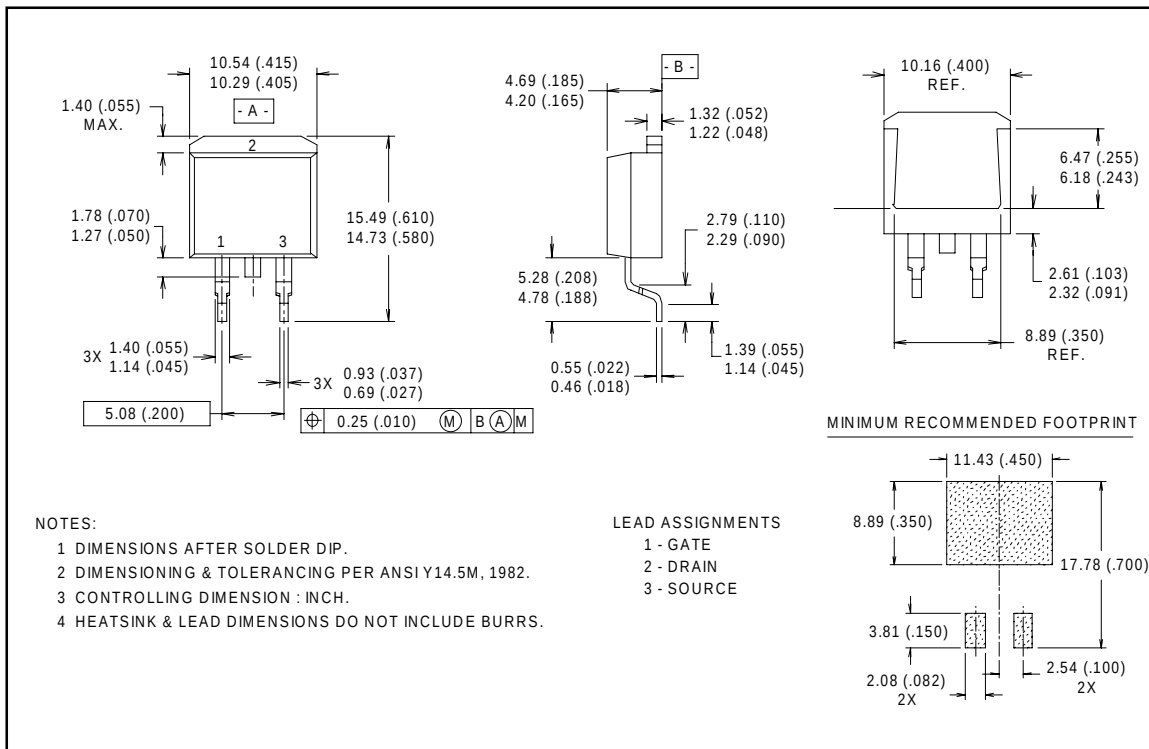


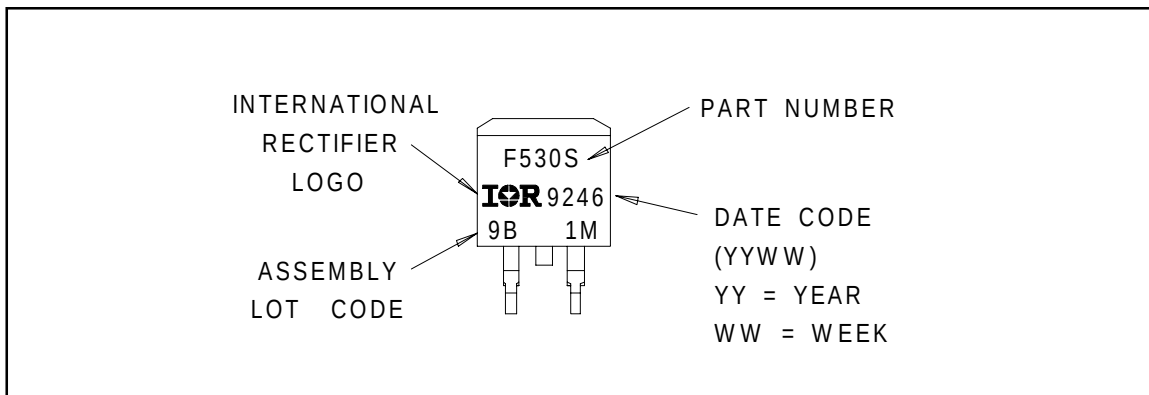
Fig 13. On-Resistance Vs. Gate Voltage

D²Pak Package Outline



Part Marking Information

D²Pak



Tape & Reel Information

D²Pak

