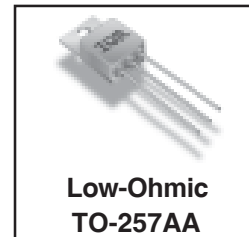


**RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
THRU-HOLE (Low-Ohmic TO-257AA)**

**2N7625T3
IRHLYS797034CM
60V, P-CHANNEL
R7™ TECHNOLOGY**

Product Summary

Part Number	Radiation Level	R _{DS(on)}	I _D
IRHLYS797034CM	100K Rads (Si)	0.074Ω	-20A*
IRHLYS793034CM	300K Rads (Si)	0.074Ω	-20A*



International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary N-Channel Available - IRHLYS77034CM

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I _D @V _{GS} = -4.5V, T _C = 25°C	Continuous Drain Current	-20*	A
I _D @V _{GS} = -4.5V, T _C = 100°C	Continuous Drain Current	-16.6	
I _{DM}	Pulsed Drain Current ①	-80	
P _D @ T _C = 25°C	Max. Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V _{GS}	Gate-to-Source Voltage	±10	V
E _{AS}	Single Pulse Avalanche Energy ②	181	mJ
I _{AR}	Avalanche Current ①	-20	A
E _{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	10.9	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063in/1.6mm from case for 10s)	
	Weight	4.3 (Typical)	g

* Current is limited by package

For footnotes refer to the last page

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Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.06	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.074	Ω	V _{GS} = -4.5V, I _D = -16.6A ^④
V _{GS(th)}	Gate Threshold Voltage	-1.0	—	-2.0	V	V _{DS} = V _{GS} , I _D = -250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	3.8	—	mV/°C	
g _{fs}	Forward Transconductance	17	—	—	S	V _{DS} = -10V, I _{DS} = -16.6A ^④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
		—	—	-10		V _{DS} = -48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 10V
Q _g	Total Gate Charge	—	—	36	nC	V _{GS} = -4.5V, I _D = -20A
Q _{gs}	Gate-to-Source Charge	—	—	14		V _{DS} = -30V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	18	ns	
t _{d(on)}	Turn-On Delay Time	—	—	32		V _{DD} = -30V, I _D = -20A, V _{GS} = -5.0V, R _G = 7.5Ω
t _r	Rise Time	—	—	265		
t _{d(off)}	Turn-Off Delay Time	—	—	100		
t _f	Fall Time	—	—	85		
LS + LD	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.025 in from package) to Source lead (6mm/ 0.025 in from package)
C _{iss}	Input Capacitance	—	2249	—	pF	V _{GS} = 0V, V _{DS} = -25V
C _{oss}	Output Capacitance	—	580	—		f = 1.0MHz
C _{rss}	Reverse Transfer Capacitance	—	86	—		
R _g	Gate Resistance	—	—	20	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-20*	A	
I _{SM}	Pulse Source Current (Body Diode) ^①	—	—	-80		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _j = 25°C, I _S = -20A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	—	100	ns	T _j = 25°C, I _F = -20A, di/dt ≤ -100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	128	nC	V _{DD} ≤ -25V ^④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

* Current is limited by package

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	1.67	°C/W	
R _{thJA}	Junction-to-Ambient	—	—	80		Typical Socket Mount

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

IRHLYS797034CM, 2N7625T3

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ $T_j = 25^\circ\text{C}$, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0		$V_{GS} = V_{DS}, I_D = -250\mu A$
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	$V_{GS} = -10V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	100		$V_{GS} = 10V$
I_{DSS}	Zero Gate Voltage Drain Current	—	-1.0	μA	$V_{DS} = -48V, V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.076	Ω	$V_{GS} = -4.5V, I_D = -16.6A$
$R_{DS(on)}$	Static Drain-to-Source On-state ④ Resistance (Low Ohmic TO-257)	—	0.074	Ω	$V_{GS} = -4.5V, I_D = -16.6A$
V_{SD}	Diode Forward Voltage④	—	-5.0	V	$V_{GS} = 0V, I_D = -20A$

1. Part numbers IRHLYS797034, IRHLYS793034

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@VGS=0V	@VGS=2V	@VGS=4V	@VGS=5V	@VGS=6V	@VGS=7V
$38 \pm 5\%$	$300 \pm 7.5\%$	$38 \pm 7.5\%$	-60	-60	-60	-60	-60	-40
$62 \pm 5\%$	$355 \pm 7.5\%$	$33 \pm 7.5\%$	-60	-60	-60	-60	-60	-
$85 \pm 5\%$	$380 \pm 7.5\%$	$29 \pm 7.5\%$	-60	-60	-60	-60	-	-

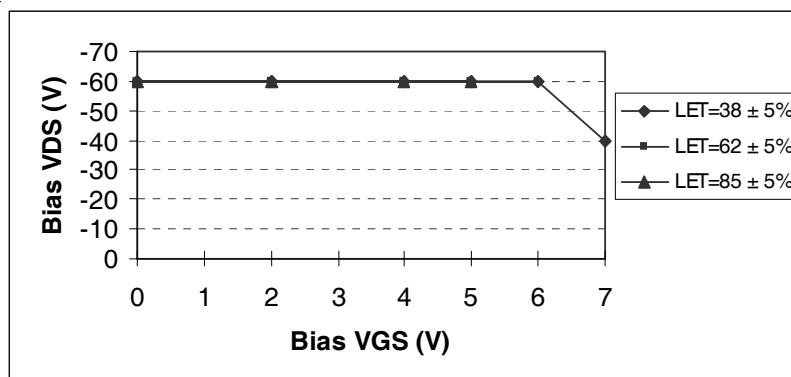
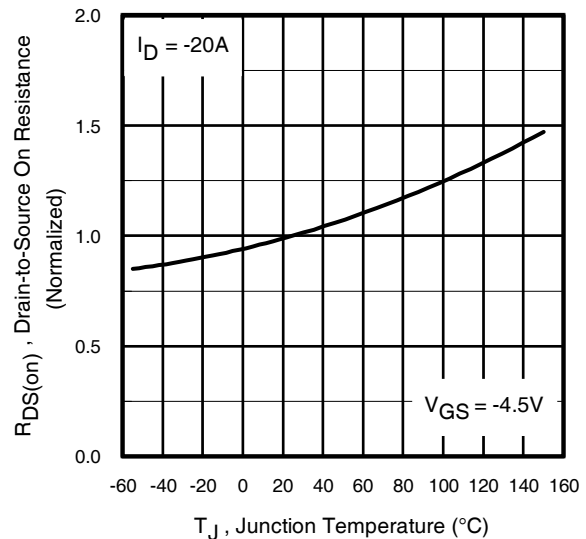
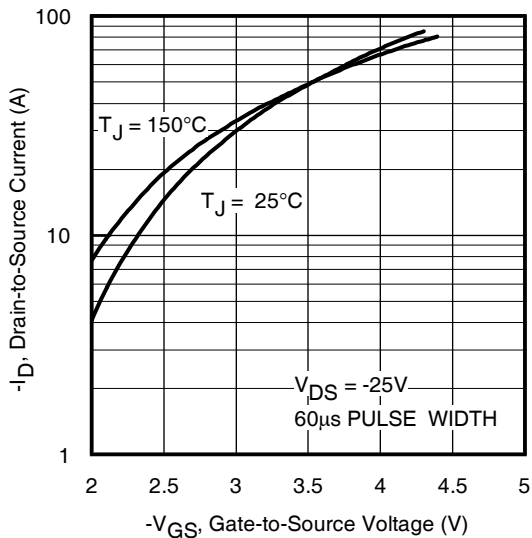
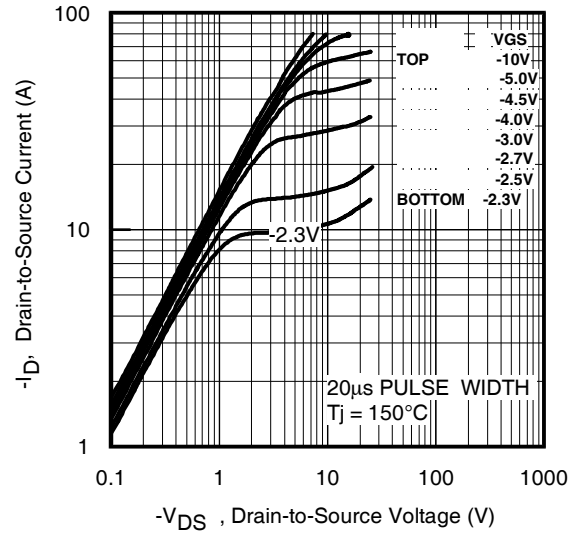
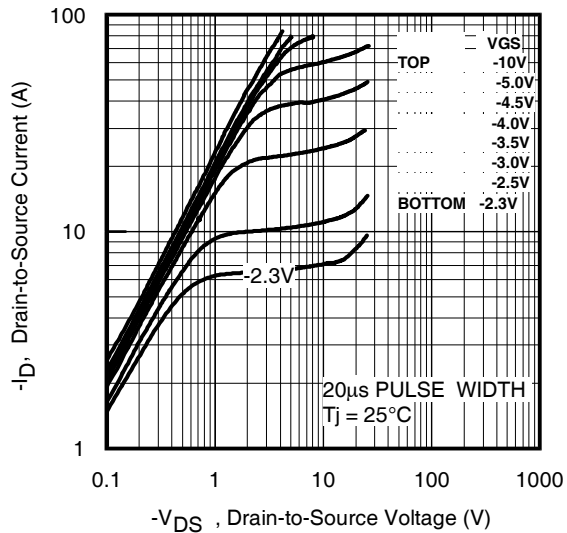


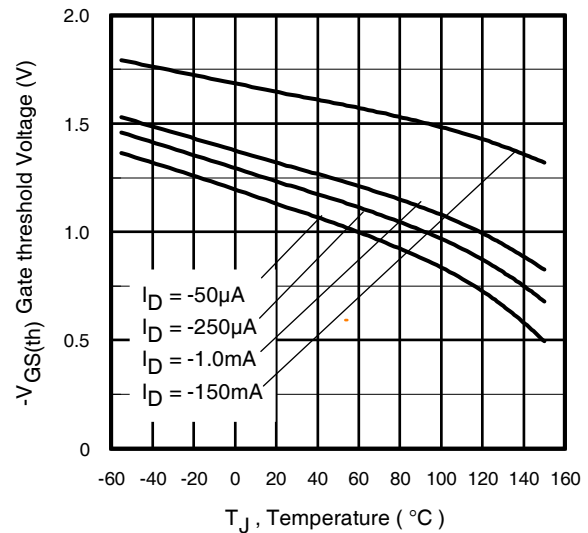
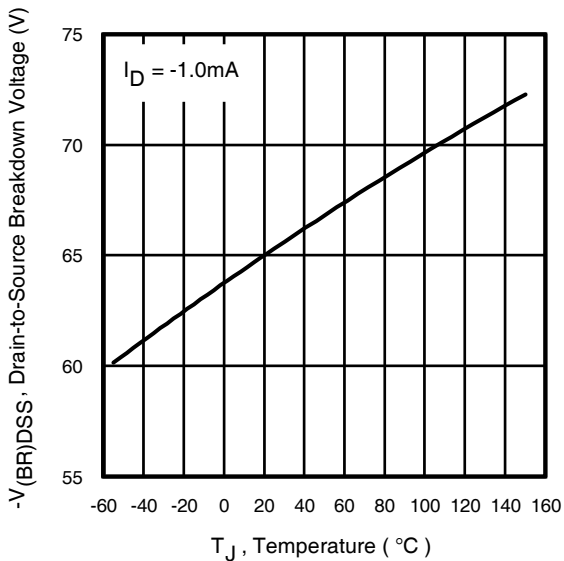
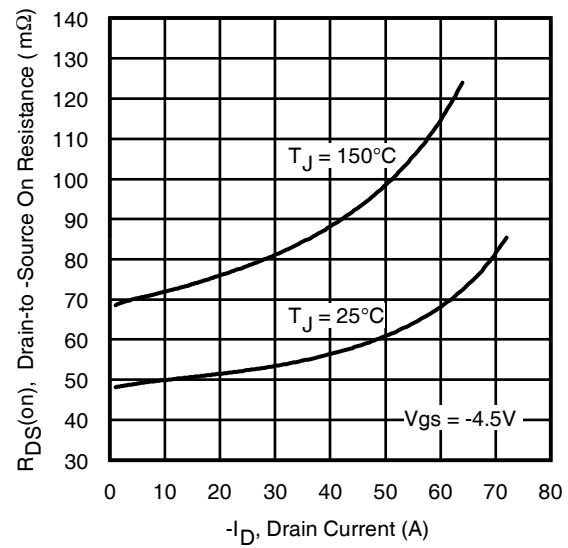
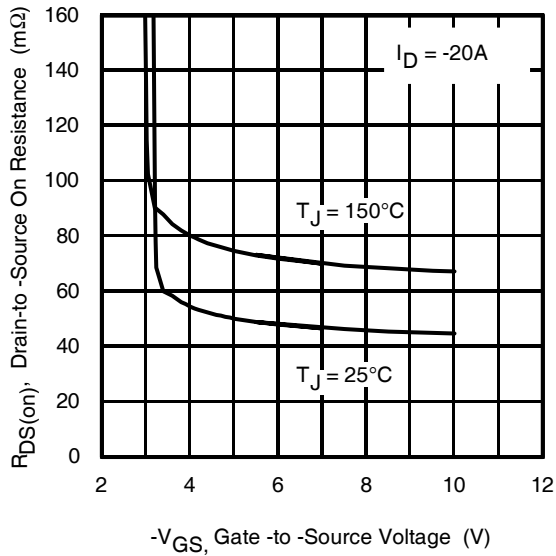
Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page



Pre-Irradiation

IRHLYS797034CM, 2N7625T3



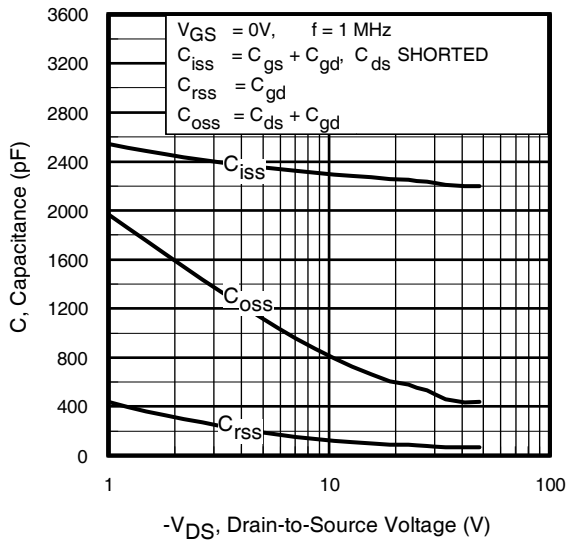


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

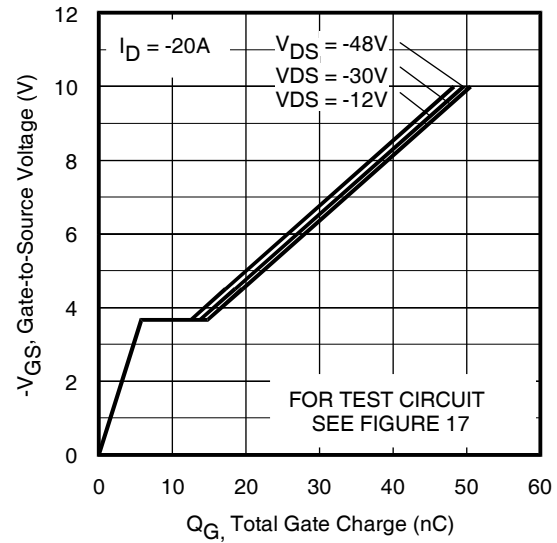


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

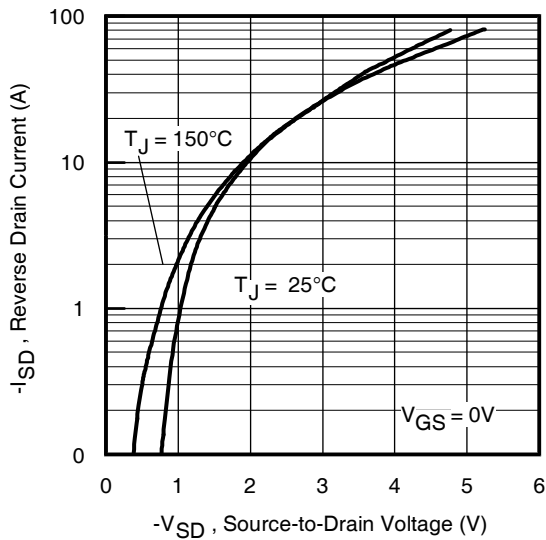


Fig 11. Typical Source-Drain Diode Forward Voltage

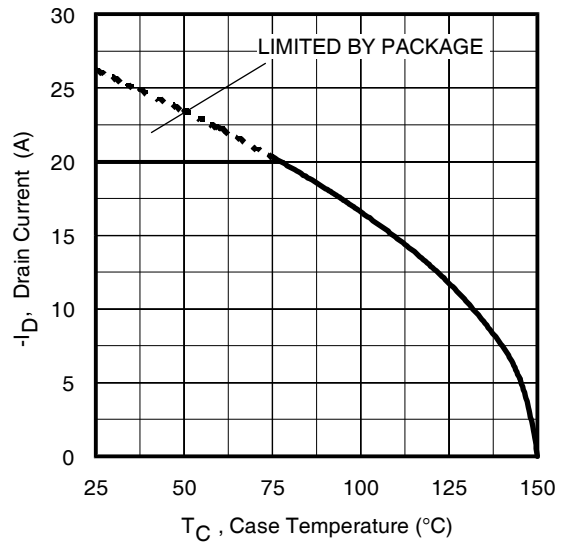


Fig 12. Maximum Drain Current Vs. Case Temperature

Pre-Irradiation

IRHLYS797034CM, 2N7625T3

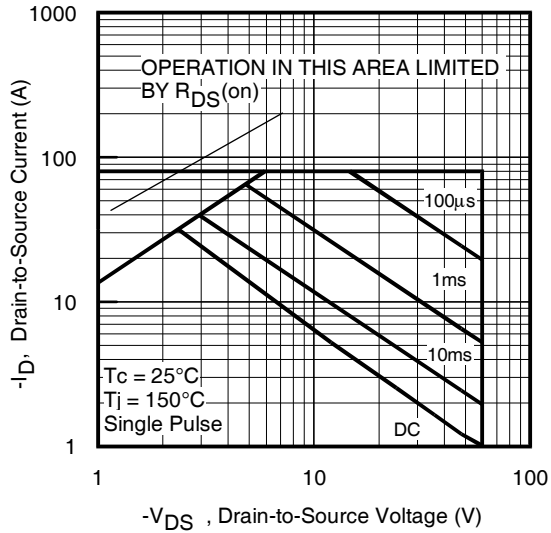


Fig 13. Maximum Safe Operating Area

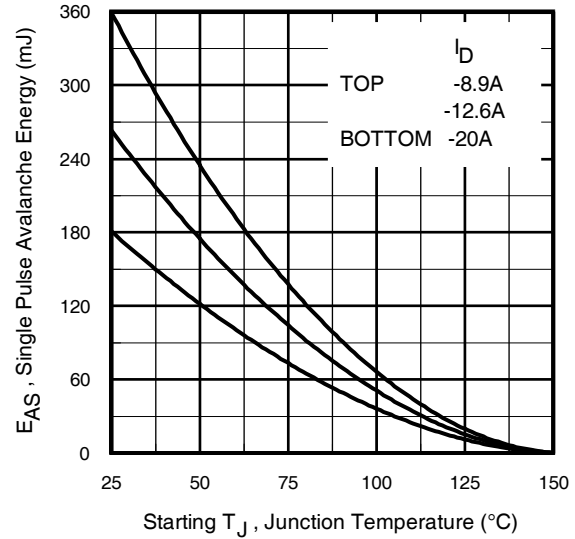


Fig 14. Maximum Avalanche Energy Vs. Drain Current

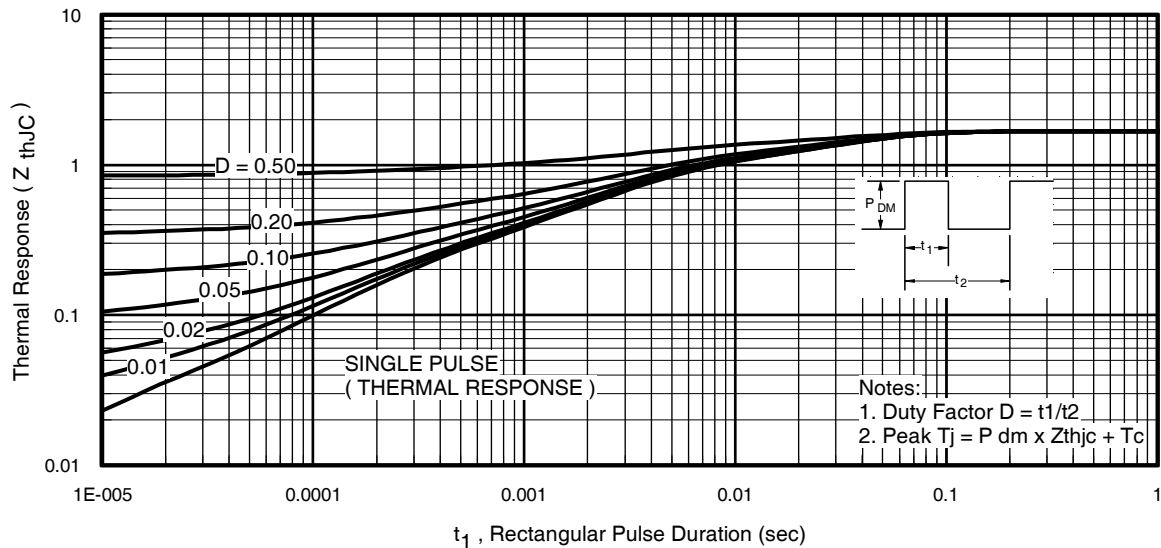


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

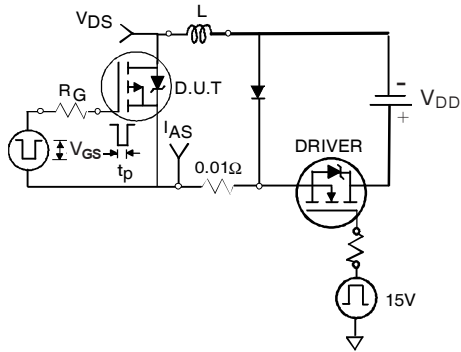


Fig 16a. Unclamped Inductive Test Circuit

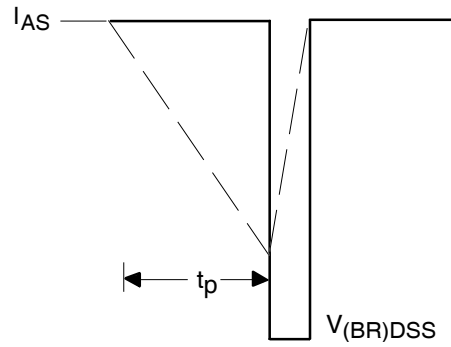


Fig 16b. Unclamped Inductive Waveforms

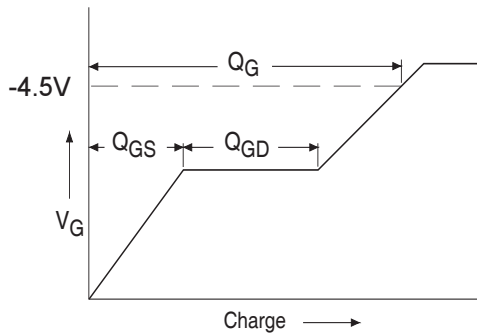


Fig 17a. Basic Gate Charge Waveform

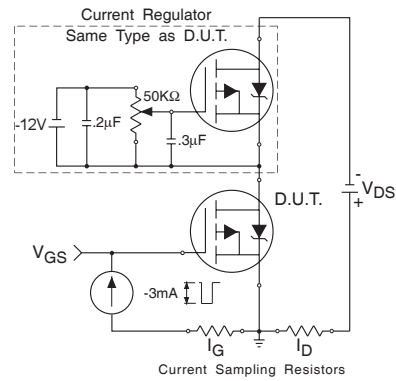


Fig 17b. Gate Charge Test Circuit

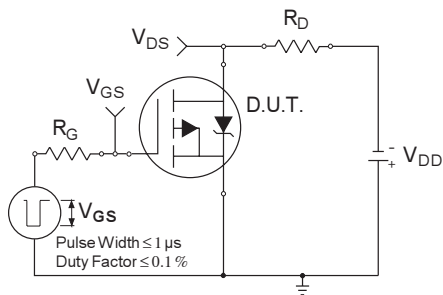


Fig 18a. Switching Time Test Circuit

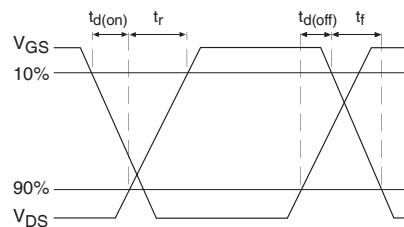


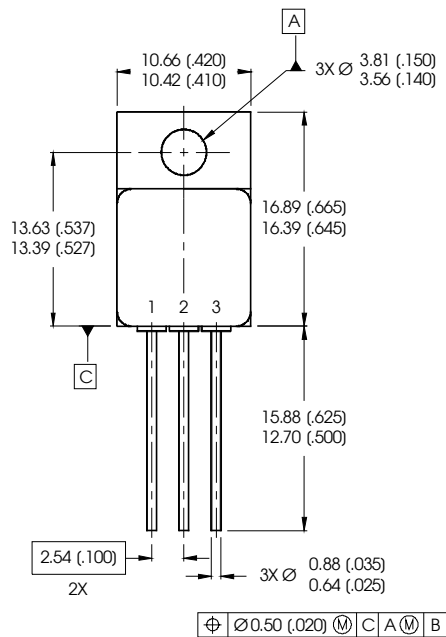
Fig 18b. Switching Time Waveforms

IRHLYS797034CM, 2N7625T3

Footnotes:

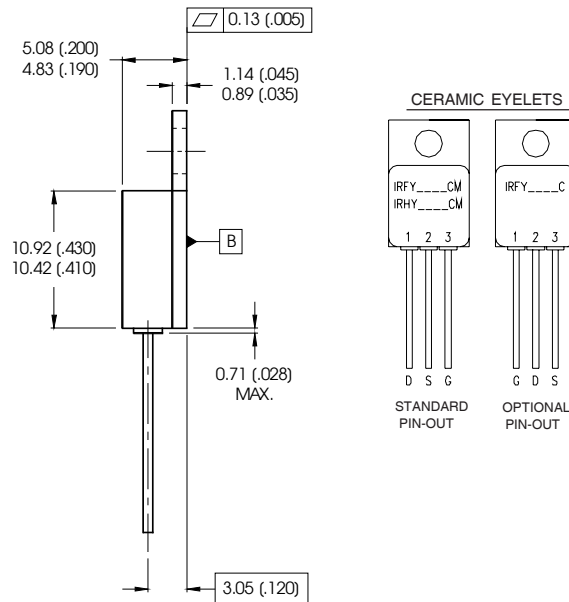
- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^{\circ}C$, $L = 0.9\text{ mH}$
Peak $I_L = -20A$, $V_{GS} = -10V$
- ③ $I_{SD} \leq -20A$, $di/dt \leq -359A/\mu s$,
 $V_{DD} \leq -60V$, $T_J \leq 150^{\circ}C$
- ④ Pulse width $\leq 300\text{ }\mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
-10 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
-48 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — Low Ohmic TO-257AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.



PIN ASSIGNMENTS

- 1 = DRAIN
2 = SOURCE
3 = GATE

CAUTION

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

International
IOR Rectifier

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Data and specifications subject to change without notice. 10/2010