

International IOR Rectifier

- Surface Mount (IRFR2405)
- Straight Lead (IRFU2405)
- Advanced Process Technology
- Dynamic dv/dt Rating
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	56@	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	40@	
I_{DM}	Pulsed Drain Current ①	220	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	130	mJ
I_{AR}	Avalanche Current①	34	A
E_{AR}	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

* When mounted on 1" square PCB (FR-4 or G-10 Material) .

For recommended footprint and soldering techniques refer to application note #AN-994

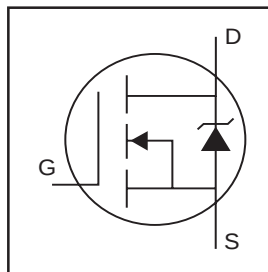
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PD - 95369A

IRFR2405PbF

IRFU2405PbF

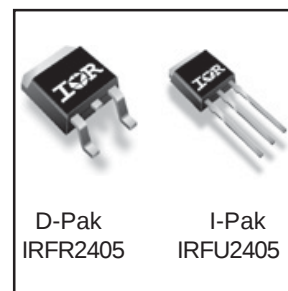
HEXFET® Power MOSFET



$$V_{DSS} = 55V$$

$$R_{DS(on)} = 0.016\Omega$$

$$I_D = 56A @$$

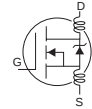


D-Pak
IRFR2405

I-Pak
IRFU2405

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0118	0.016	Ω	$V_{GS} = 10V, I_D = 34A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
g_{fs}	Forward Transconductance	30	—	—	S	$V_{DS} = 25V, I_D = 34A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	70	110	nC	$I_D = 34A$
Q_{gs}	Gate-to-Source Charge	—	16	23		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	19	29		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	130	—		$I_D = 34A$
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	78	—		$V_{GS} = 10V$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2430	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	470	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—		$f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	2040	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	350	—		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	350	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	56	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	220		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 34A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	62	93	ns	$T_J = 25^\circ\text{C}, I_F = 34A$
Q_{rr}	Reverse Recovery Charge	—	170	260	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.22mH$, $R_G = 25\Omega$, $I_{AS} = 34A$.
- ③ $I_{SD} \leq 34A$, $di/dt \leq 190A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A

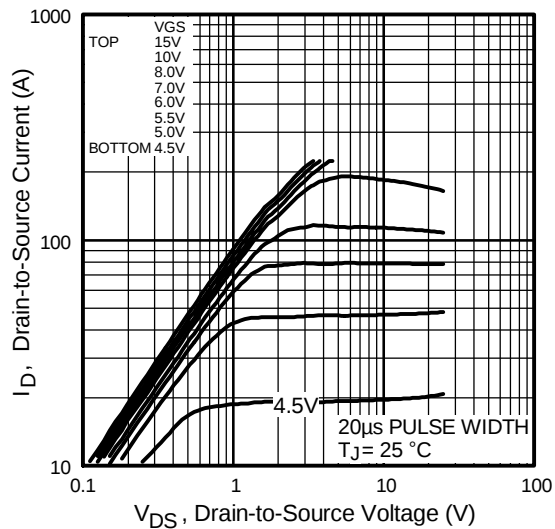


Fig 1. Typical Output Characteristics

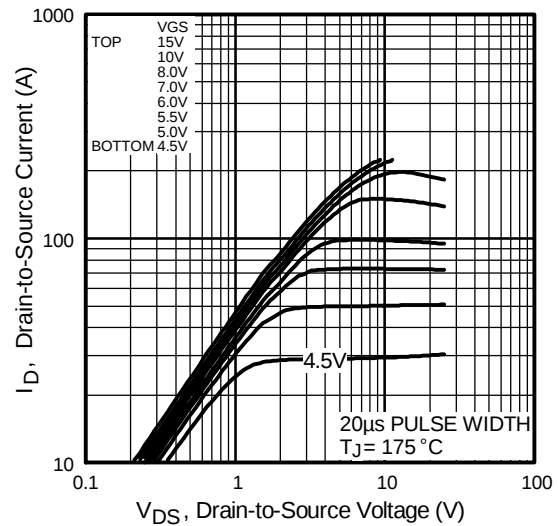


Fig 2. Typical Output Characteristics

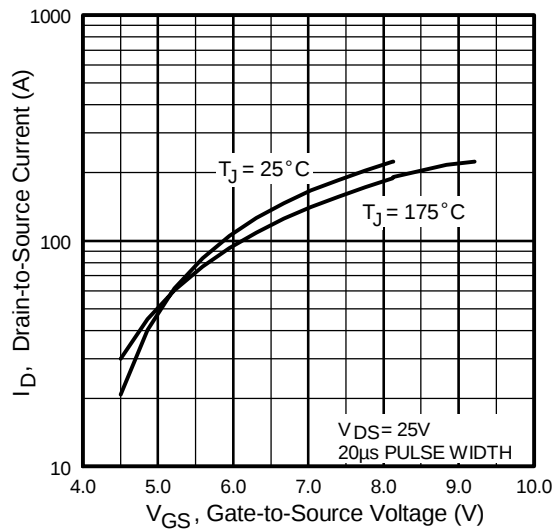


Fig 3. Typical Transfer Characteristics

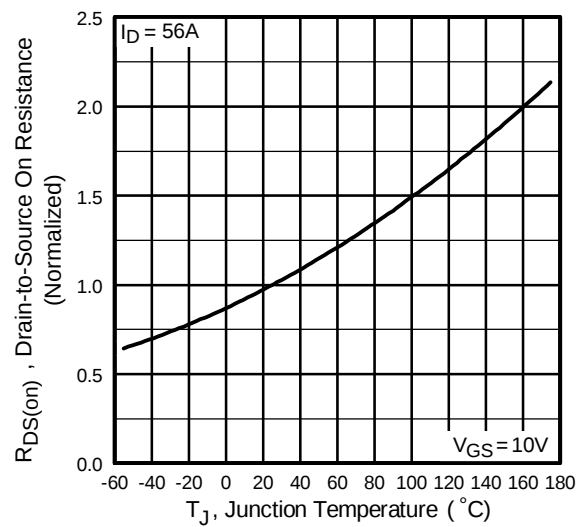


Fig 4. Normalized On-Resistance Vs. Temperature

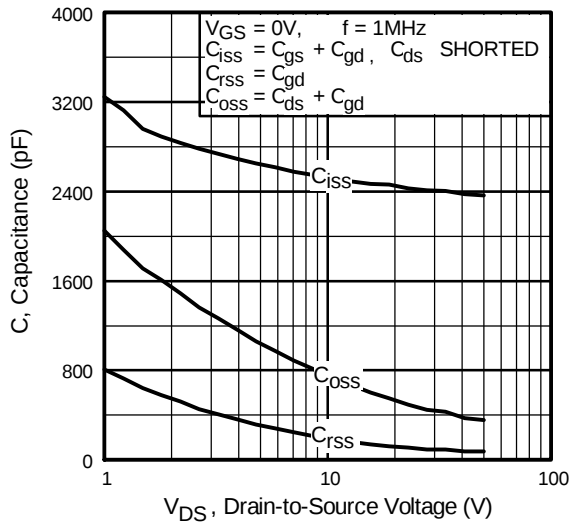


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

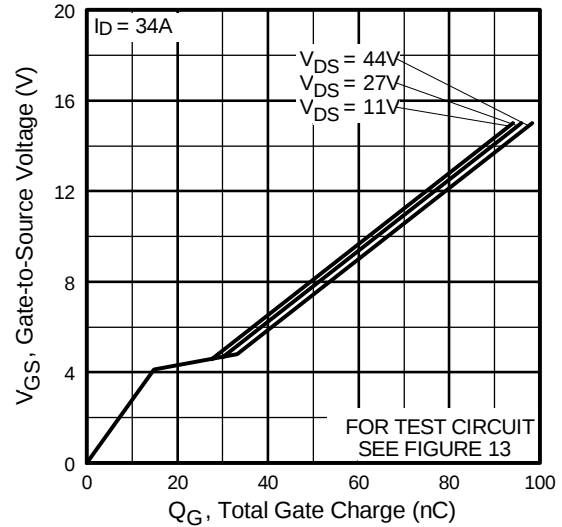


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

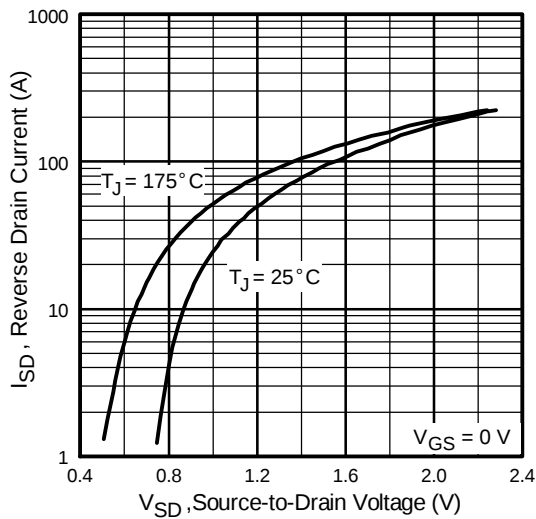


Fig 7. Typical Source-Drain Diode Forward Voltage

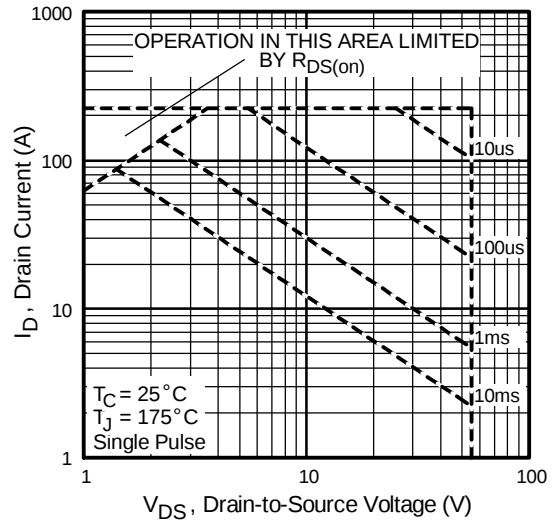


Fig 8. Maximum Safe Operating Area

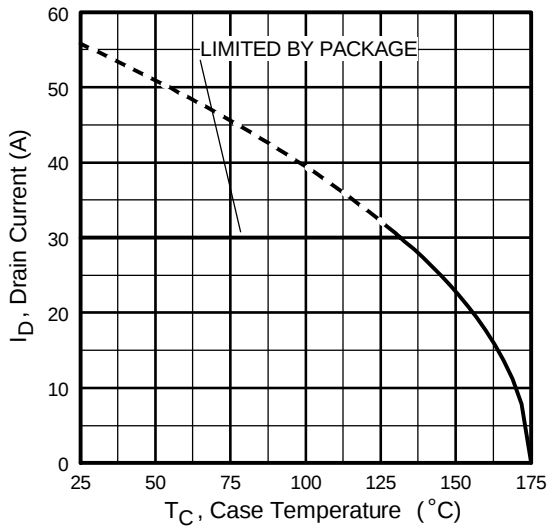


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

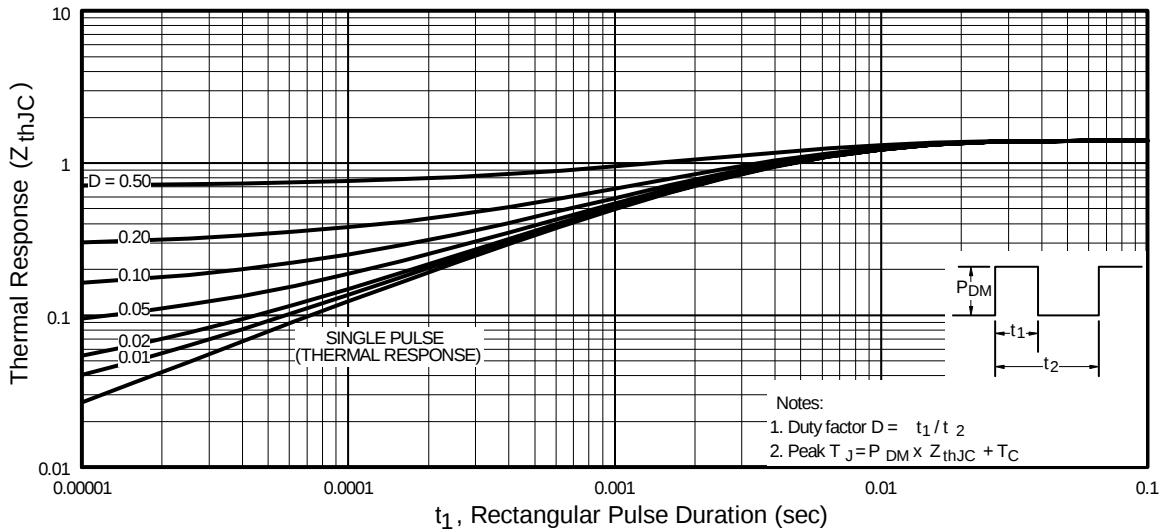


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Fig 12a. Unclamped Inductive Test Circuit

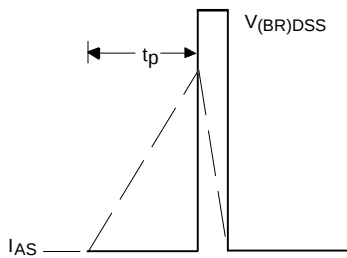


Fig 12b. Unclamped Inductive Waveforms

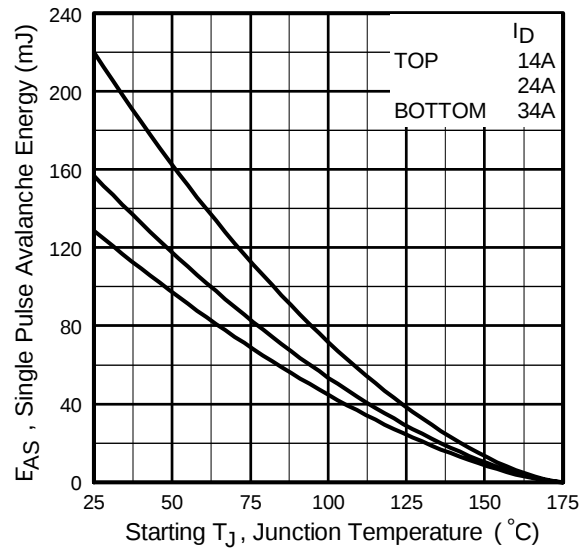


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

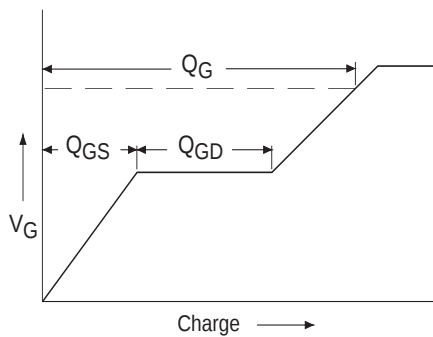


Fig 13a. Basic Gate Charge Waveform

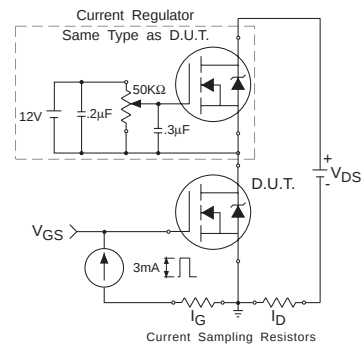


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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Technical drawing of a thermal pad assembly, showing multiple views and dimensions:

- Top View:** Shows a rectangular pad with dimensions E (total width), $b3$ (inner width), and $L3$ (height). It features a central circular feature with a diameter of $\varnothing 10.010$ (C35) and a square feature with a side length of $\varnothing 14.10$. A dimension $b1$ is also indicated.
- Side View:** Shows the profile of the pad with dimensions A (total height), $c2$ (height of the central feature), H (height of the main body), and A (height of the base). A detail callout **DETAIL A** points to the central feature.
- Detail A:** A magnified view of the central feature, showing a circular hole with a diameter of $\varnothing 10.010$ (C35) and a square feature with a side length of $\varnothing 14.10$.
- Bottom View:** Shows the underside of the pad with dimensions $2x b2$ (width of the base) and $2x a$ (width of the base). A dimension $3x b$ is also indicated.
- Section A-A:** A cross-sectional view of the pad, showing the internal structure. It includes dimensions e (thickness of the pad), L (length of the pad), and $(L1)$ (length of the base). A dimension $L2$ is also indicated. A label **SEATING PLANE** points to the base of the pad.
- Section C-C:** A cross-sectional view of the pad, showing the internal structure. It includes dimensions b (width of the pad), $c1$ (height of the pad), $b1$ (width of the base), and $c3$ (height of the base). Labels **PLATING** and **PLATING METAL** point to the internal layers.
- View A-A:** A cross-sectional view of the pad, showing the internal structure. It includes dimensions $E1$ (width of the pad), JE (height of the pad), and $D1$ (height of the base). A label **(DATUM A)** points to the base of the pad. A label **THERMAL PAD** points to the main body of the pad.

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.0 LEAD DIMENSION UNCONSTRAINED IN L5
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN	MAX	MIN	MAX	
A	2.18	2.39	.086	.094	5
A1		0.13		.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	1.95	4.56	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	0.46	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
E	5.21	—	.205	—	4
D1	6.35	6.75	.250	.265	6
E1	4.32	—	.170	—	4
	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.061 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
#	0"	10"	0"	10"	
#1	0"	15"	0"	15"	

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

Diagram illustrating the markings on a MOSFET package:

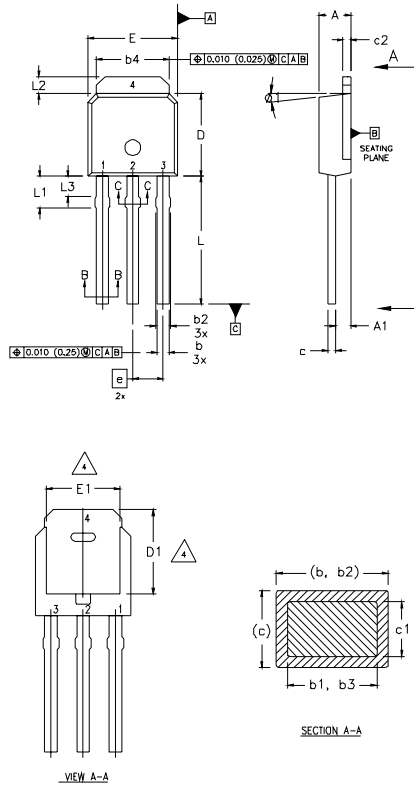
- INTERNATIONAL RECTIFIER LOGO**: Points to the IR logo on the package.
- PART NUMBER**: Points to the text **IRFU120** on the package.
- DATE CODE**: Points to the text **916A** on the package.
- YEAR 9 = 1999**: Points to the first digit of the date code (9).
- WEEK 16**: Points to the second digit of the date code (16).
- LINE A**: Points to the third digit of the date code (A).
- ASSEMBLY LOT CODE**: Points to the text **12 34** on the package.

Diagram illustrating the identification marks on the IRFU120 package:

- INTERNATIONAL RECTIFIER LOGO**: Points to the "IR" logo on the package.
- PART NUMBER**: Points to "IRFU120" on the package.
- DATE CODE**: Points to "P918A" on the package.
- ASSEMBLY LOT CODE**: Points to "12 34" on the package.
- P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)**: Points to the "P" in the date code.
- YEAR 9 = 1999**: Points to the "9" in the date code.
- WEEK 16**: Points to the "16" in the date code.
- A = ASSEMBLY SITE CODE**: Points to the "A" in the date code.

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

HEXFET

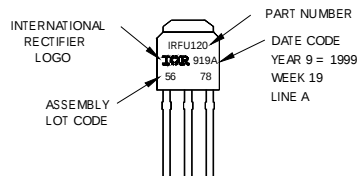
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	—	0.205	—	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	—	0.170	—	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15"	0"	15"	

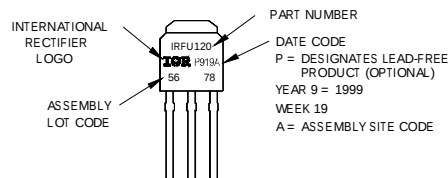
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line
position indicates "Lead-Free"



OR

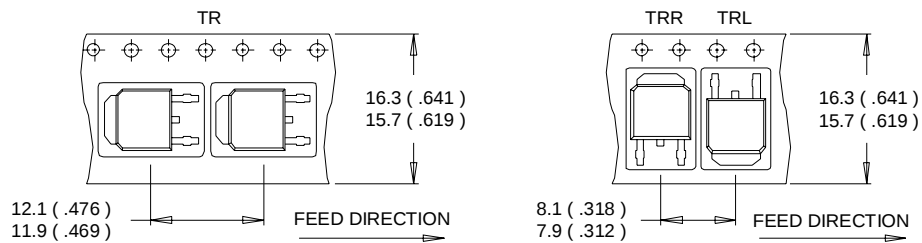


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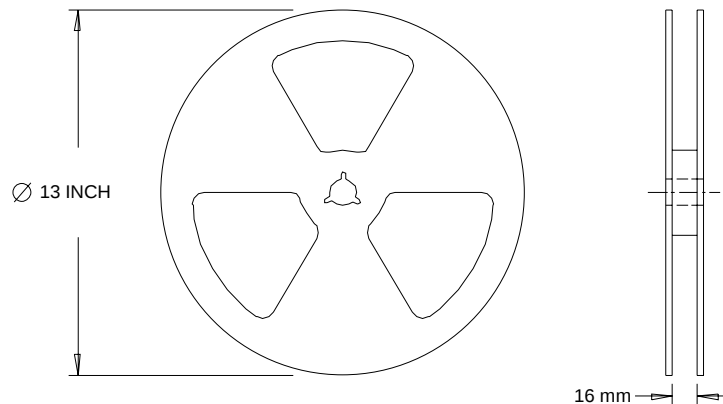
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

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TAC Fax: (310) 252-7903

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