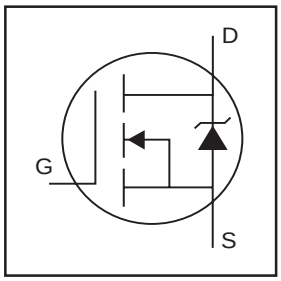
International
IOR Rectifier

PD - 95369A

IRFR2405PbF
IRFU2405PbF

HEXFET® Power MOSFET

- Surface Mount (IRFR2405)
- Straight Lead (IRFU2405)
- Advanced Process Technology
- Dynamic dv/dt Rating
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



V_{DSS} = 55V

$R_{DS(on)}$ = 0.016Ω

I_D = 56A⑥

Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

D-Pak IRFR2405 I-Pak IRFU2405

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	56⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	40⑥	
I_{DM}	Pulsed Drain Current ①	220	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	130	mJ
I_{AR}	Avalanche Current①	34	A
E_{AR}	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

* When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0118	0.016	Ω	V_{GS} = 10V, I_D = 34A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	30	—	—	S	V_{DS} = 25V, I_D = 34A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	70	110	nC	I_D = 34A
Q_{gs}	Gate-to-Source Charge	—	16	23		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	19	29		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = 28V
t_r	Rise Time	—	130	—		I_D = 34A
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		R_G = 6.8Ω
t_f	Fall Time	—	78	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2430	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	470	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	100	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	2040	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	350	—		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	350	—		V_{GS} = 0V, V_{DS} = 0V to 44V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	56⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	220		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 34A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	62	93	ns	T_J = 25°C, I_F = 34A
Q_{rr}	Reverse RecoveryCharge	—	170	260	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.22mH R_G = 25Ω, I_{AS} = 34A.

③ I_{SD} ≤ 34A, di/dt ≤ 190A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A

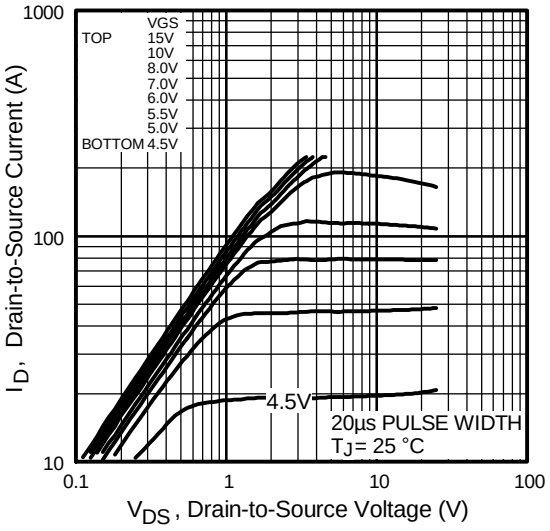


Fig 1. Typical Output Characteristics

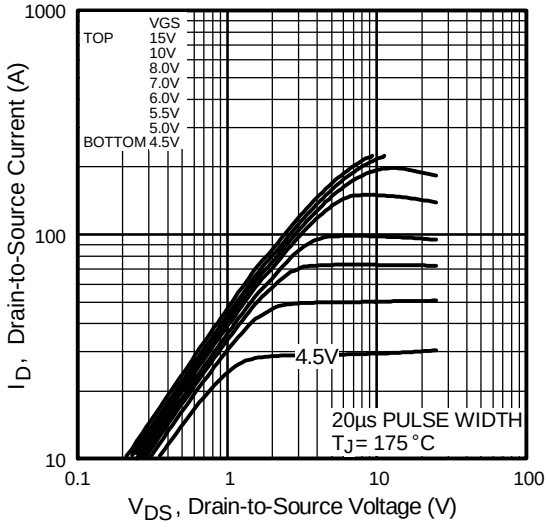


Fig 2. Typical Output Characteristics

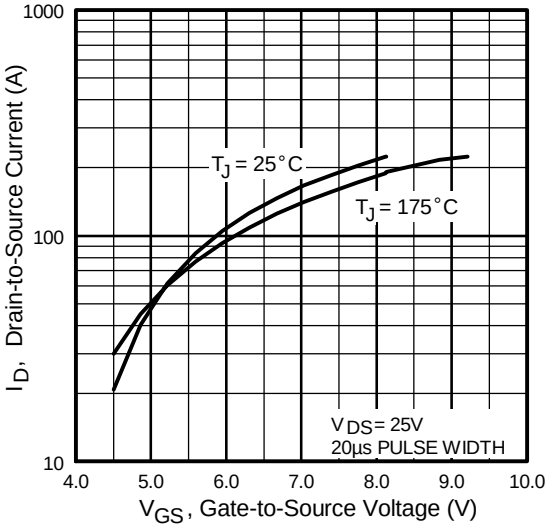


Fig 3. Typical Transfer Characteristics

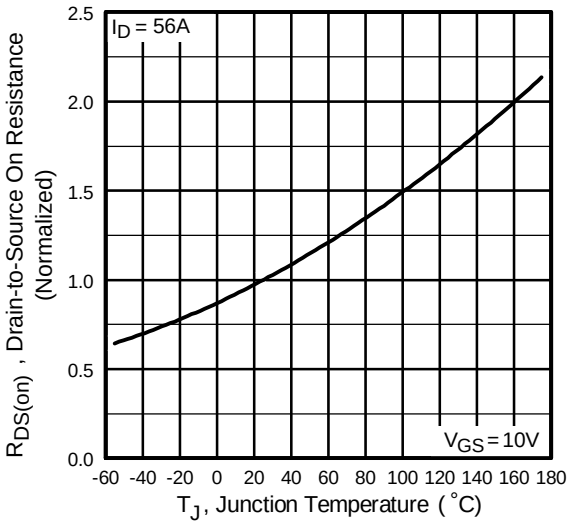


Fig 4. Normalized On-Resistance Vs. Temperature

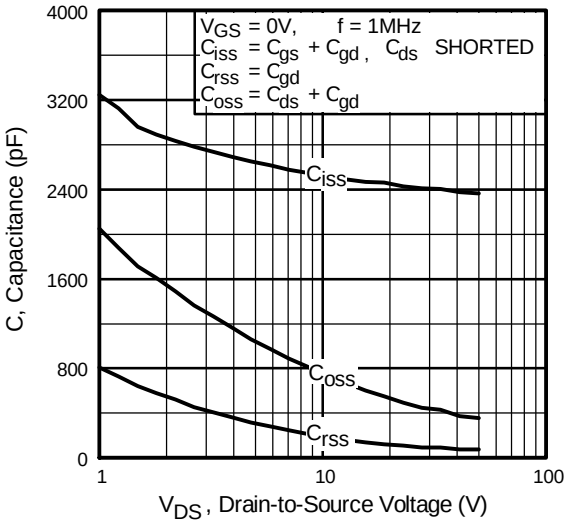


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

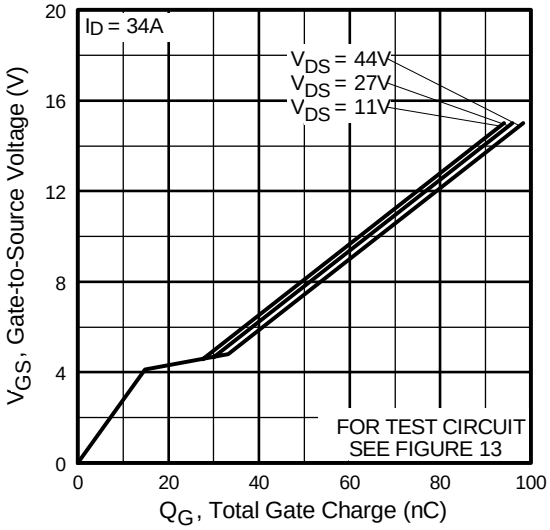


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

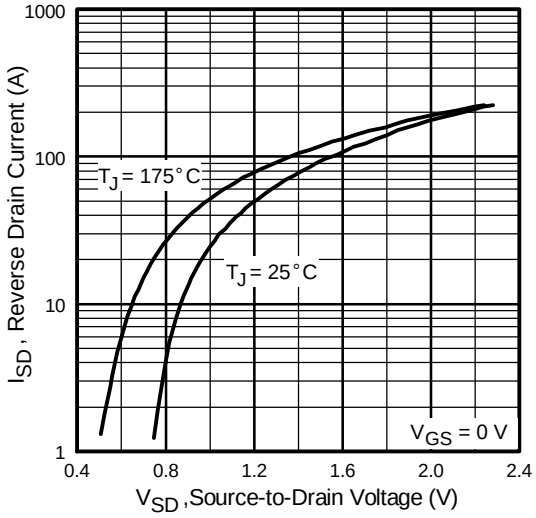


Fig 7. Typical Source-Drain Diode Forward Voltage

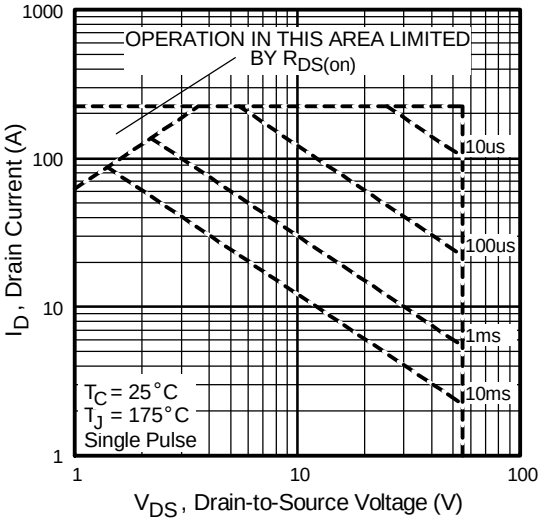


Fig 8. Maximum Safe Operating Area

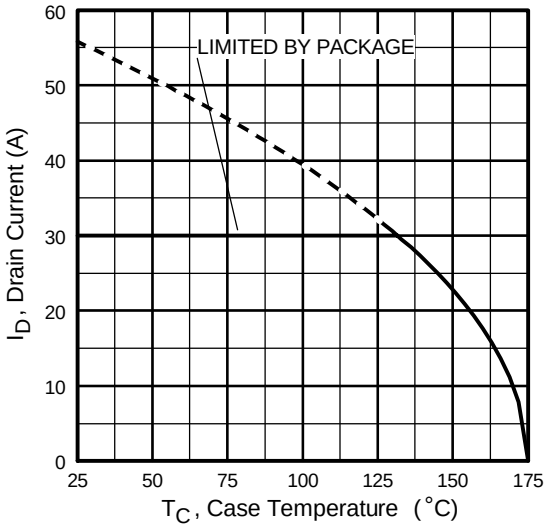


Fig 9. Maximum Drain Current Vs. Case Temperature

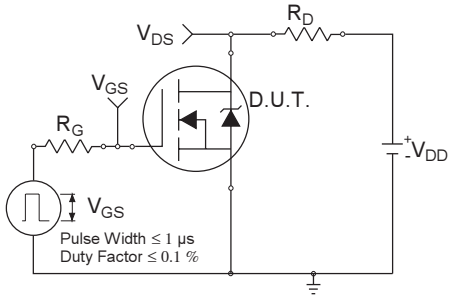


Fig 10a. Switching Time Test Circuit

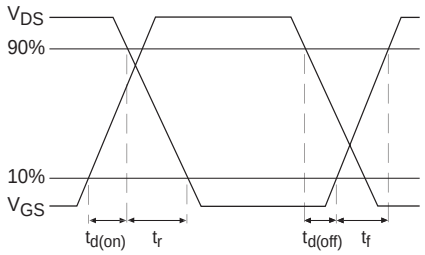


Fig 10b. Switching Time Waveforms

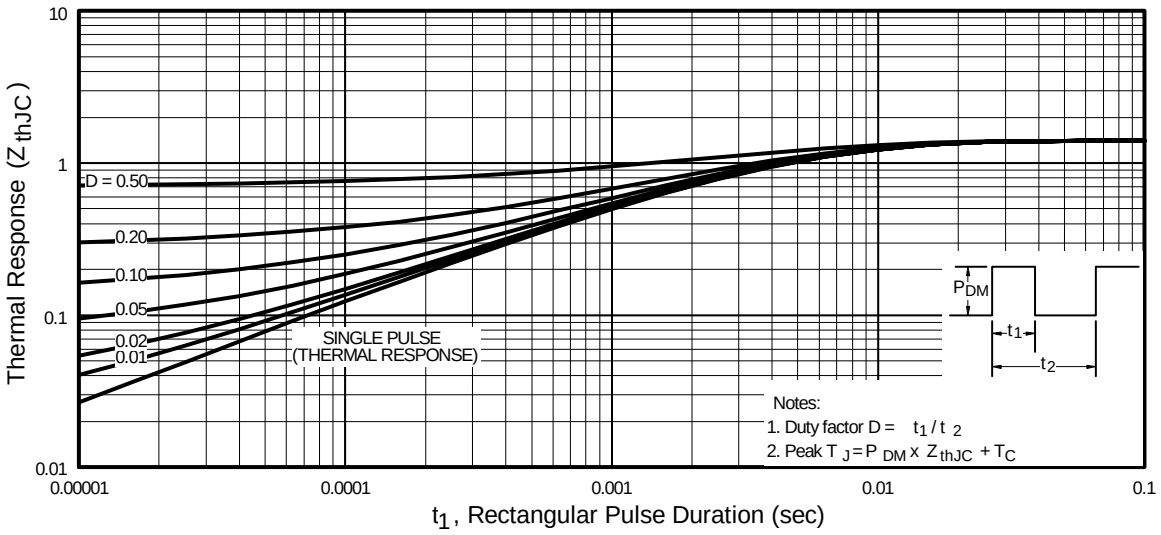


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

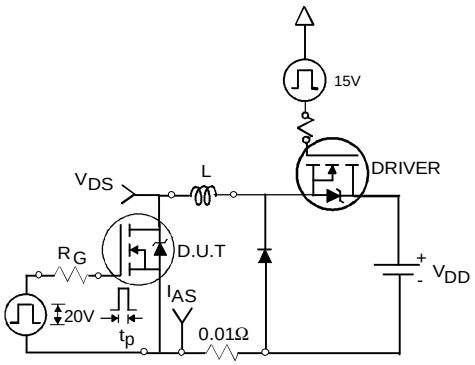


Fig 12a. Unclamped Inductive Test Circuit

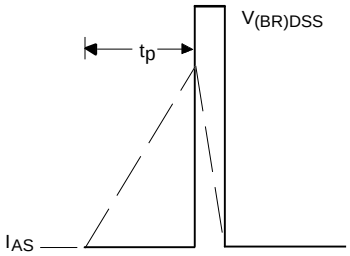


Fig 12b. Unclamped Inductive Waveforms

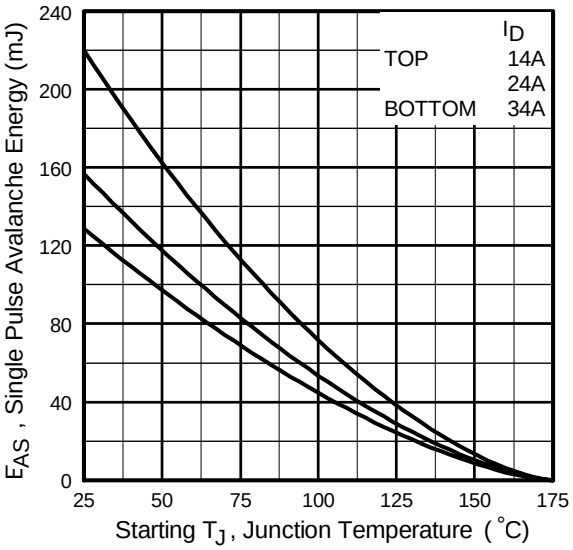


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

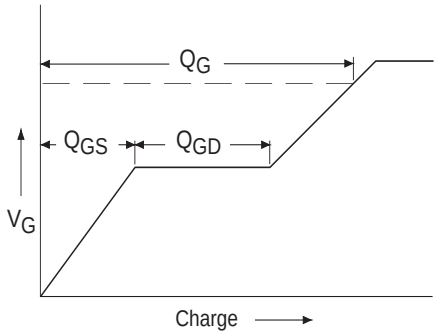


Fig 13a. Basic Gate Charge Waveform

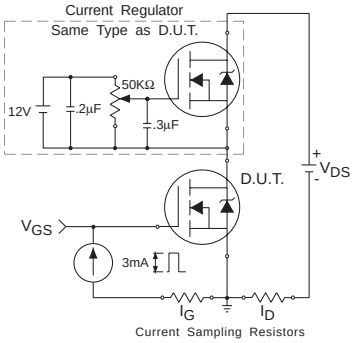
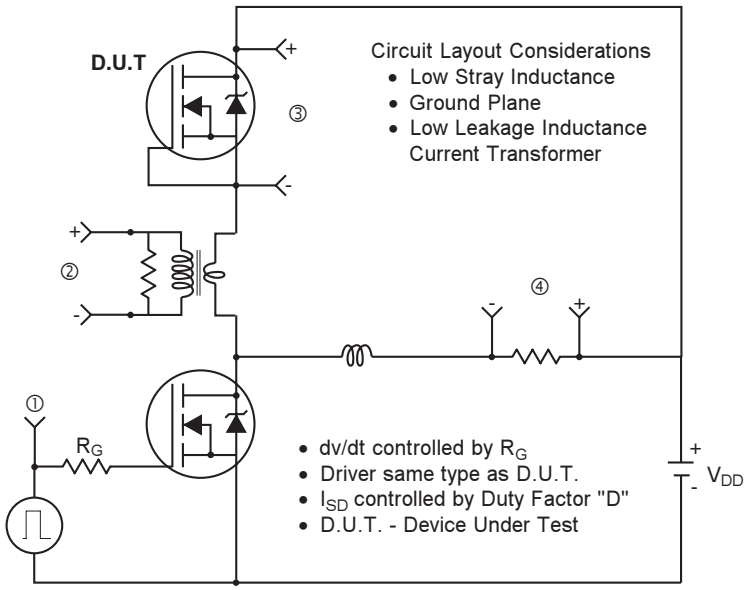
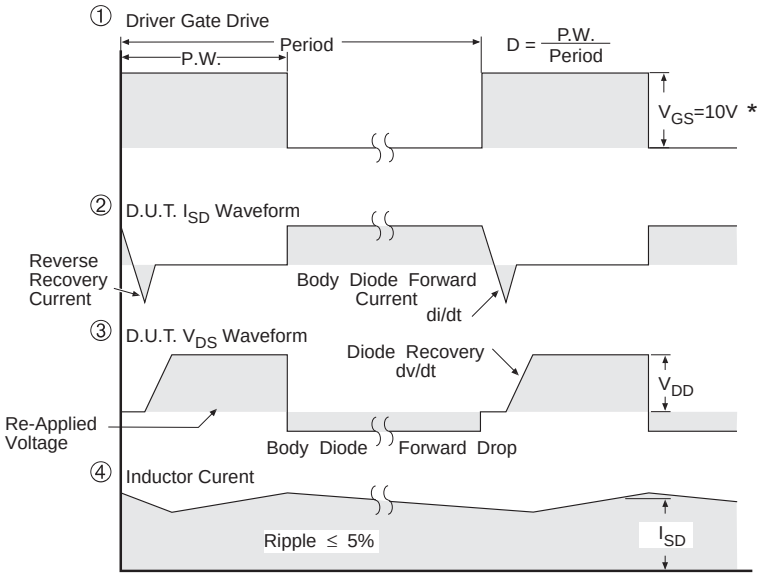


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

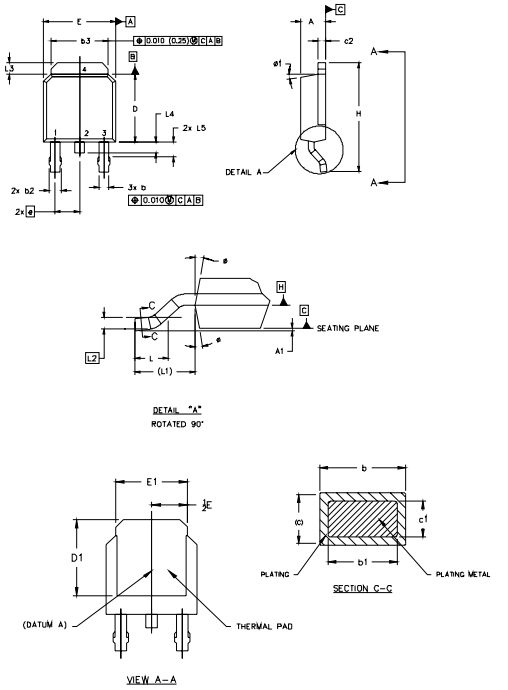




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline



NOTES:

1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.0 LEAD DIMENSION UNCONTROLLED IN L5
4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.0 SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540 FROM THE LEAD TIP.
6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170		4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

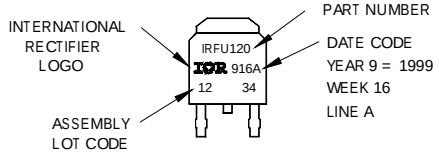
IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

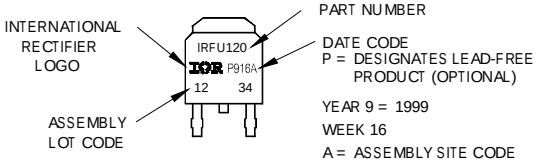
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

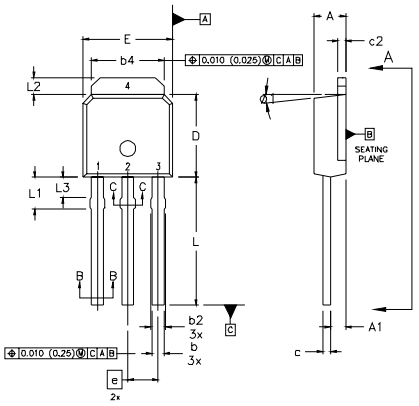


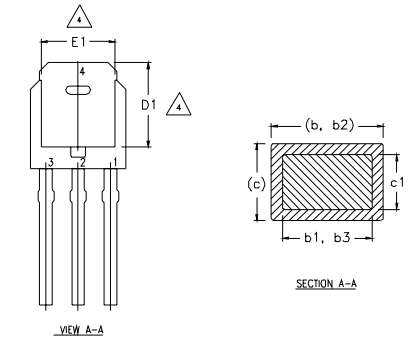
OR



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)





NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5 LEAD DIMENSION UNCONTROLLED IN L3.
6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
8 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	–	0.205	–	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	–	0.170	–	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

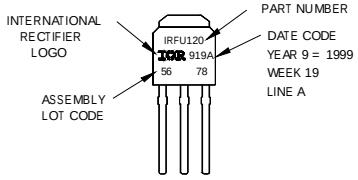
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

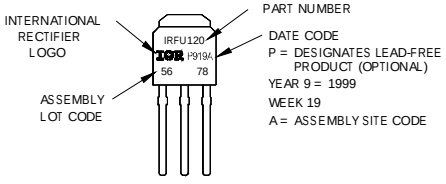
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

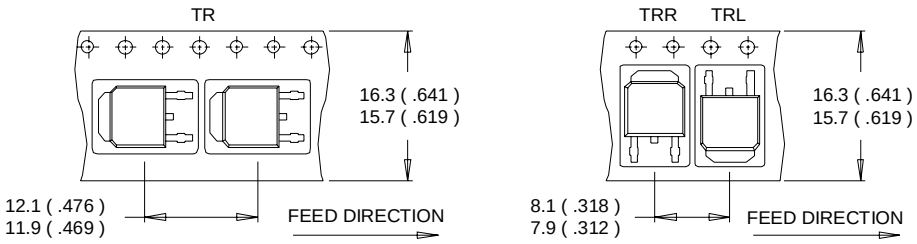


OR

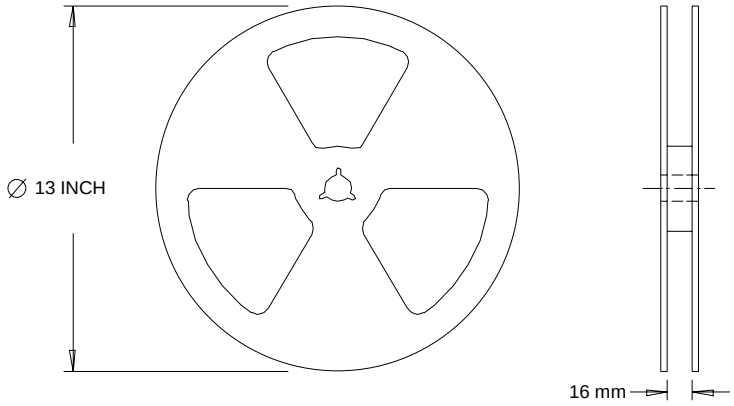


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 12/04