

International IOR Rectifier

HEXFET® POWER MOSFET

IRFN9240

N-CHANNEL

-200 Volt, 0.51Ω HEXFET

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry achieves very low on-state resistance combined with high transconductance.

HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

The Surface Mount Device (SMD-1) package represents another step in the continual evolution of surface mount technology. The SMD-1 will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the SMD-1 package to meet the specific needs of the power market by increasing the size of the termination pads, thereby enhancing thermal and electrical performance.

Product Summary

Part Number	BV _{DSS}	R _{DS(on)}	I _D
IRFN9240	-200V	0.51Ω	-11A

Features:

- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light-weight


Absolute Maximum Ratings

	Parameter	IRFN9240	Units
I _D @ V _{GS} = -10V, T _C = 25°C	Continuous Drain Current	-11	A
I _D @ V _{GS} = -10V, T _C = 100°C	Continuous Drain Current	-7	
I _{DM}	Pulsed Drain Current ①	-44	
P _D @ T _C = 25°C	Max. Power Dissipation	125	W
	Linear Derating Factor	1.0	W/K ⑤
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	500	mJ
I _{AR}	Avalanche Current ①	-11	A
E _{AR}	Repetitive Avalanche Energy ①	12.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Package Mounting Surface Temperature	300 (for 5 seconds)	
	Weight	2.6 (typical)	

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.20	—	V/°C	Reference to 25°C, I _D = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.51	Ω	V _{GS} = -10V, I _D = -7A ④
		—	—	0.52		V _{GS} = -10V, I _D = -11A
VGS(th)	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
gfs	Forward Transconductance	4.0	—	—	S (r)	V _{DS} > -15V, I _{DS} = -7A ④
IDSS	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = 0.8 x Max Rating, V _{GS} = 0V
		—	—	-250		V _{DS} = 0.8 x Max Rating V _{GS} = 0V, T _J = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
IGSS	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Qg	Total Gate Charge	28	—	60	nC	V _{GS} = -10V, I _D = -11A
Qgs	Gate-to-Source Charge	3.0	—	15		V _{DS} = Max. Rating x 0.5
Qgd	Gate-to-Drain ("Miller") Charge	4.5	—	38		see figures 6 and 13
td(on)	Turn-On Delay Time	—	—	35	ns	V _{DD} = -100V, I _D = -11A, R _G = 9.1Ω, V _{GS} = -10V
tr	Rise Time	—	—	85		
td(off)	Turn-Off Delay Time	—	—	85		
tf	Fall Time	—	—	65		see figure 10
LD	Internal Drain Inductance	—	2.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
LS	Internal Source Inductance	—	6.5	—		Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
Ciss	Input Capacitance	—	1200	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0 MHz see figure 5
Coss	Output Capacitance	—	570	—		
Crss	Reverse Transfer Capacitance	—	81	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-11	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-44		
V _{SD}	Diode Forward Voltage	—	—	-4.6	V	T _j = 25°C, I _S = -11A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	440	ns	T _j = 25°C, I _F = -11A, di/dt ≤ -100A/μs V _{DD} ≤ -50V ④
Q _{RR}	Reverse Recovery Charge	—	—	7.2	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RthJC	Junction-to-Case	—	—	1.0	K/W	
RthJ-PCB	Junction-to-PC Board	—	TBD	—		Soldered to a copper clad PC board

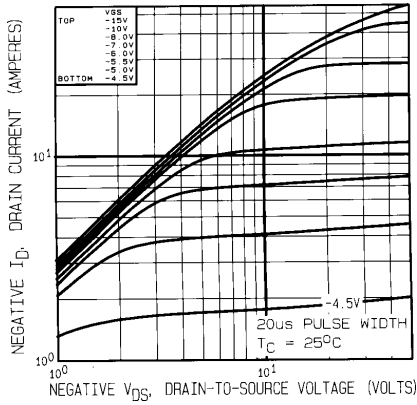


Fig. 1 — Typical Output Characteristics
 $T_C = 25^\circ\text{C}$

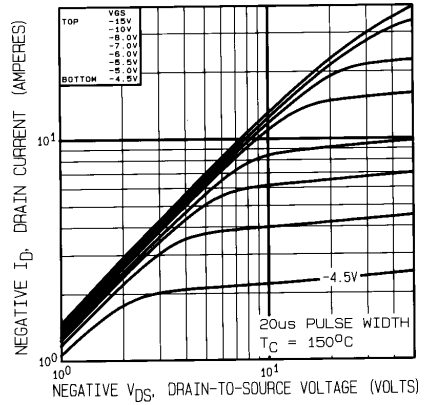


Fig. 2 — Typical Output Characteristics
 $T_C = 150^\circ\text{C}$

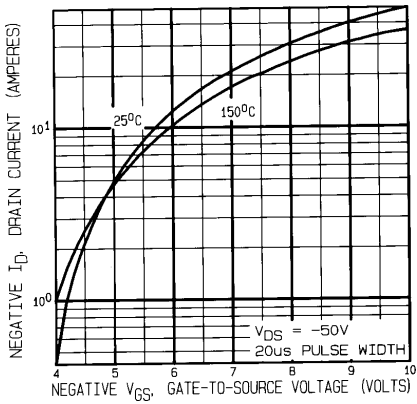


Fig. 3 — Typical Transfer Characteristics

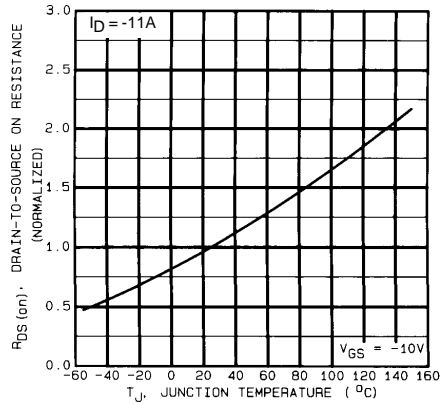


Fig. 4 — Normalized On-Resistance Vs. Temperature

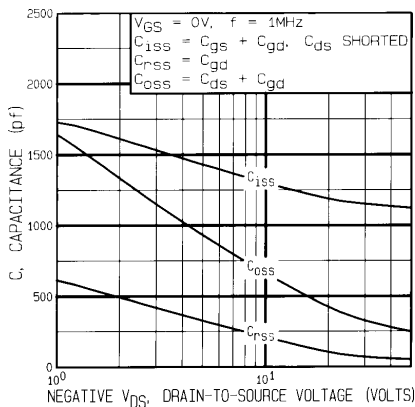


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

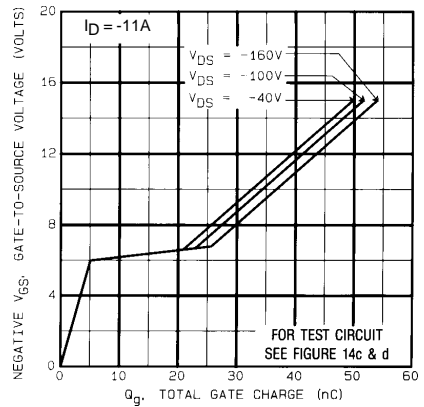


Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage
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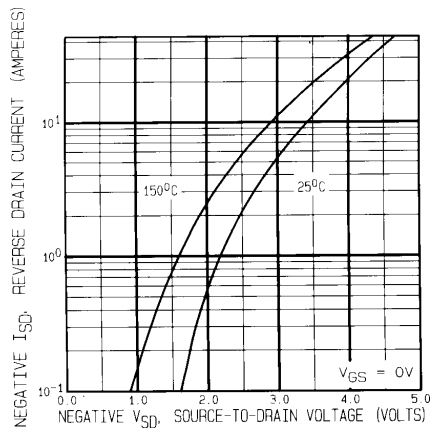


Fig. 7 — Typical Source-to-Drain Diode Forward Voltage

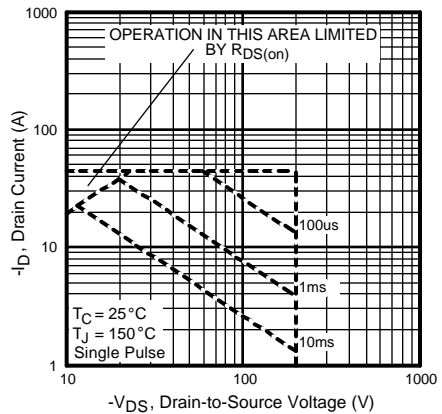


Fig. 8 — Maximum Safe Operating Area

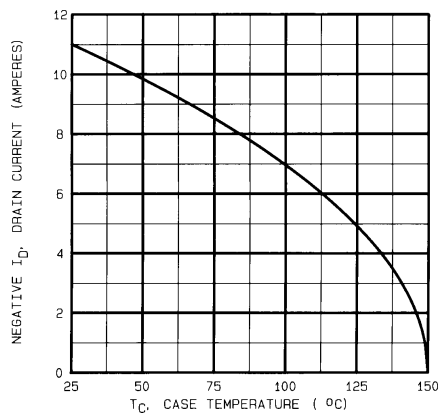


Fig. 9 — Maximum Drain Current Vs. Case Temperature

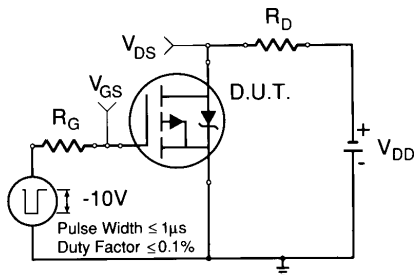


Fig. 10a — Switching Time Test Circuit

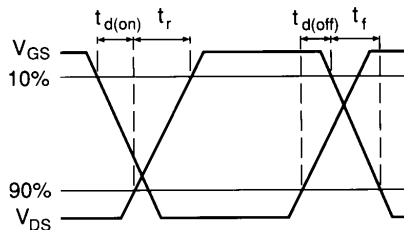


Fig. 10b — Switching Time Waveforms

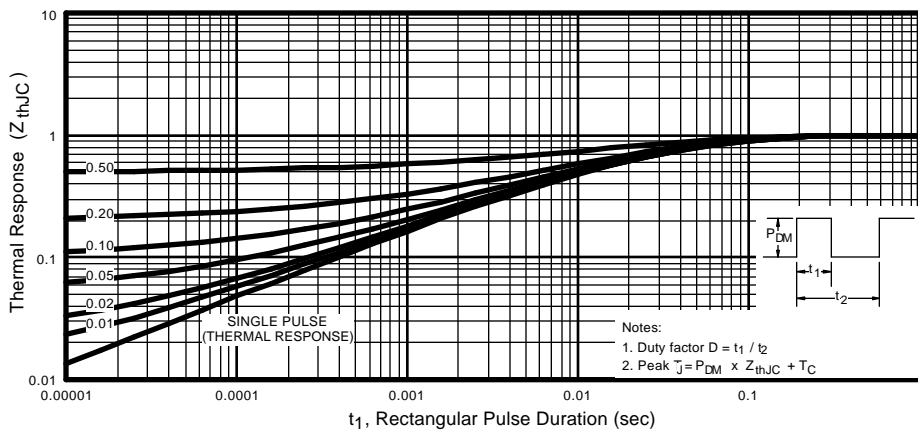


Fig. 11 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

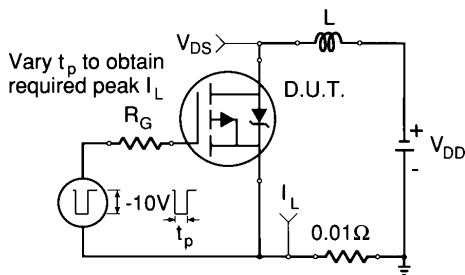


Fig. 12a — Unclamped Inductive Test Circuit

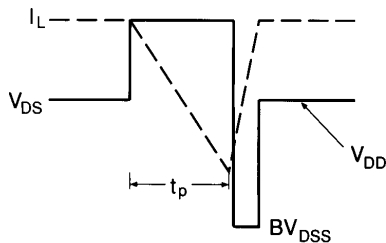


Fig. 12b — Unclamped Inductive Waveforms

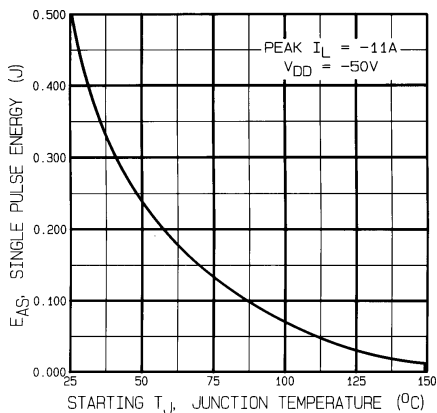


Fig. 12c — Max. Avalanche Energy vs. Current

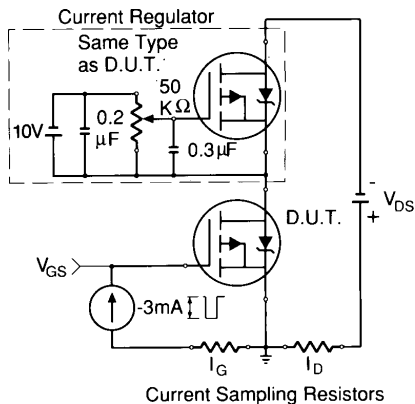


Fig. 13a — Gate Charge Test Circuit

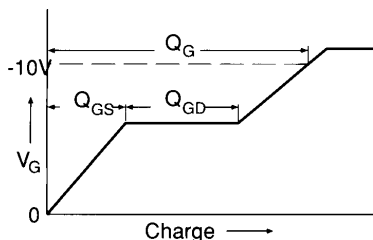
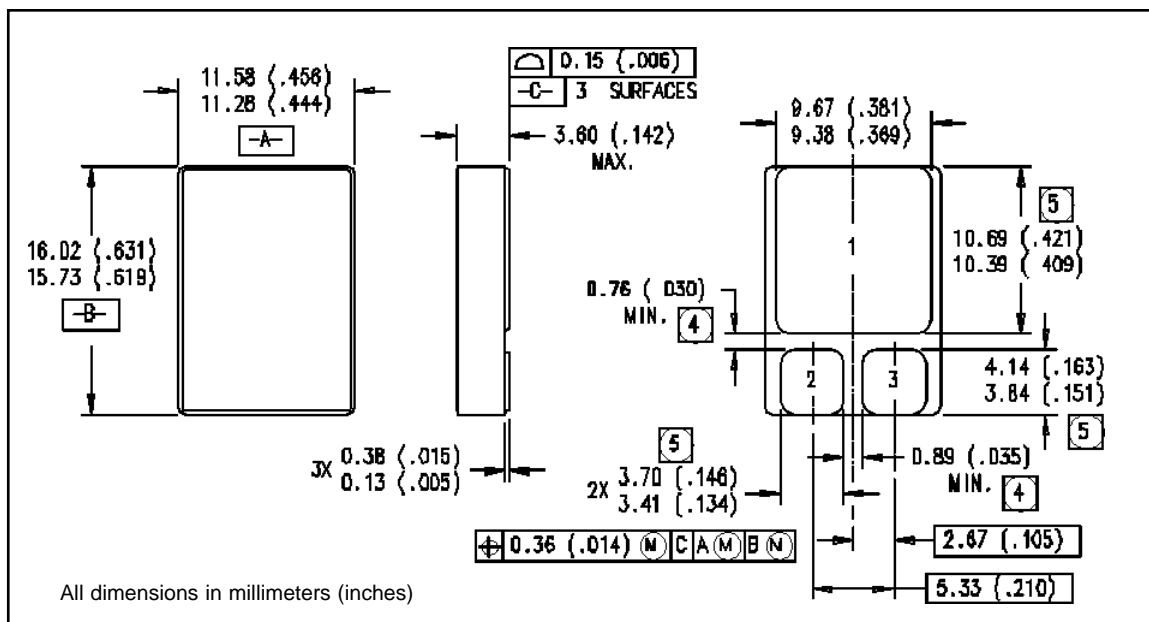


Fig. 13b — Basic Gate Charge Waveform

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
(see figure 11)
- ② @ $V_{DD} = -50V$, Starting $T_J = 25^\circ C$,
 $EAS = [0.5 * L * (I_L^2) * [BV_{DSS}/(BV_{DSS} - V_{DD})]$
Peak $I_L = -11A$, $V_{GS} = -10V$, $25 \leq R_G \leq 200\Omega$
- ③ $I_{SD} \leq -11A$, $di/dt \leq -150A/\mu s$,
 $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ $K/W = ^\circ C/W$
 $W/K = W/^\circ C$

Case Outline and Dimensions — SMD-1



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Data and specifications subject to change without notice

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