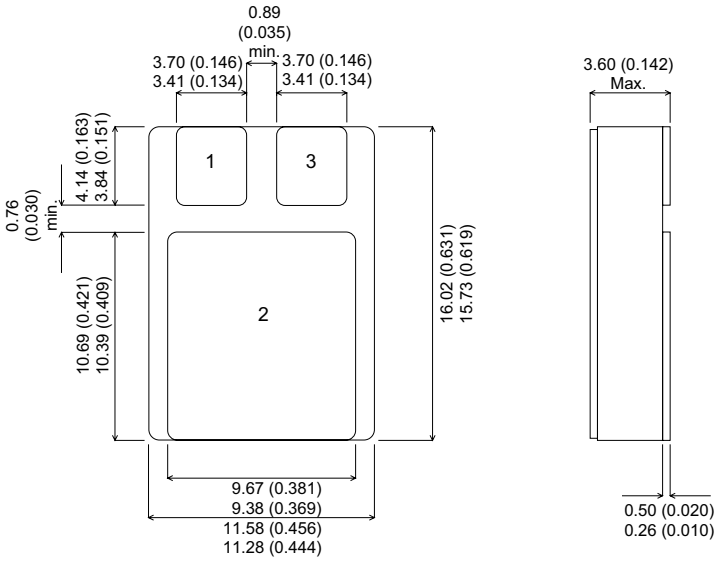
IRFN9140SMD

MECHANICAL DATA
Dimensions in mm (inches)



SMD1

Pad 1 – Source Pad 2 – Drain Pad 3 – Gate

P–CHANNEL POWER MOSFET

V_{DSS} **–100V**
$I_{D(cont)}$ **–14A**
$R_{DS(on)}$ **0.020Ω**

FEATURES

- **HERMETICALLY SEALED SURFACE MOUNT PACKAGE**
- **SMALL FOOTPRINT – EFFICIENT USE OF PCB SPACE.**
- **SIMPLE DRIVE REQUIREMENTS**
- **LIGHTWEIGHT**
- **HIGH PACKING DENSITIES**

Note: IRFxxxSM also available with pins 1 and 3 reversed.

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

V_{GS}	Gate – Source Voltage		±20V
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 25°C)	–14A
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 100°C)	–9.0A
I_{DM}	Pulsed Drain Current [1]		–56A
P_D	Power Dissipation @ T_{case} = 25°C		75W
	Linear Derating Factor		0.6W/°C
E_{AS}	Single Pulse Avalanche Energy [2]		500mJ
dv/dt	Peak Diode Recovery [3]		–5.0V/ns
T_J , T_{stg}	Operating and Storage Temperature Range		–55 to 150°C
T_L	Package Mounting Surface Temperature (for 5 sec)		300°C
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.67°C/W
$R_{\theta J–PCB}$	Thermal Resistance Junction to PCB (Typical)		4°C/W

Notes

1) Pulse Test: Pulse Width ≤ 300ms, δ ≤ 2%

2) @ V_{DD} = –25V , L ≥ 3.8mH , R_G = 25Ω , Peak I_L = –14A , Starting T_J = 25°C

3) @ I_{SD} ≤ –14A , di/dt ≤ –100A/μs , V_{DD} ≤ BV_{DSS} , T_J ≤ 150°C , SUGGESTED R_G = 9.1Ω

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SEME LAB

IRFN9140SMD

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise stated)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	STATIC ELECTRICAL RATINGS					
BV_{DSS}	Drain – Source Breakdown Voltage	V_{GS} = 0 I_D = –1mA	–100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Temperature Coefficient of Breakdown Voltage	Reference to 25°C I_D = –1mA		–0.087		V/°C
$R_{DS(on)}$	Static Drain – Source On–State Resistance [1]	V_{GS} = –10V I_D = –9A			0.20	Ω
		V_{GS} = –10V I_D = –14A			0.22	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = –250μA	–2		–4	V
g_{fs}	Forward Transconductance [1]	V_{DS} ≥ –15V I_{DS} = –9A	6.2			S(℧)
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V_{DS} = 0.8BV_{DSS}			–25	μA
		T_J = 125°C			–250	
I_{GSS}	Forward Gate – Source Leakage	V_{GS} = –20V			–100	nA
I_{GSS}	Reverse Gate – Source Leakage	V_{GS} = 20V			100	
	DYNAMIC CHARACTERISTICS					
C_{iss}	Input Capacitance	V_{GS} = 0		1400		pF
C_{oss}	Output Capacitance	V_{DS} = –25V		600		
C_{rss}	Reverse Transfer Capacitance	f = 1MHz		200		
Q_g	Total Gate Charge [1]	V_{GS} = –10V I_D = –14A V_{DS} = 0.5BV_{DSS}	31		60	nC
Q_{gs}	Gate – Source Charge [1]	I_D = –14A	3.7		13	nC
Q_{gd}	Gate – Drain (“Miller”) Charge [1]	V_{DS} = 0.5BV_{DSS}	7		35.2	
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –50V I_D = –14A R_G = 9.1Ω			35	ns
t_r	Rise Time				85	
$t_{d(off)}$	Turn–Off Delay Time				85	
t_f	Fall Time				65	
	SOURCE – DRAIN DIODE CHARACTERISTICS					
I_S	Continuous Source Current				–14	A
I_{SM}	Pulse Source Current [2]				–56	
V_{SD}	Diode Forward Voltage	I_S = –14A T_J = 25°C V_{GS} = 0			–4.2	V
t_{rr}	Reverse Recovery Time	I_F = –14A T_J = 25°C			280	ns
Q_{rr}	Reverse Recovery Charge	d_i / d_t ≤ –100A/μs V_{DD} ≤ –50V			3.6	μC
t_{on}	Forward Turn–On Time			negligible		
	PACKAGE CHARACTERISTICS					
L_D	Internal Drain Inductance (from centre of drain pad to die)			0.8		nH
L_S	Internal Source Inductance (from centre of source pad to end of source bond wire)			2.8		

Notes

1) Pulse Test: Pulse Width ≤ 300ms, δ ≤ 2%

2) Repetitive Rating – Pulse width limited by maximum junction temperature.

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