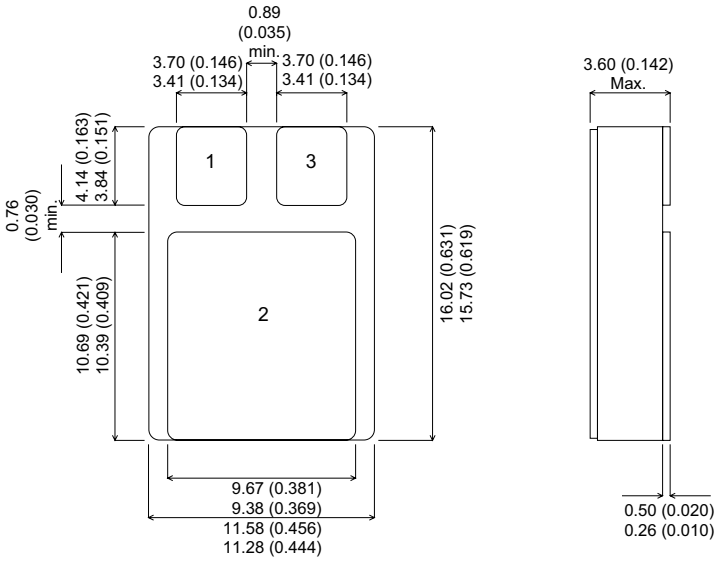
IRFN340SMD

MECHANICAL DATA
Dimensions in mm (inches)



SMD1 PACKAGE

Pad 1 – Source Pad 2 – Drain Pad 3 – Gate

N–CHANNEL POWER MOSFET

BV_{DSS}	400V
$I_{D(cont)}$	10A
$R_{DS(on)}$	0.55Ω

FEATURES

- **HERMETICALLY SEALED SURFACE MOUNT PACKAGE**
- **SMALL FOOTPRINT – EFFICIENT USE OF PCB SPACE.**
- **SIMPLE DRIVE REQUIREMENTS**
- **LIGHTWEIGHT**
- **HIGH PACKING DENSITIES**

Note: IRFxxxSM also available with pins 1 and 3 reversed.

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

V_{GS}	Gate – Source Voltage		±20V
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 25°C)	10A
I_D	Continuous Drain Current	(V_{GS} = 0 , T_{case} = 100°C)	6A
I_{DM}	Pulsed Drain Current [1]		40A
P_D	Power Dissipation @ T_{case} = 25°C		125W
	Linear Derating Factor		1.0W/°C
E_{AS}	Single Pulse Avalanche Energy [2]		650mJ
I_{AR}	Avalanche Energy [1]		10A
E_{AR}	Repetitive Avalanche Energy [1]		12.5mJ
dv/dt	Peak Diode Recovery [3]		4.0V/ns
T_J , T_{stg}	Operating and Storage Temperature Range		–55 to 150°C
T_L	Package Mounting Surface Temperature (for 5 sec)		300°C
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.0°C/W
$R_{\theta J–PCB}$	Thermal Resistance Junction to PCB (Typical)		TBD

Notes
1) Repetitive Rating – Pulse width limited by maximum junction temperature.
2) @ V_{DD} = 50V,Starting T_J = 25°C, E_{AS} =[0.5 * L* (I_L^2) * [BV_{DSS}/(BV_{DSS}-V_{DD})], Peak I_L = 10A V_{GS} = 10V, 25 ≤ R_G ≤ 200Ω
3) I_{SD} ≤ 10A , di/dt ≤ 120A/μs , V_{DD} ≤ BV_{DSS} , T_J ≤ 150°C
4) Pulse Test: Pulse Width ≤ 300ms, δ ≤ 2%

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SEME LAB

IRFN340SMD

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
	STATIC ELECTRICAL RATINGS						
BV_{DSS}	Drain – Source Breakdown Voltage	V_{GS} = 0	I_D = 1mA	400			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Temperature Coefficient of Breakdown Voltage	Reference to 25°C I_D = 1mA			0.46		V/°C
$R_{DS(on)}$	Static Drain – Source On–State Resistance[4]	V_{GS} = 10V	I_D = 6A			0.55	Ω
		V_{GS} = 10V	I_D = 10A			0.70	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}	I_D = 250µA	2		4	V
g_{fs}	Forward Transconductance[4]	V_{DS} ≥ 15V	I_{DS} = 6A	4.9			S(℧)
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0	V_{DS} = 0.8BV_{DSS}			25	µA
			T_J = 125°C			250	
I_{GSS}	Forward Gate – Source Leakage	V_{GS} = 20V				100	nA
I_{GSS}	Reverse Gate – Source Leakage	V_{GS} = –20V				–100	
	DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0			1400		pF
C_{oss}	Output Capacitance	V_{DS} = 25V			3500		
C_{rss}	Reverse Transfer Capacitance	f = 1MHz			2300		
Q_g	Total Gate Charge [1]	V_{GS} = 10V	I_D = 10A	32		65	nC
Q_{gs}	Gate – Source Charge [1]	V_{DS} = 0.5BV_{DSS}		2.2		10.0	
Q_{gd}	Gate – Drain (“Miller”) Charge [1]			13.8		40.5	
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 200V	I_D = 10A			2.5	ns
t_r	Rise Time					92	
$t_{d(off)}$	Turn–Off Delay Time	R_G = 9.1Ω	V_{GS} = 10V			79	
t_f	Fall Time					58	
	SOURCE – DRAIN DIODE CHARACTERISTICS						
I_S	Continuous Source Current					10	A
I_{SM}	Pulse Source Current [1]					40	
V_{SD}	Diode Forward Voltage[4]	I_S = 10A V_{GS} = 0	T_J = 25°C			1.5	V
t_{rr}	Reverse Recovery Time[4]	I_F = 10A	T_J = 25°C			600	ns
Q_{rr}	Reverse Recovery Charge[4]	d_i / d_t ≤ 100A/µs	V_{DD} ≤ 50V			5.6	µC
t_{on}	Forward Turn–On Time				Negligible		
	PACKAGE CHARACTERISTICS						
L_D	Internal Drain Inductance (from centre of drain pad to die)				2.0		nH
L_S	Internal Source Inductance (from centre of source pad to end of source bond wire)				6.5		

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