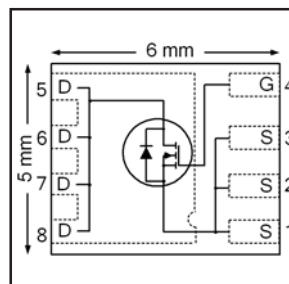


IRFH5004PbF

HEXFET® Power MOSFET

V_{DS}	40	V
R_{DS(on)} max (@ V _{GS} = 10V)	2.6	mΩ
Q_g (typical)	73	nC
R_G (typical)	1.2	Ω
I_D (@ T _{C(Bottom)} = 25°C)	100 ⑥	A



Applications

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications
- Boost Converters

Features and Benefits

Features

Low R _{DS(on)} (≤ 2.6mΩ)
Low Thermal Resistance to PCB (≤ 0.5°C/W)
100% R _g tested
Low Profile (≤ 0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in

⇒

Benefits

Lower Conduction Losses
Enables better thermal dissipation
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH5004TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRFH5004TR2PBF	PQFN 5mm x 6mm	Tape and Reel	1000	

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	40	V
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	28	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	23	
I _D @ T _{C(Bottom)} = 25°C	Continuous Drain Current, V _{GS} @ 10V ⑥	100	
I _D @ T _{C(Bottom)} = 100°C	Continuous Drain Current, V _{GS} @ 10V ⑥	100	
I _{DM}	Pulsed Drain Current ①	400	
P _D @ T _A = 25°C	Power Dissipation ⑤	3.6	W
P _D @ T _{C(Bottom)} = 25°C	Power Dissipation ⑤	250	
	Linear Derating Factor ⑤	0.029	W/°C
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		

Notes ① through ⑥ are on page 8

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02/08/2010

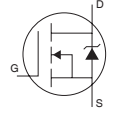
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.1	2.6	m Ω	$V_{GS} = 10V, I_D = 50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.6	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
gfs	Forward Transconductance	91	—	—	S	$V_{DS} = 15V, I_D = 50A$
Q_g	Total Gate Charge	—	73	110	nC	$V_{DS} = 20V$ $V_{GS} = 10V$ $I_D = 50A$ See Fig.17 & 18
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	15	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	6.1	—		
Q_{gd}	Gate-to-Drain Charge	—	27	—		
Q_{godr}	Gate Charge Overdrive	—	25	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	33.1	—		
Q_{oss}	Output Charge	—	27	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.2	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 20V, V_{GS} = 10V$ $I_D = 50A$ $R_G = 1.8\Omega$ See Fig.15
t_r	Rise Time	—	39	—		
$t_{d(off)}$	Turn-Off Delay Time	—	28	—		
t_f	Fall Time	—	16	—		
C_{iss}	Input Capacitance	—	4490	—	pF	$V_{GS} = 0V$ $V_{DS} = 20V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	970	—		
C_{rss}	Reverse Transfer Capacitance	—	460	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	340	mJ
I_{AR}	Avalanche Current ①	—	50	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ⑥	—	—	100	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	32	48	ns	$T_J = 25^\circ\text{C}, I_F = 50A, V_{DD} = 20V$
Q_{rr}	Reverse Recovery Charge	—	100	150	nC	$di/dt = 300A/\mu s$ ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	0.5	$^\circ\text{C/W}$
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	15	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	35	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ⑤	—	33	

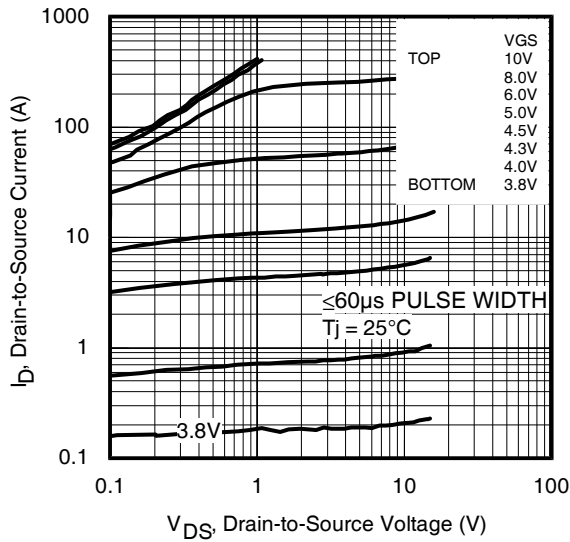


Fig 1. Typical Output Characteristics

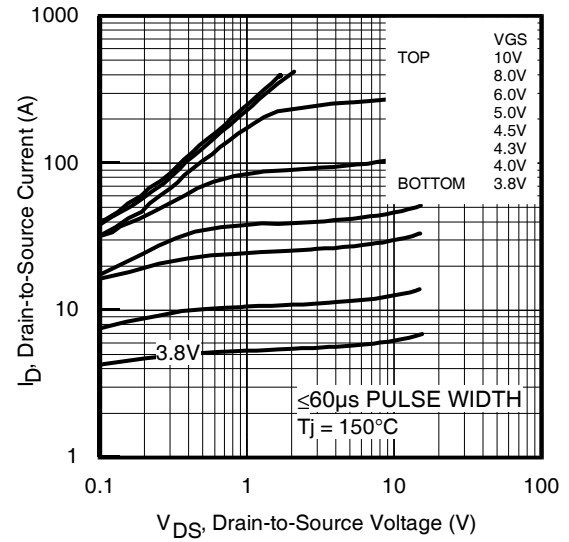


Fig 2. Typical Output Characteristics

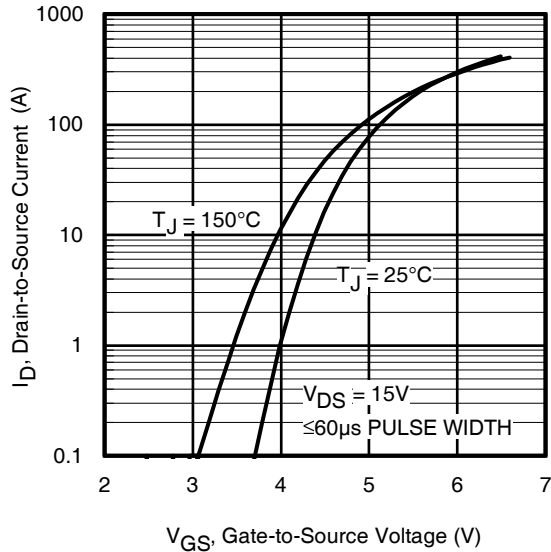


Fig 3. Typical Transfer Characteristics

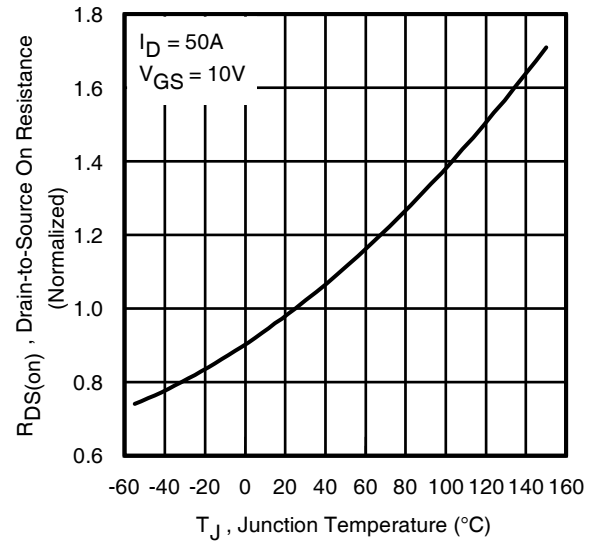


Fig 4. Normalized On-Resistance vs. Temperature

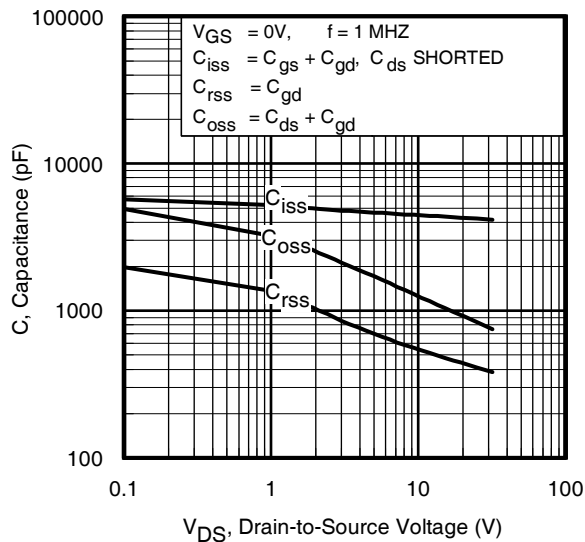


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
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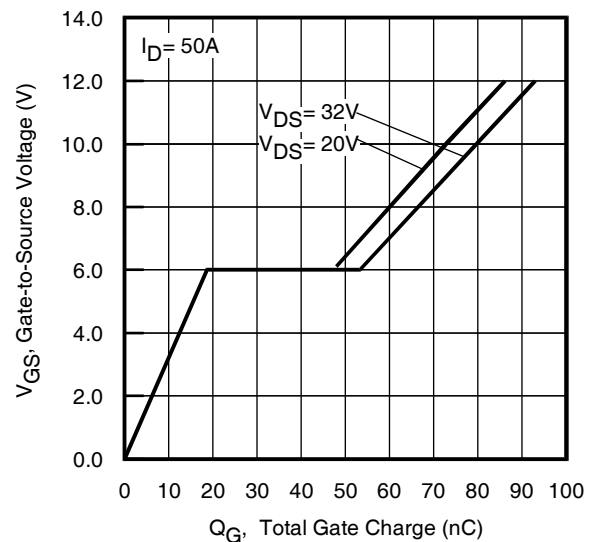


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage
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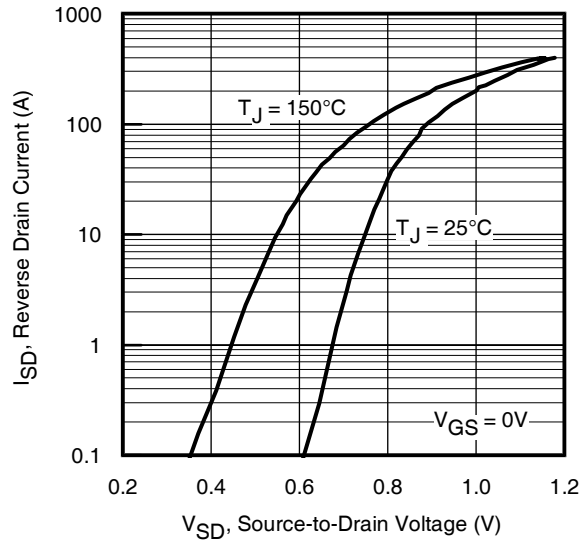


Fig 7. Typical Source-Drain Diode Forward Voltage

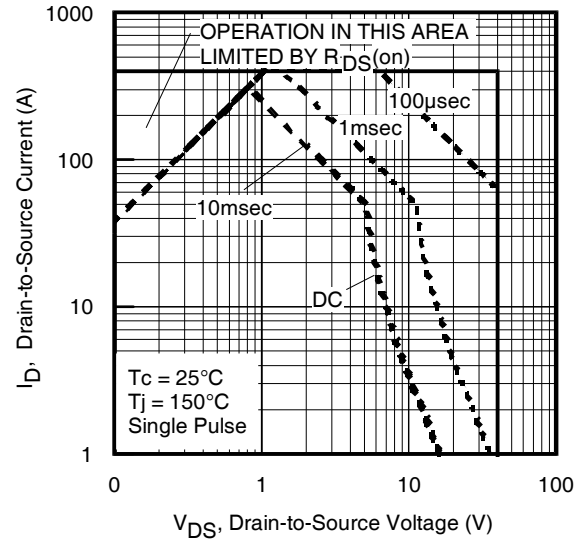


Fig 8. Maximum Safe Operating Area

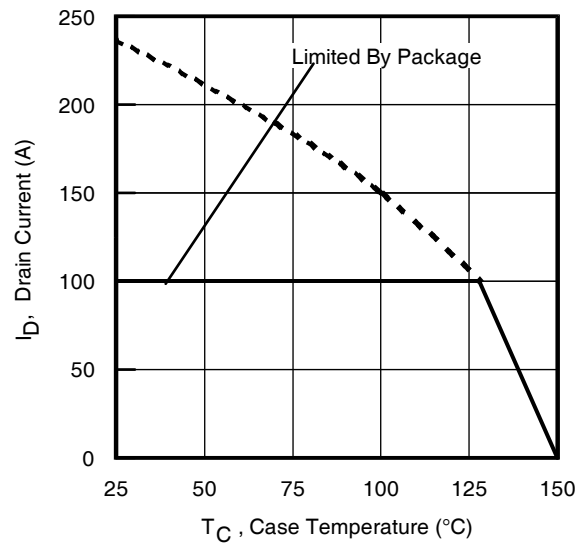


Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

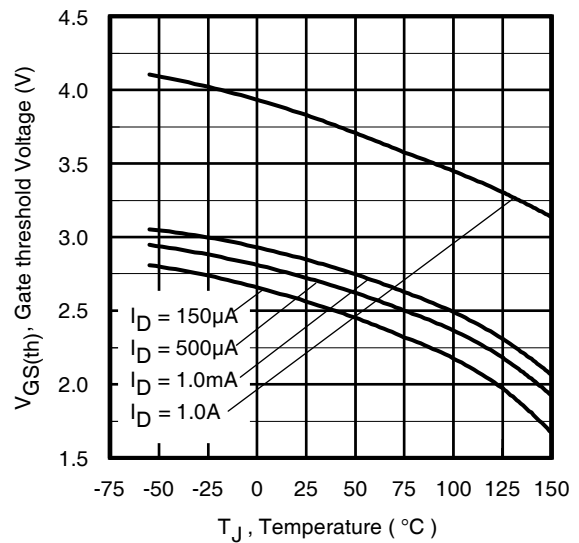


Fig 10. Threshold Voltage vs. Temperature

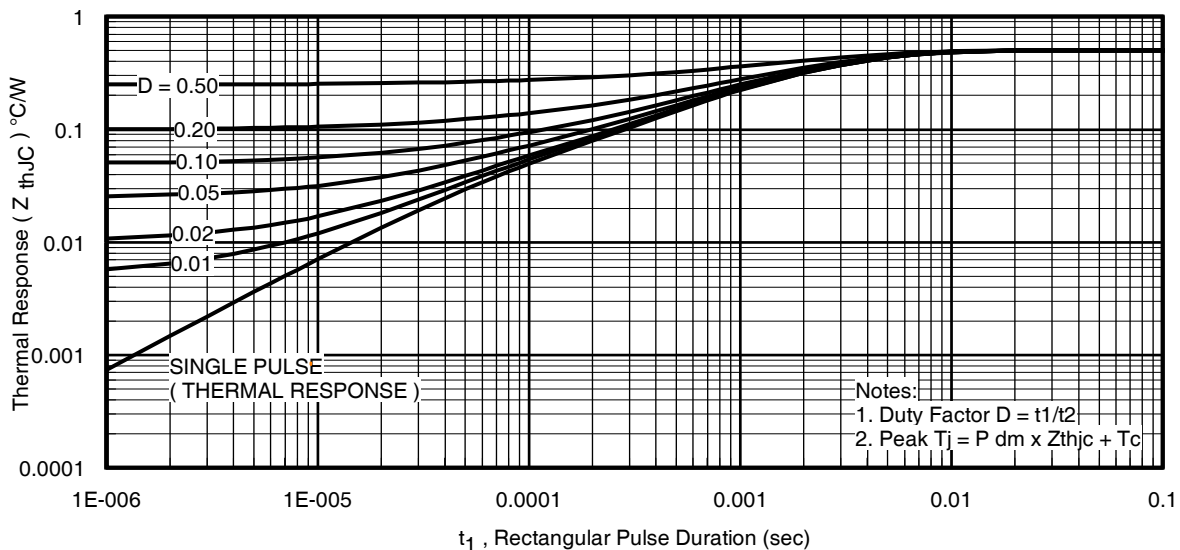


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

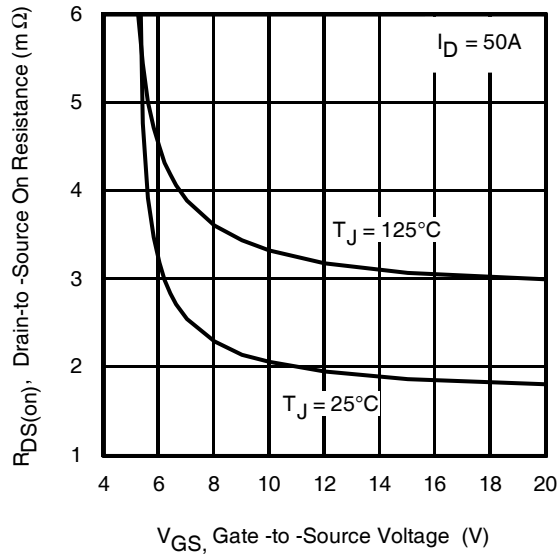


Fig 12. On-Resistance vs. Gate Voltage

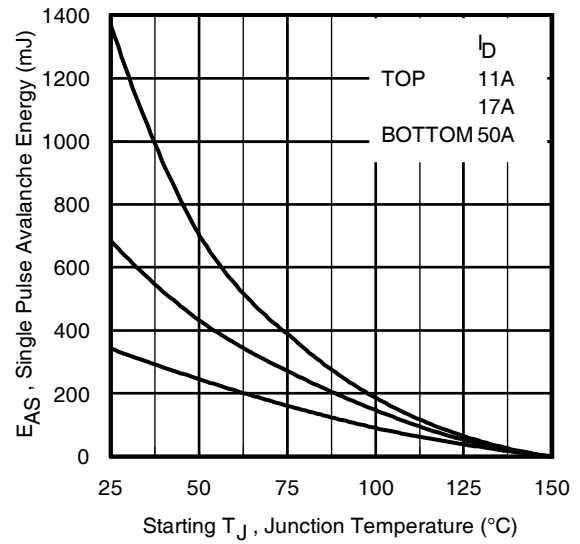


Fig 13. Maximum Avalanche Energy vs. Drain Current

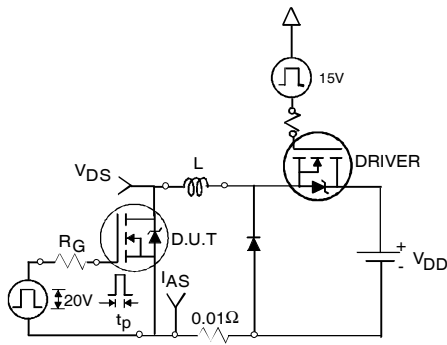


Fig 14a. Unclamped Inductive Test Circuit

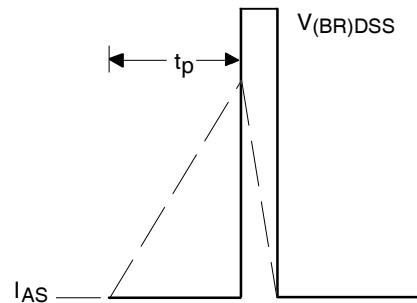


Fig 14b. Unclamped Inductive Waveforms

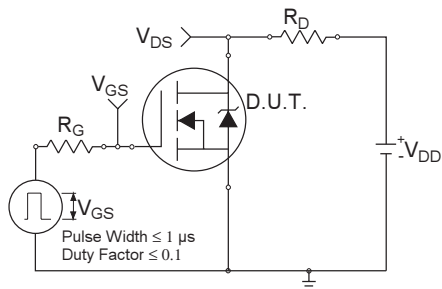


Fig 15a. Switching Time Test Circuit

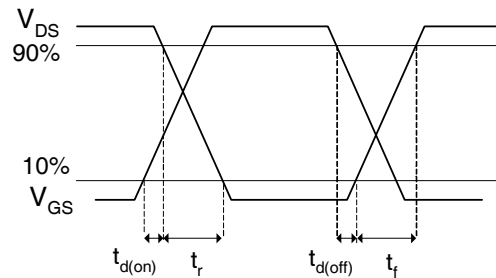


Fig 15b. Switching Time Waveforms

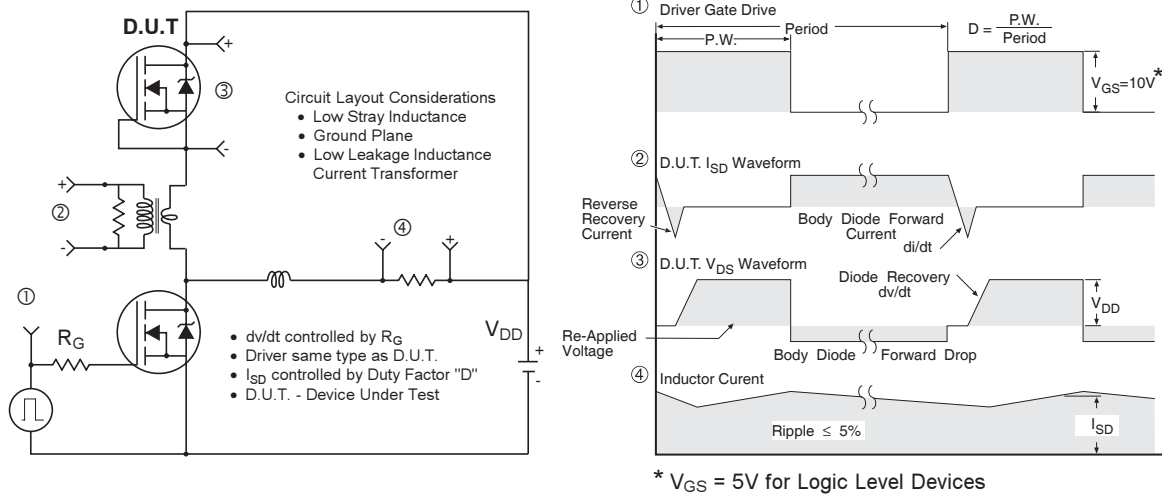


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

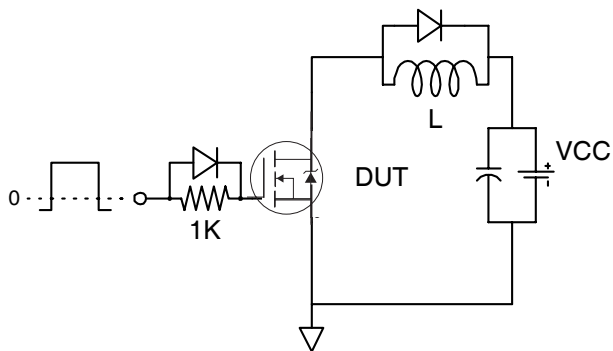


Fig 17. Gate Charge Test Circuit

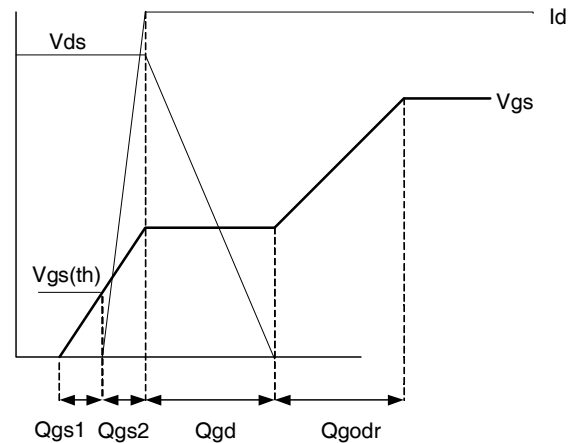
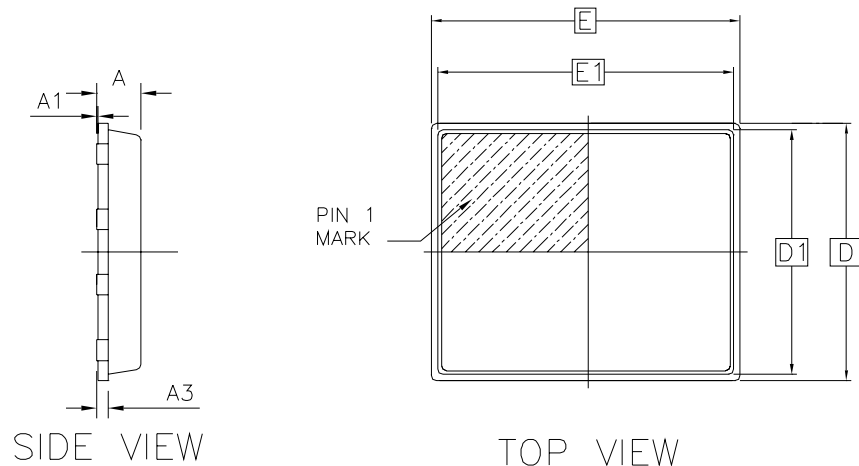
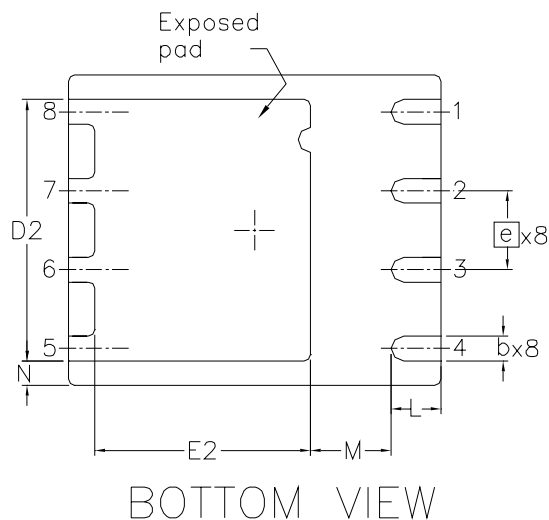


Fig 18. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details

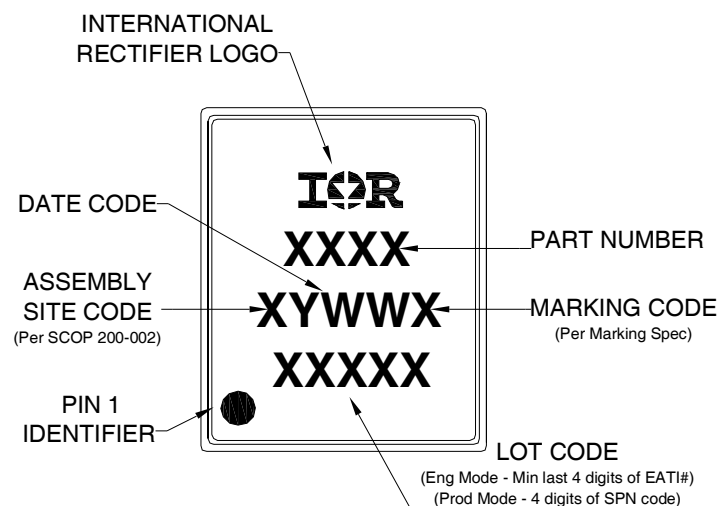


OUTLINE PQFN 5x6B				
DIM SYMBOL	MIN	NOM	MAX	
A	0.80	0.83	0.90	
A1	0	0.020	0.05	
A3		0.20	REF	
b	0.35	0.40	0.47	
D		5.00	BSC	
D1		4.75	BSC	
D2	4.10	4.21	4.30	
e		1.27	BSC	
E		6.00	BSC	
E1		5.75	BSC	
E2	3.38	3.48	3.58	
L	0.70	0.80	0.90	
M		1.30	REF	
N		0.40	REF	



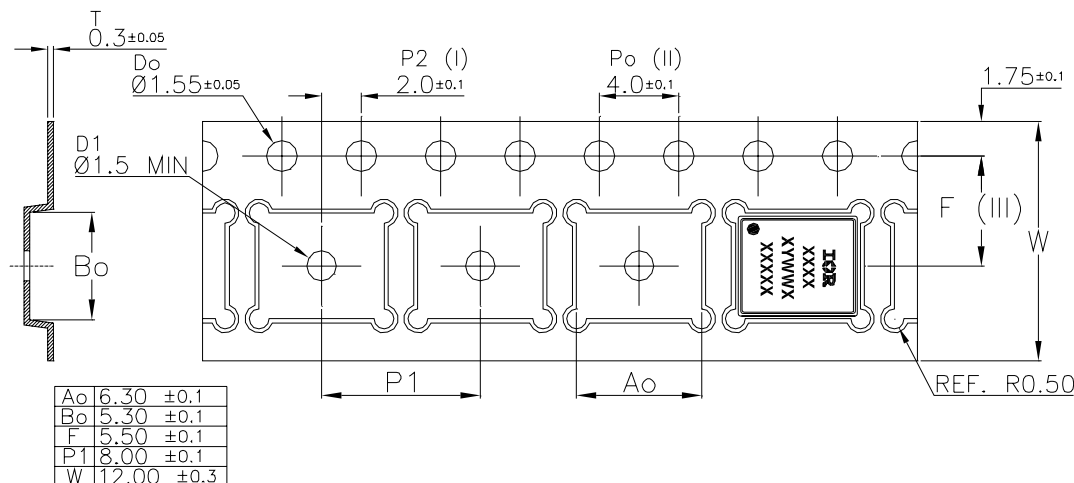
For footprint and stencil design recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/apnotes/an-1154.pdf>

PQFN 5x6 Outline "B" Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>
www.irf.com

PQFN 5x6 Outline "B" Tape and Reel



Qualification information[†]

Qualification level	Industrial ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.27\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 50\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability.

Data and specifications subject to change without notice.

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