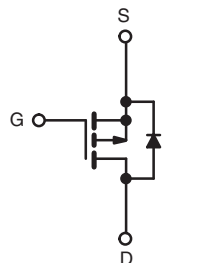
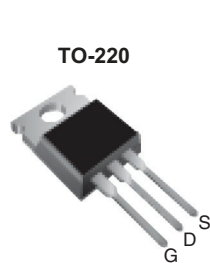


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 50	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.33
Q_g (Max.) (nC)	26	
Q_{gs} (nC)	6.2	
Q_{gd} (nC)	8.6	
Configuration	Single	



P-Channel MOSFET

FEATURES

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability
- Lead (Pb)-free Available



RoHS*
COMPLIANT

DESCRIPTION

The Power MOSFET technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel Power MOSFET's are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel Power MOSFET's such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel Power MOSFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRF9Z22PbF
	SiHF9Z22-E3
SnPb	IRF9Z22
	SiHF9Z22

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 50	V
Gate-Source Voltage	V_{GS}	± 20	
Drain-Gate Voltage ($R_{GS} = 20$ K Ω)	V_{GDR}	- 50	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	- 36	
Linear Derating Factor		0.32	W/ $^\circ\text{C}$
Inductive Current, Clamped	$L = 100$ μH	- 36	A
Unclamped Inductive Current (Avalanche Current)	I_L	- 2.2	A
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	40	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25$ V, starting $T_J = 25^\circ\text{C}$, $L = 100$ μH , $R_G = 25$ Ω
- $I_{SD} \leq -6.7$ A, $dI/dt \leq 90$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 175^\circ\text{C}$.
- 0.063" (1.6 mm) from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

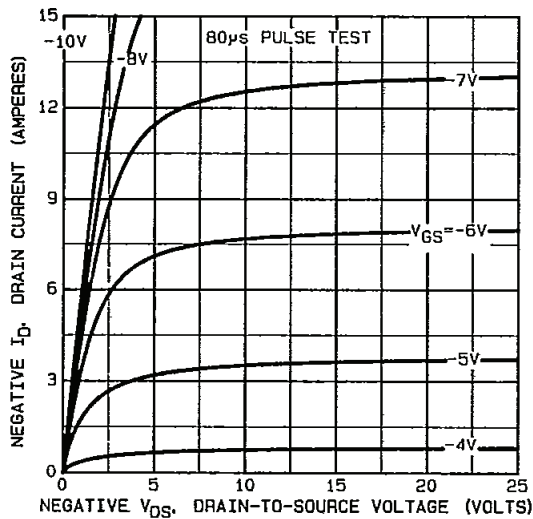
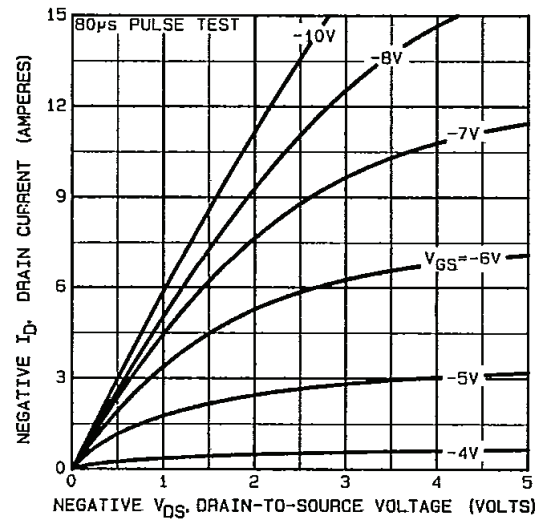
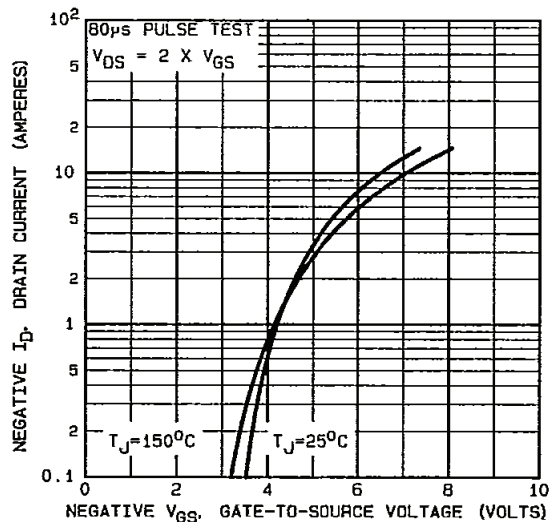
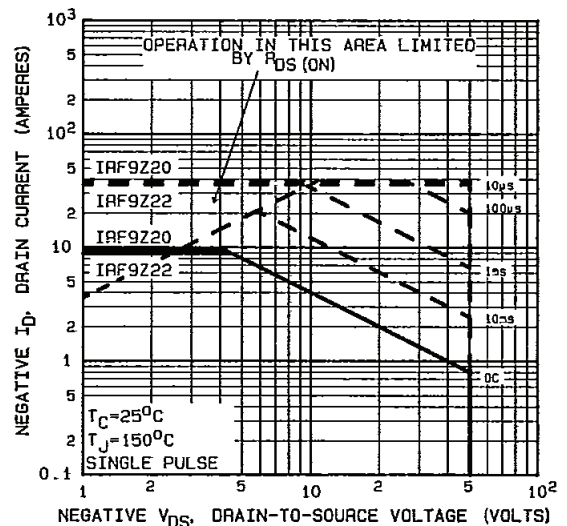
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	80	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	1.0	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 50	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = max. rating, V _{GS} = 0 V		-	-	- 250	μA
		V _{DS} = max. rating x 0.8, V _{GS} = 0 V, T _J = 125°C		-	-	- 1000	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 5.6 A ^b	-	0.28	0.33	Ω
Forward Transconductance	g _{fs}	V _{DS} = 2 x V _{GS} , I _{DS} = - 5.6 A ^b		2.3	3.5	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 9		-	480	-	pF
Output Capacitance	C _{oss}			-	320	-	
Reverse Transfer Capacitance	C _{rss}			-	58	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 9.7 A, V _{DS} = - 0.8 max. rating. see fig. 17	-	17	26	nC
Gate-Source Charge	Q _{gs}			-	4.1	6.2	
Gate-Drain Charge	Q _{gd}			-	5.7	8.6	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 25 V, I _D = - 9.7 A, R _G = 18 Ω, R _D = 2.4 Ω, see fig. 16 (MOSFET switching times are essentially independent of operating temperature)		-	8.2	12	ns
Rise Time	t _r			-	57	86	
Turn-Off Delay Time	t _{d(off)}			-	12	18	
Fall Time	t _f			-	25	38	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 9.7	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 39	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 9.7 A, V _{GS} = 0 V ^b		-	-	- 6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 9.7 A, dI/dt = 100 A/μs ^b		56	110	280	ns
Body Diode Reverse Recovery Charge	Q _{rr}			0.17	0.34	0.85	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Saturation Characteristics

Fig. 2 - Typical Transfer Characteristics

Fig. 4 - Maximum Safe Operating Area

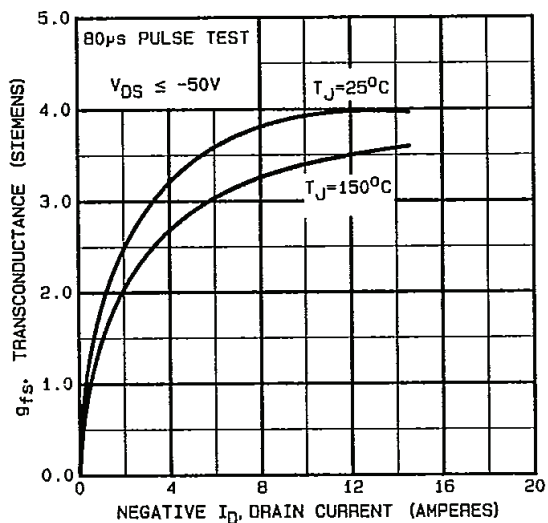


Fig. 5 - Typical Transconductance vs. Drain Current

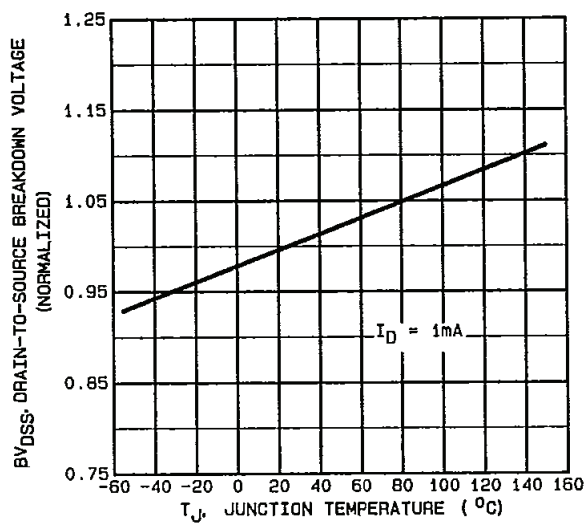


Fig. 7 - Typical Source-Drain Diode Forward Voltage

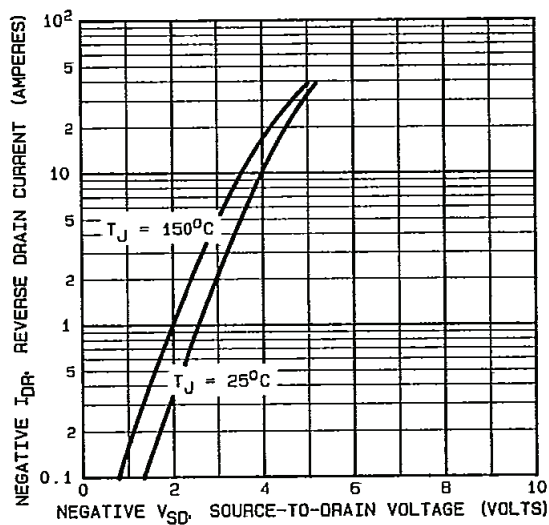


Fig. 6 - Breakdown Voltage vs. Temperature

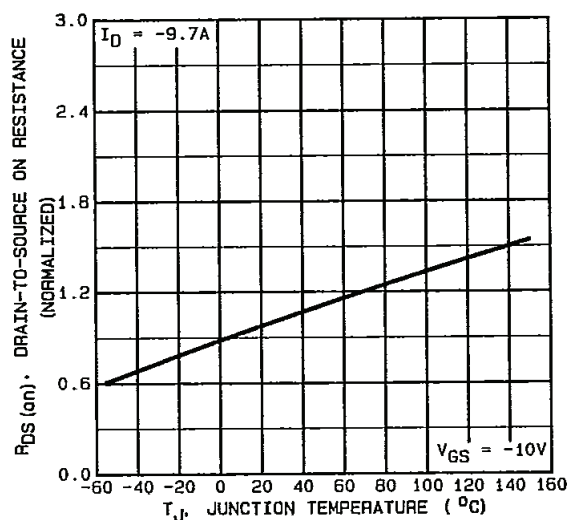


Fig. 8 - Normalized On-Resistance vs. Temperature

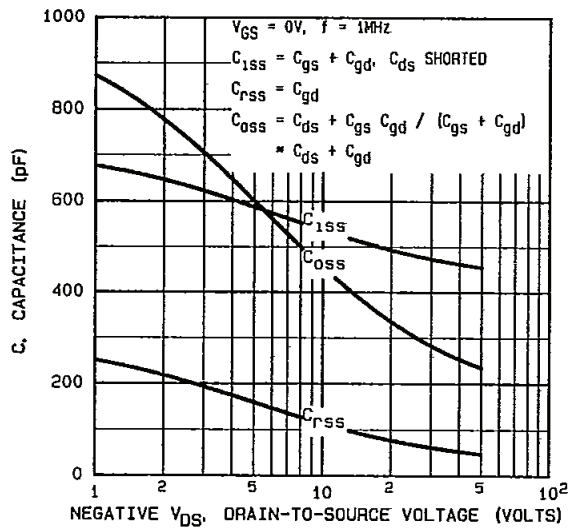


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

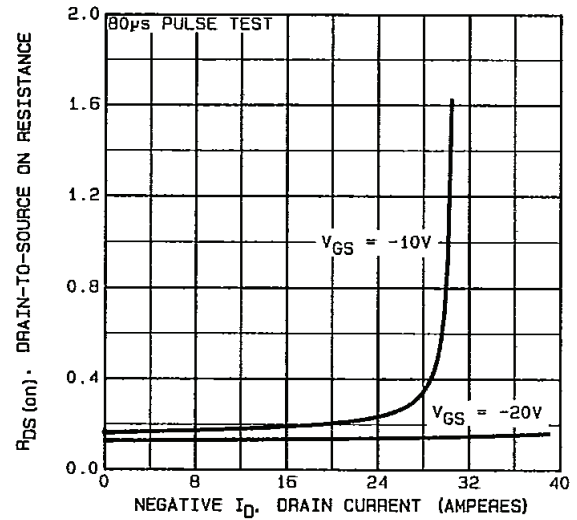


Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

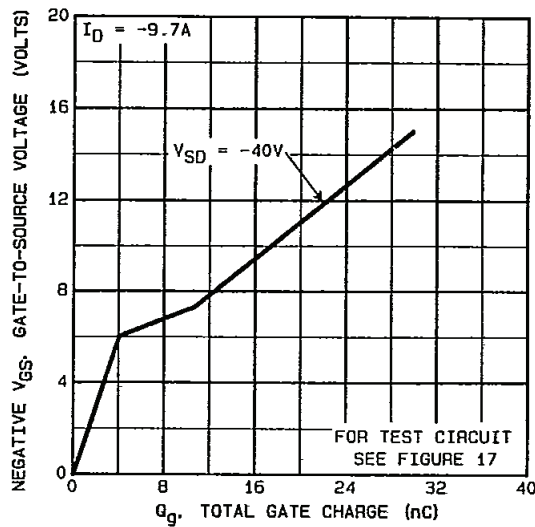


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

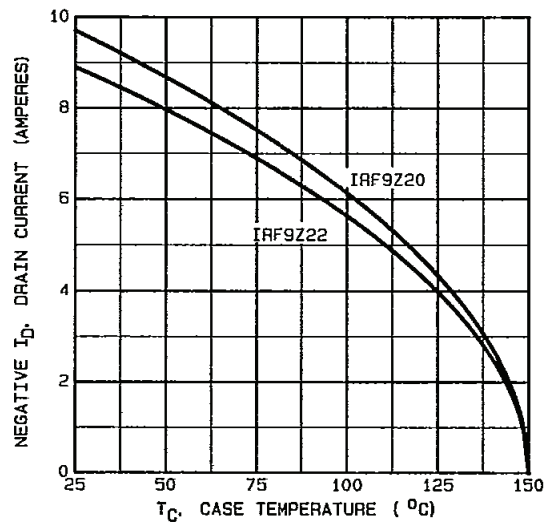


Fig. 12 - Maximum Drain Current vs. Case Temperature

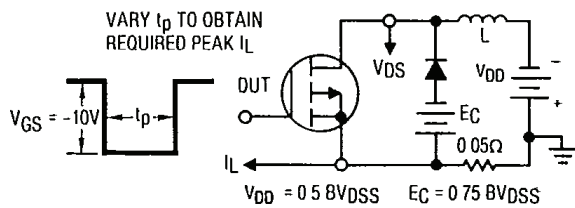


Fig. 13a - Clamped Inductive Test Circuit

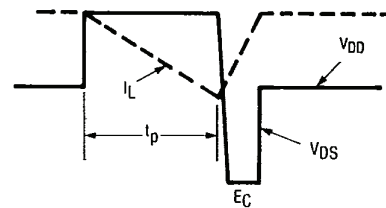


Fig. 13b - Clamped Inductive Waveforms

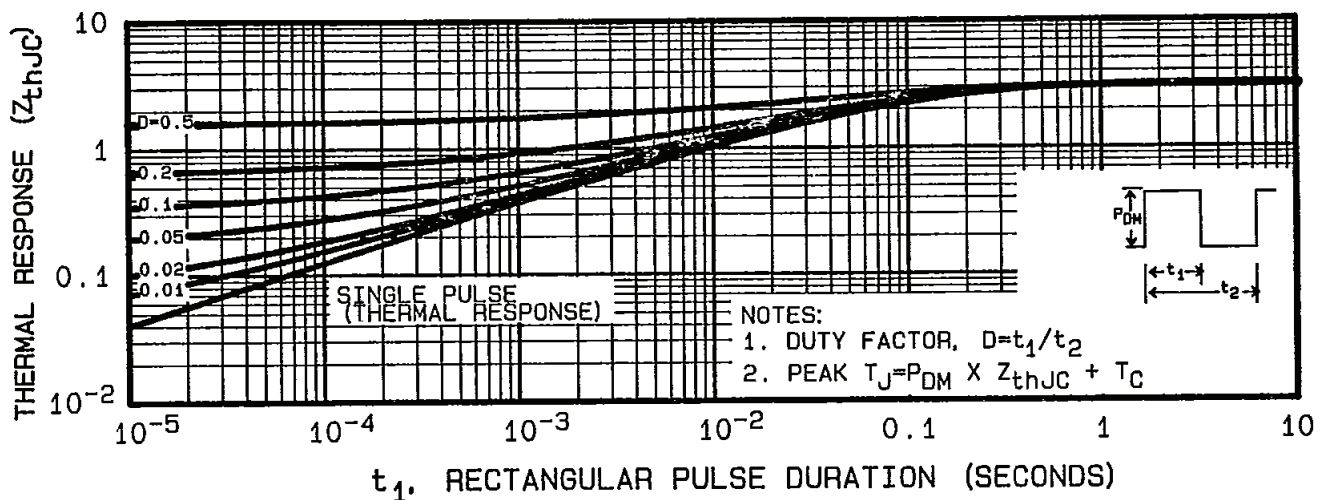


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

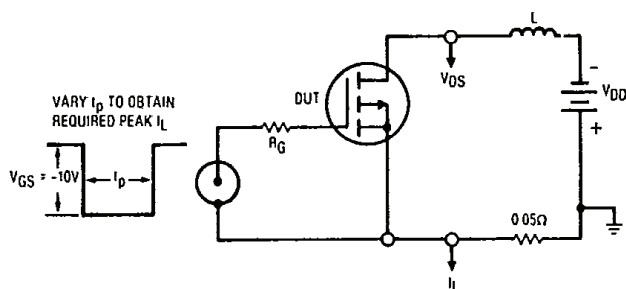


Fig. 15a - Unclamped Inductive Test Circuit

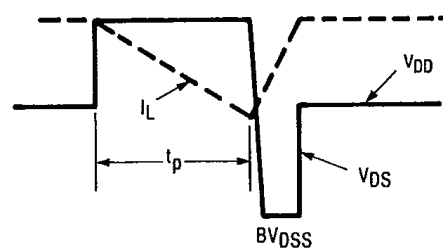
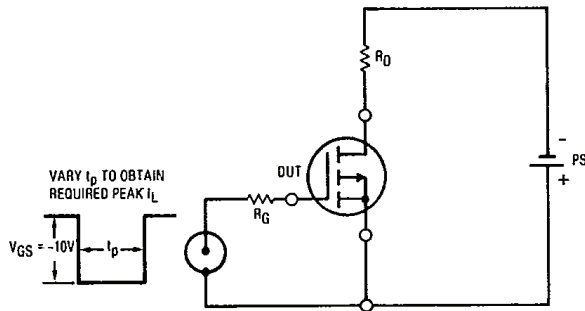
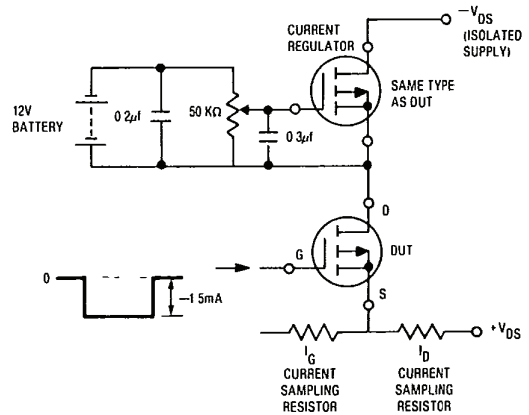
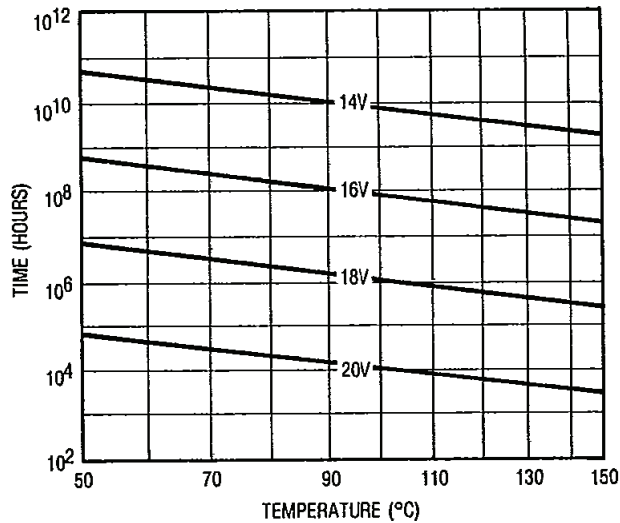
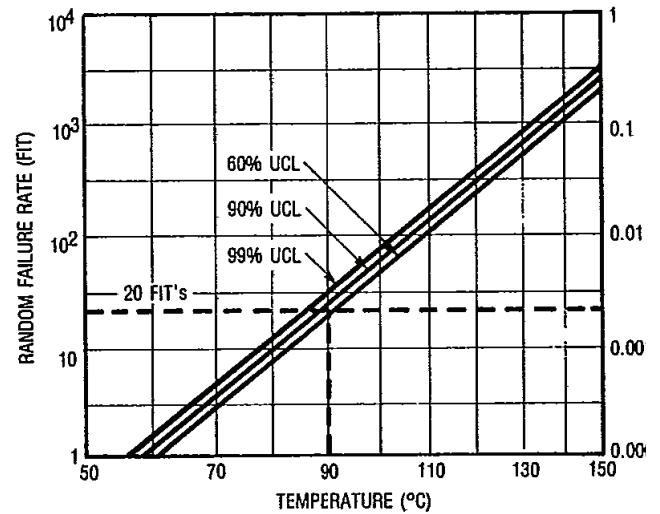


Fig. 15b - Unclamped Inductive Load Test Waveforms


Fig. 16 - Switching Time Test Circuit

Fig. 17 - Gate Charge Test Circuit

Fig. 18 - Typical Time to Accumulated 1 % Gate Failure

Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

Peak Diode Recovery dV/dt Test Circuit

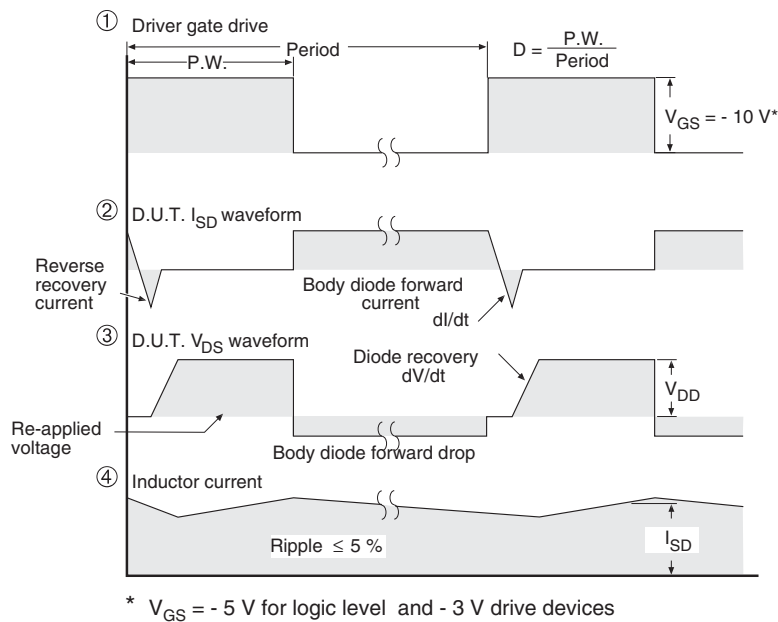
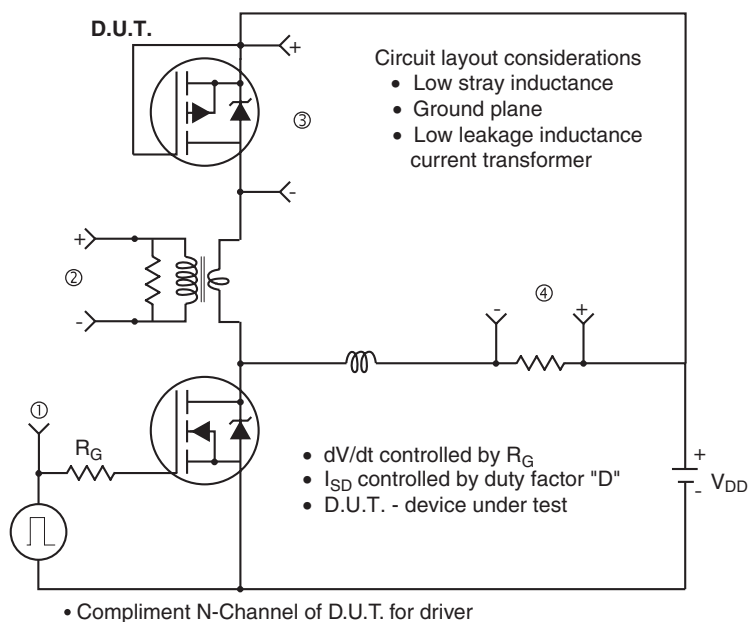


Fig. 20 - For P-Channel

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