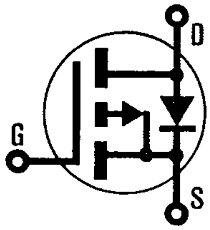
Data Sheet No. PD-9.461A



INTERNATIONAL RECTIFIER IOR

# HEXFET® TRANSISTORS IRF9Z20 IRF9Z22

## P-CHANNEL 50 VOLT POWER MOSFETs




TO-220

## -50 Volt, 0.28 Ohm, HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

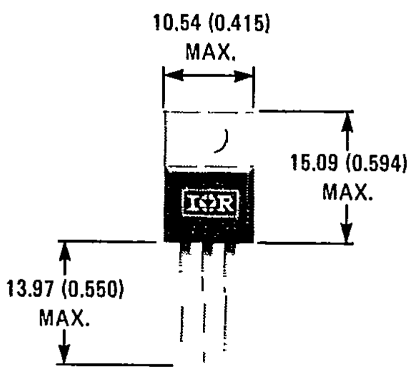
### Product Summary

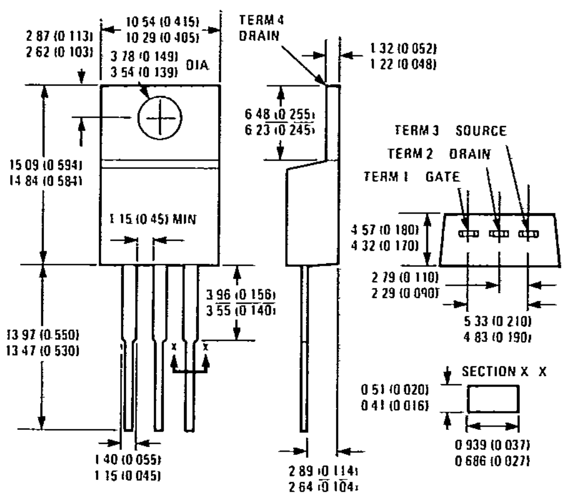
| Part Number | $V_{DS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| IRF9Z20 | -50V | 0.28Ω | -9.7A |
| IRF9Z22 | -50V | 0.33Ω | -8.9A |

### Features:

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

## CASE STYLE AND DIMENSIONS



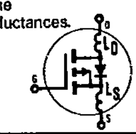

Case Style TO-220AB
Dimensions in Millimeters and (Inches)

# IRF9Z20, IRF9Z22 Devices

## Absolute Maximum Ratings

| Parameter | | IRF9Z20 | IRF9Z22 | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain - Source Voltage ① | −50 | −50 | V |
| $V_{DGR}$ | Drain - Gate Voltage ($R_{GS}$ = 20 KΩ) ① | −50 | −50 | V |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current | −9.7 | −8.9 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current | −6.1 | −5.6 | A |
| $I_{DM}$ | Pulsed Drain Current ② | −39 | −36 | A |
| $V_{GS}$ | Gate - Source Voltage | ±20 | | V |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 40 | | W |
| | Linear Derating Factor | 0.32 | | W/K ⑤ |
| $I_{LM}$ | Inductive Current, Clamped | −39 (See Fig. 14), L = 100μH | −36 | A |
| $I_L$ | Unclamped Inductive Current (Avalanche Current) ③ | (See Fig. 15) −2.2 | | A |
| $T_J$ $T_{stg}$ | Operating Junction and Storage Temperature Range | −55 to 150 | | °C |
| | Lead Temperature | 300 (0.063 in. (1.6mm) from case for 10s) | | °C |

## Electrical Characteristics @ $T_C$ = 25°C (Unless Otherwise Specified)

| Parameter | | Type | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain - Source Breakdown Voltage | IRF9Z20 IRF9Z22 | −50 | — | — | V | $V_{GS}$ = 0V, $I_D$ = −250 μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | ALL | −2.0 | — | −4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = −250 μA |
| $I_{GSS}$ | Gate-Source Leakage Forward | ALL | — | — | −500 | nA | $V_{GS}$ = −20V |
| $I_{GSS}$ | Gate-Source Leakage Reverse | ALL | — | — | 500 | nA | $V_{GS}$ = 20V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | ALL | — | — | −250 | μA | $V_{DS}$ = Max. Rating, $V_{GS}$ = 0V |
| | | | — | — | −1000 | μA | $V_{DS}$ = Max. Rating × 0.8, $V_{GS}$ = 0V, $T_C$ = 125°C |
| $I_{D(on)}$ | On-State Drain Current ④ | IRF9Z20 | −9.7 | — | — | A | $V_{DS}$ > $I_{D(on)}$ × $R_{DS(on)max.}$, $V_{GS}$ = −10V |
| | | IRF9Z22 | −8.9 | — | — | A | |
| $R_{DS(on)}$ | Static Drain-Source On-State Resistance ④ | IRF9Z20 | — | 0.20 | 0.28 | Ω | $V_{GS}$ = −10V, $I_D$ = −5.6A |
| | | IRF9Z22 | — | 0.28 | 0.33 | Ω | |
| $g_{fs}$ | Forward Transconductance ④ | ALL | 2.3 | 3.5 | — | S(℧) | $V_{DS}$ = 2 × $V_{GS}$, $I_{DS}$ = −5.6A |
| $C_{iss}$ | Input Capacitance | ALL | — | 480 | | pF | $V_{GS}$ = 0V, $V_{DS}$ = −25V, f = 1.0 MHz See Fig. 10 |
| $C_{oss}$ | Output Capacitance | ALL | — | 320 | | pF | |
| $C_{rss}$ | Reverse Transfer Capacitance | ALL | — | 58 | | pF | |
| $t_{d(on)}$ | Turn-On Delay Time | ALL | — | 8.2 | 12 | ns | $V_{DD}$ = −25V, $I_D$ ≈ −9.7A, $R_G$ = 18Ω, $R_D$ = 2.4Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.) |
| $t_r$ | Rise Time | ALL | — | 57 | 86 | ns | |
| $t_{d(off)}$ | Turn-Off Delay Time | ALL | — | 12 | 18 | ns | |
| $t_f$ | Fall Time | ALL | — | 25 | 38 | ns | |
| $Q_g$ | Total Gate Charge (Gate-Source Plus Gate-Drain) | ALL | — | 17 | 26 | nC | $V_{GS}$ = −10V, $I_D$ = −9.7A, $V_{DS}$ = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.) |
| $Q_{gs}$ | Gate-Source Charge | ALL | — | 4.1 | 6.2 | nC | |
| $Q_{gd}$ | Gate-Drain ("Miller") Charge | ALL | — | 5.7 | 8.6 | nC | |
| $L_D$ | Internal Drain Inductance | ALL | — | 4.5 | — | nH | Measured from the drain lead, 6mm (0.25 in.) from package to center of die. / Modified MOSFET symbol showing the internal device inductances.  |
| $L_S$ | Internal Source Inductance | ALL | — | 7.5 | — | nH | Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad. |

## Thermal Resistance

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction-to-Case | ALL | — | — | 3.1 | K/W⑤ | |
| $R_{thCS}$ | Case-to-Sink | ALL | — | 1.0 | — | K/W⑤ | Mounting surface flat, smooth, and greased. |
| $R_{thJA}$ | Junction-to-Ambient | ALL | — | — | 80 | K/W⑤ | Typical socket mount |

## Source-Drain Diode Ratings and Characteristics

| Symbol | Parameter | Type | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | IRF9Z20 | — | — | −9.7 | A | Modified MOSFET symbol showing the integral reverse P-N junction rectifier.  |
| | | IRF9Z20 | — | — | −8.9 | A | |
| $I_{SM}$ | Pulse Source Current (Body Diode) ③ | IRF9Z22 | — | — | −39 | A | |
| | | IRF9Z22 | — | — | −36 | A | |
| $V_{SD}$ | Diode Forward Voltage ② | ALL | — | — | −6.3 | V | $T_C$ = 25°C, $I_S$ = −9.7A, $V_{GS}$ = 0V |
| $t_{rr}$ | Reverse Recovery Time | ALL | 56 | 110 | 280 | ns | $T_J$ = 25°C, $I_F$ = −9.7A, $dI_F/dt$ = 100A/μs |
| $Q_{RR}$ | Reverse Recovered Charge | ALL | 0.17 | 0.34 | 0.85 | μC | $T_J$ = 25°C, $I_F$ = −9.7A, $dI_F/dt$ = 100A/μs |
| $t_{on}$ | Forward Turn-on Time | ALL | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$. | | | | |

①$T_J$ = 25°C to 150°C
⑤K/W = °C/W
W/K = W/°C

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ @ $V_{dd}$ = −25V, $T_j$ = 25°C
L = 100 μH, $R_G$ = 25Ω

④ Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%

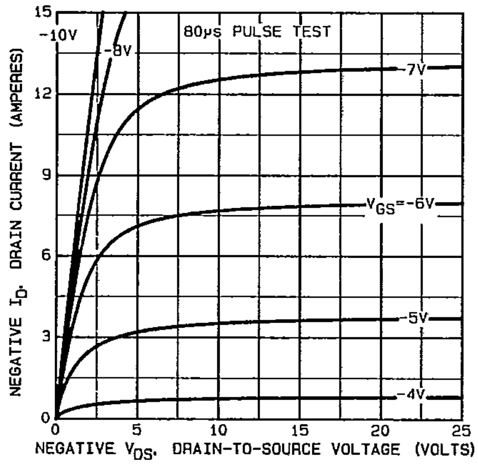



**Fig. 1 — Typical Output Characteristics**

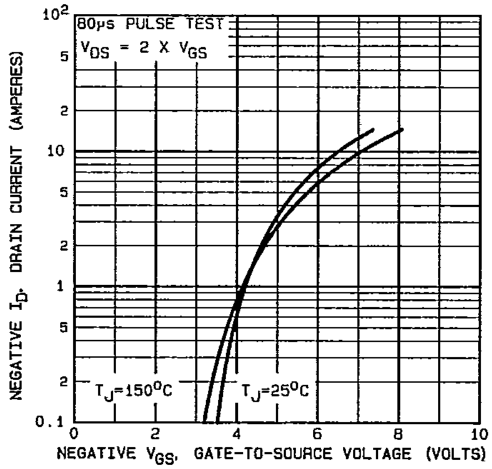



**Fig. 2 — Typical Transfer Characteristics**

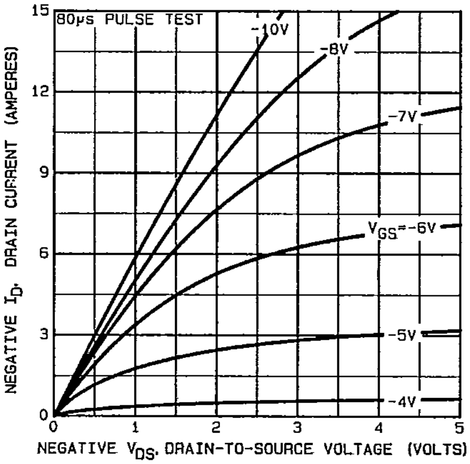



**Fig. 3 — Typical Saturation Characteristics**

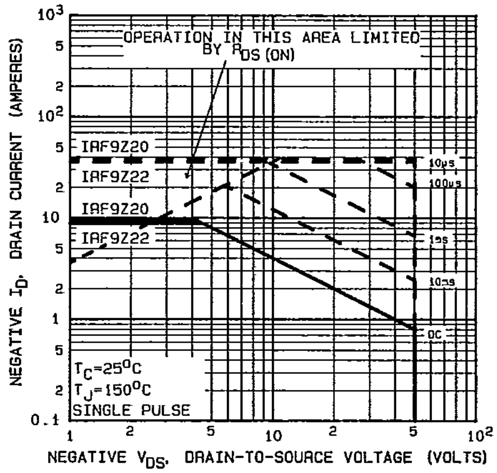



**Fig. 4 — Maximum Safe Operating Area**

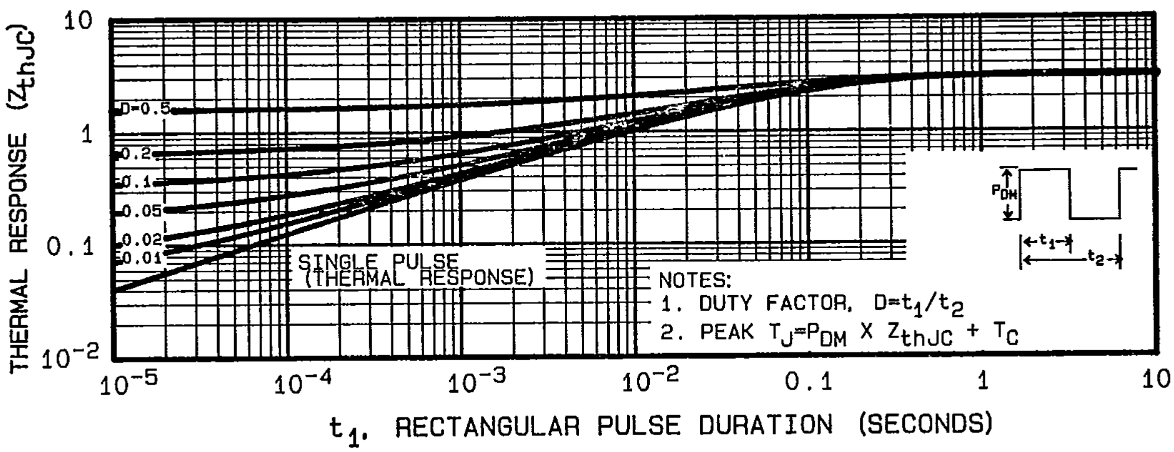



**Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration**

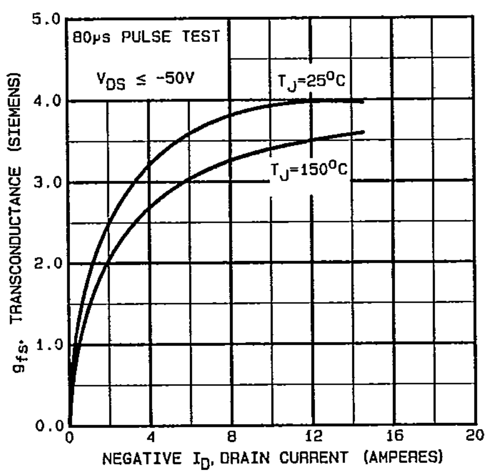



**Fig. 6 — Typical Transconductance Vs. Drain Current**

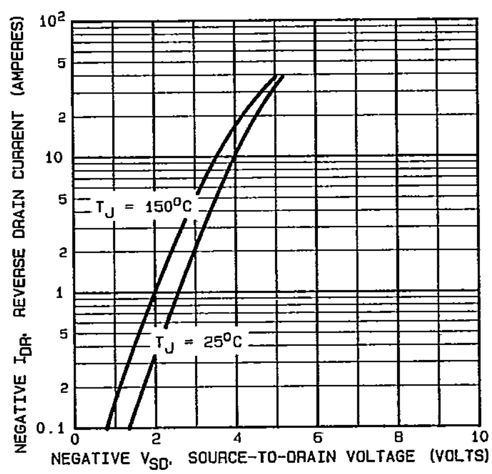



**Fig. 7 — Typical Source-Drain Diode Forward Voltage**

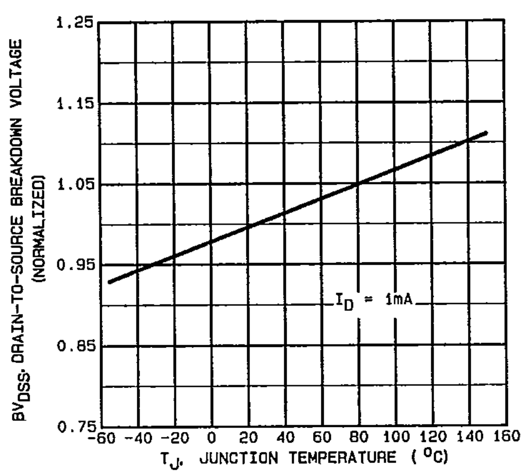



**Fig. 8 — Breakdown Voltage Vs. Temperature**

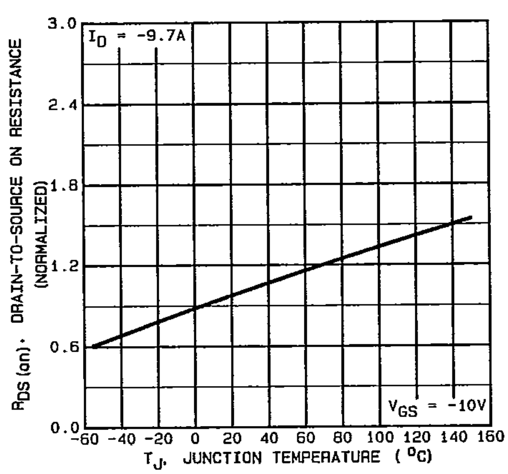



**Fig. 9 — Normalized On-Resistance Vs. Temperature**

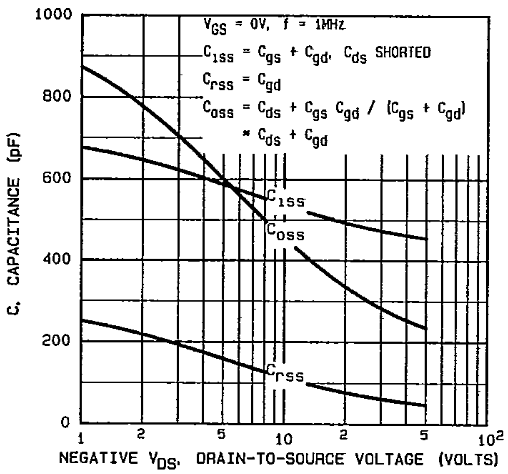



**Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage**

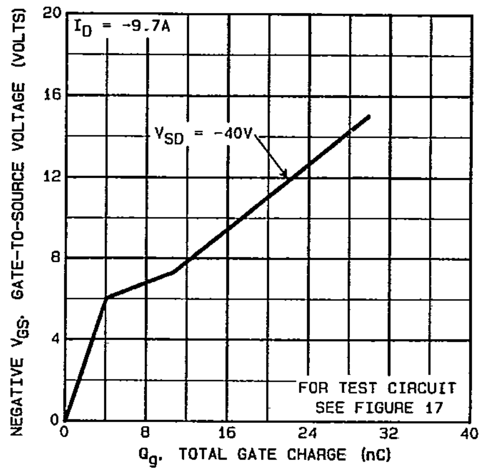



**Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage**

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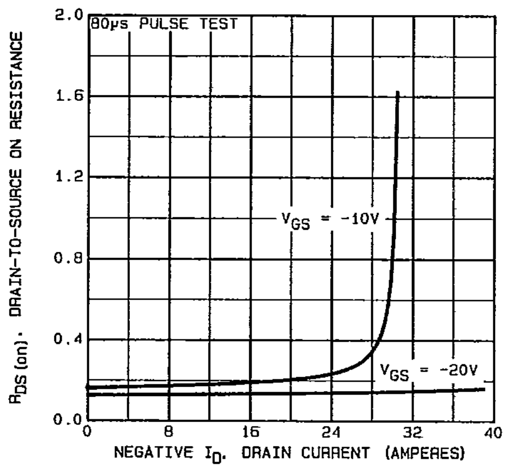


**Fig. 12 — Typical On-Resistance Vs. Drain Current**

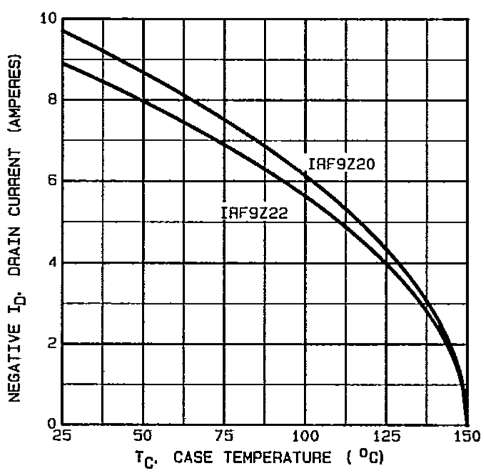


**Fig. 13 — Maximum Drain Current Vs. Case Temperature**

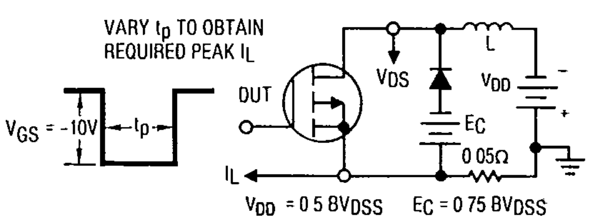


**Fig. 14a — Clamped Inductive Test Circuit**

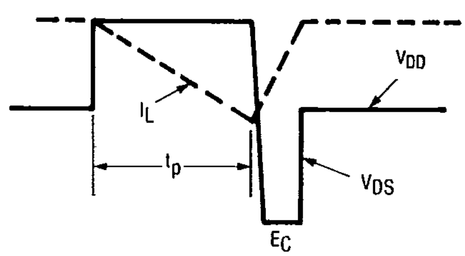


**Fig. 14b — Clamped Inductive Waveforms**

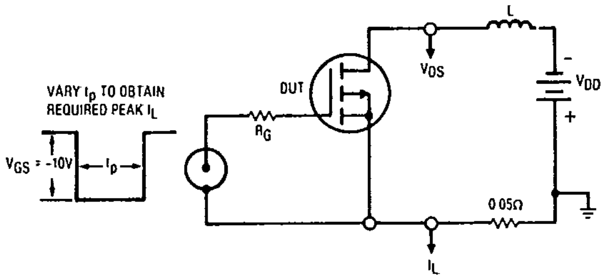


**Fig. 15a — Unclamped Inductive Test Circuit**

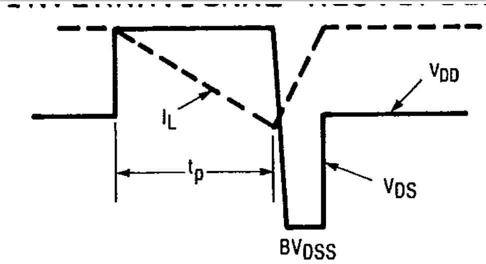


**Fig. 15b — Unclamped Inductive Load Test Waveforms**

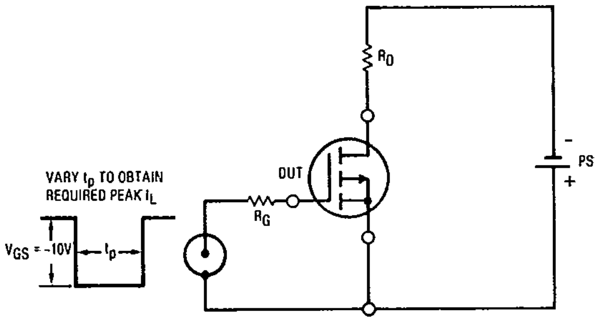


**Fig. 16 — Switching Time Test Circuit**

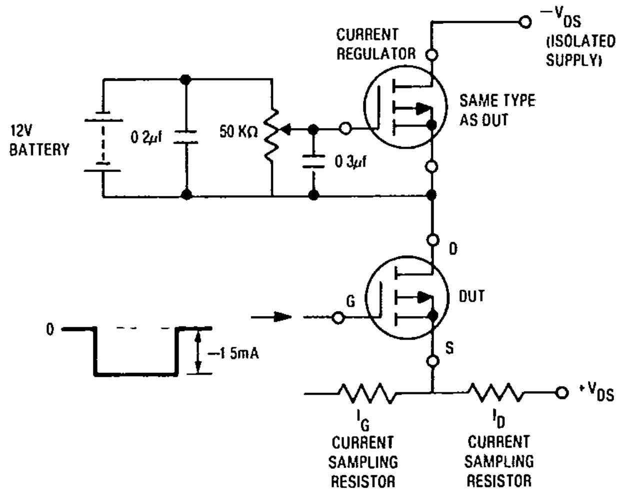


**Fig. 17 — Gate Charge Test Circuit**

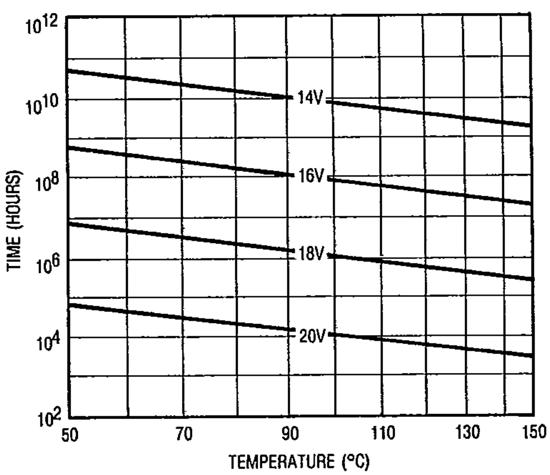


***Fig. 18 — Typical Time to Accumulated 1% Gate Failure**

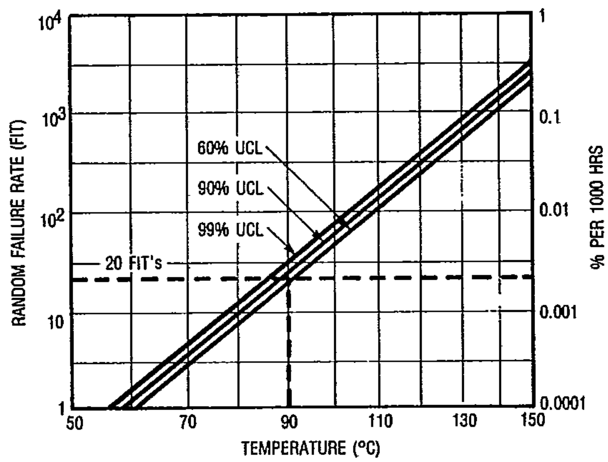


***Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate**

*The data shown in correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.