

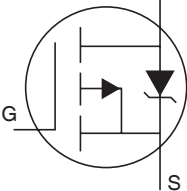
IRF9540NSPbF IRF9540NLPbF

HEXFET® Power MOSFET

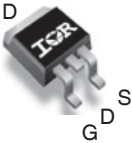
- Advanced Process Technology
- Ultra Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Some Parameters are Different from IRF9540NS/L
- P-Channel
- Lead-Free

Description

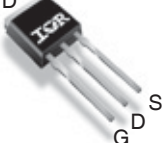
Features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of other applications.



$V_{DSS} = -100V$
 $R_{DS(on)} = 117m\Omega$
 $I_D = -23A$



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IRF9540NSPbF



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IRF9540NLPbF

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ -10V	-23	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ -10V	-14	
I_{DM}	Pulsed Drain Current ①	-92	
P_D @ $T_A = 25^\circ C$	Maximum Power Dissipation	3.1	W
P_D @ $T_C = 25^\circ C$	Maximum Power Dissipation	110	
	Linear Derating Factor	0.9	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	84	mJ
I_{AR}	Avalanche Current ①	-14	A
E_{AR}	Repetitive Avalanche Energy ①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-13	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑤	—	40	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0\text{V}$, $I_D = -250\mu\text{A}$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	117	m Ω	$V_{GS} = -10\text{V}$, $I_D = -14\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$
g_{fs}	Forward Transconductance	5.6	—	—	S	$V_{DS} = -50\text{V}$, $I_D = -14\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-50	μA	$V_{DS} = -100\text{V}$, $V_{GS} = 0\text{V}$
		—	—	-250		$V_{DS} = -80\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = -20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = 20\text{V}$
Q_g	Total Gate Charge	—	73	110	nC	$I_D = -14\text{A}$
Q_{gs}	Gate-to-Source Charge	—	13	20		$V_{DS} = -80\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	38	57		$V_{GS} = -10\text{V}$ ④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = -50\text{V}$
t_r	Rise Time	—	64	—		$I_D = -14\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	40	—		$R_G = 5.1\Omega$
t_f	Fall Time	—	45	—		$V_{GS} = -10\text{V}$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1450	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	430	—		$V_{DS} = -25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	230	—		$f = 1.0\text{MHz}$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-23	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-92		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	$T_J = 25^\circ\text{C}$, $I_S = -14\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	140	210	ns	$T_J = 25^\circ\text{C}$, $I_F = -14\text{A}$, $V_{DD} = -25\text{V}$
Q_{rr}	Reverse Recovery Charge	—	890	1340	nC	$di/dt = -100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

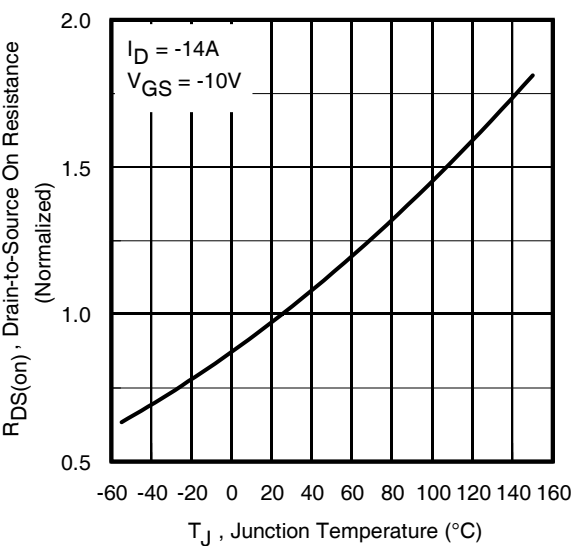
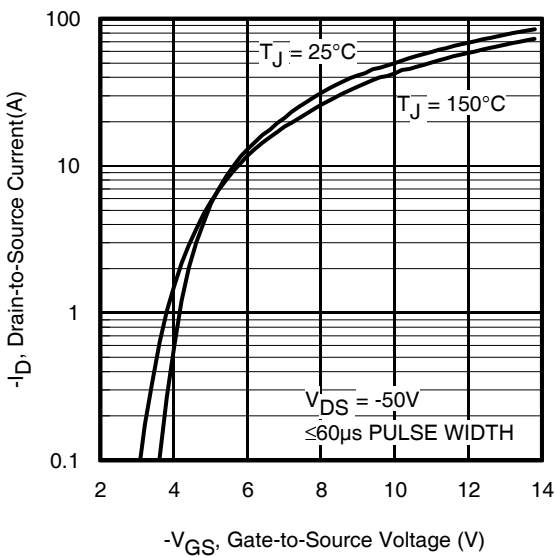
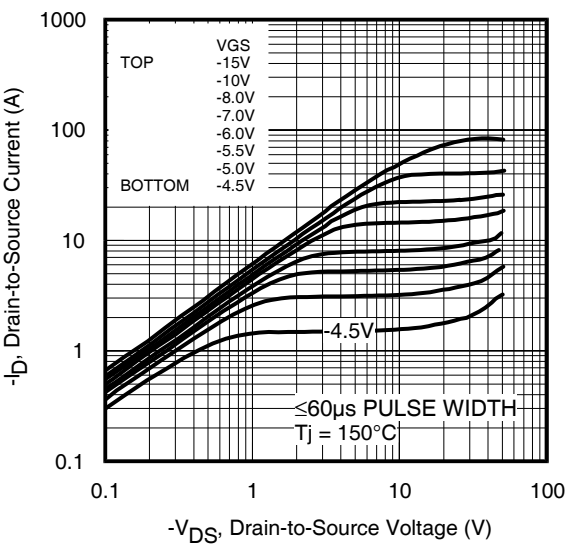
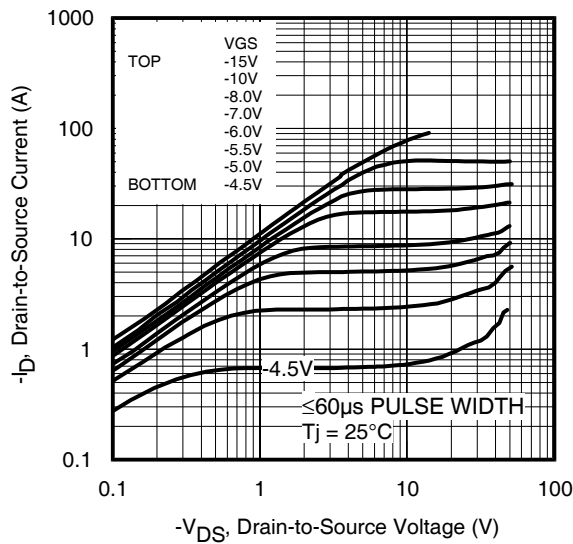
Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.88\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = -14\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq -14\text{A}$, $di/dt \leq -620\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$.

④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

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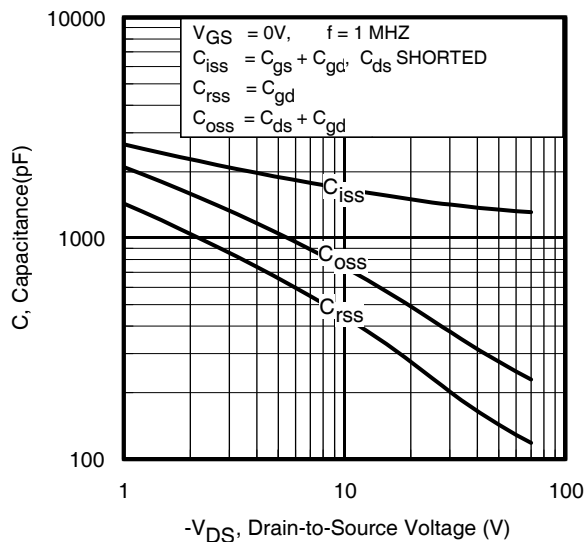


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

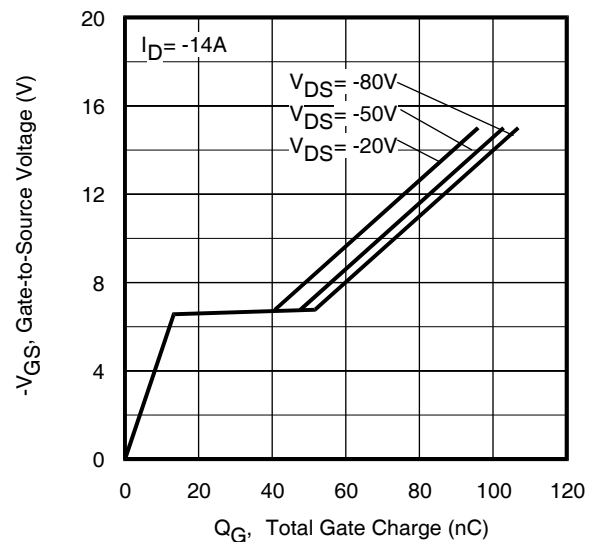


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

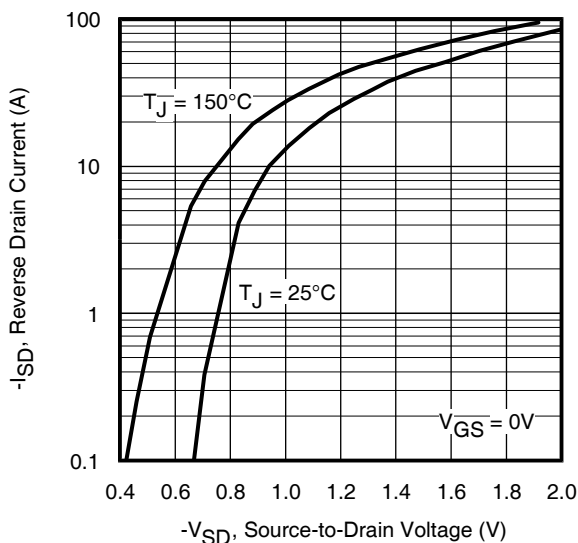


Fig 7. Typical Source-Drain Diode Forward Voltage

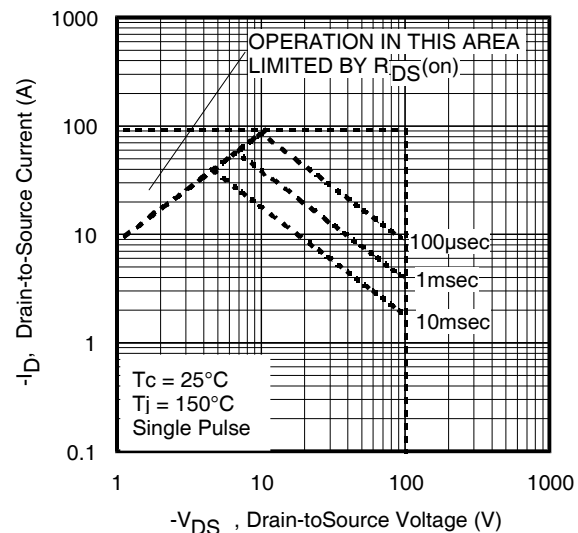


Fig 8. Maximum Safe Operating Area

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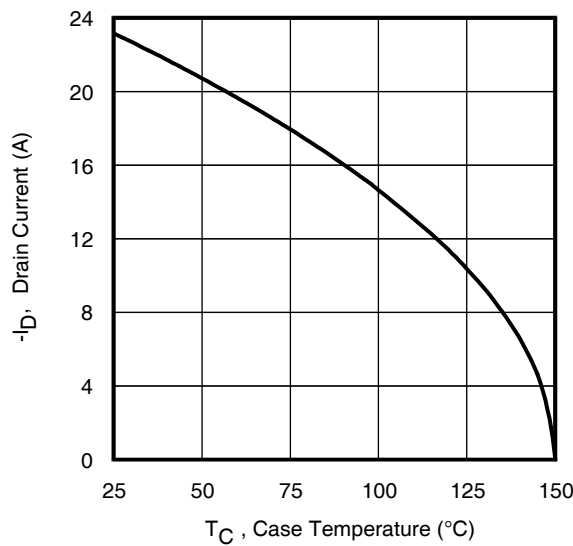


Fig 9. Maximum Drain Current vs. Case Temperature

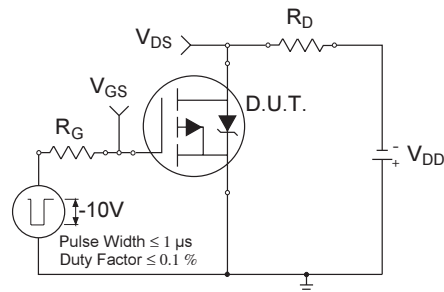


Fig 10a. Switching Time Test Circuit

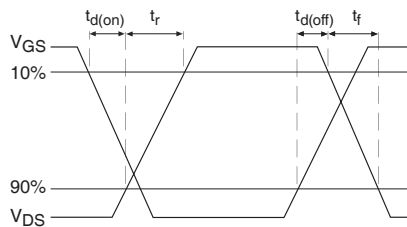


Fig 10b. Switching Time Waveforms

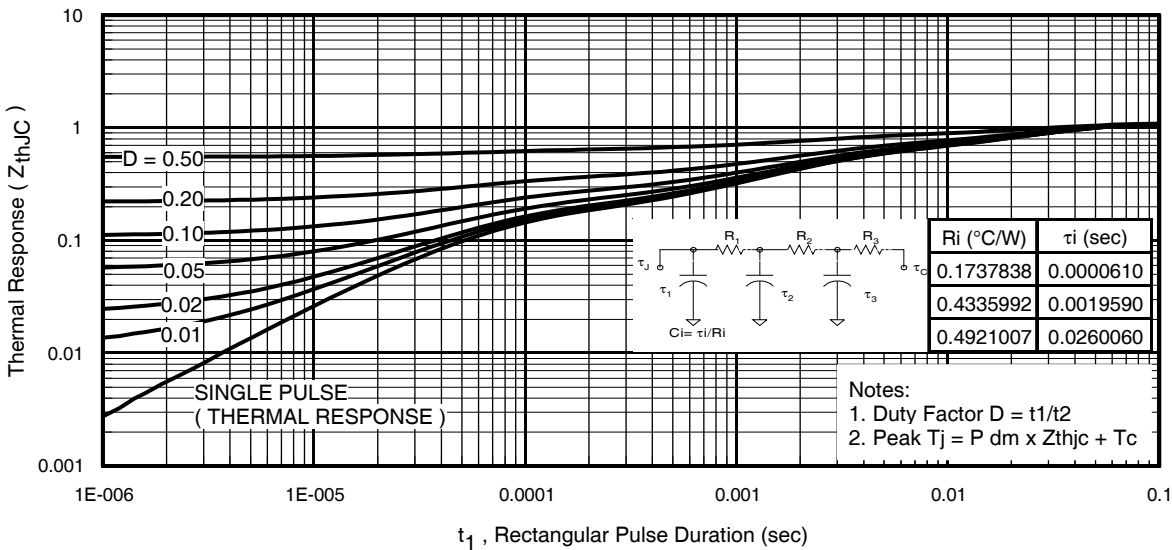


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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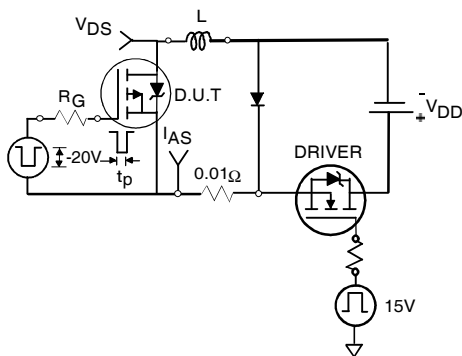


Fig 12a. Unclamped Inductive Test Circuit

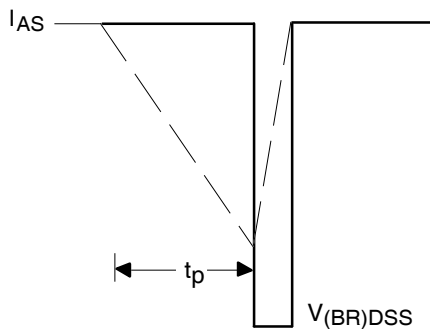


Fig 12b. Unclamped Inductive Waveforms

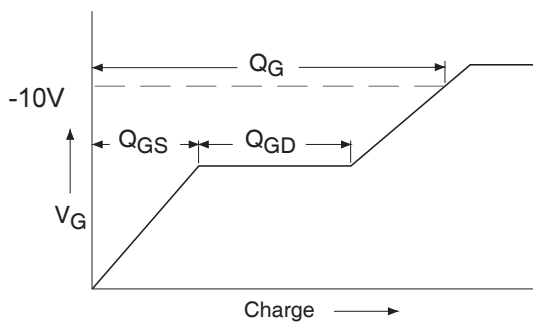


Fig 14a. Basic Gate Charge Waveform

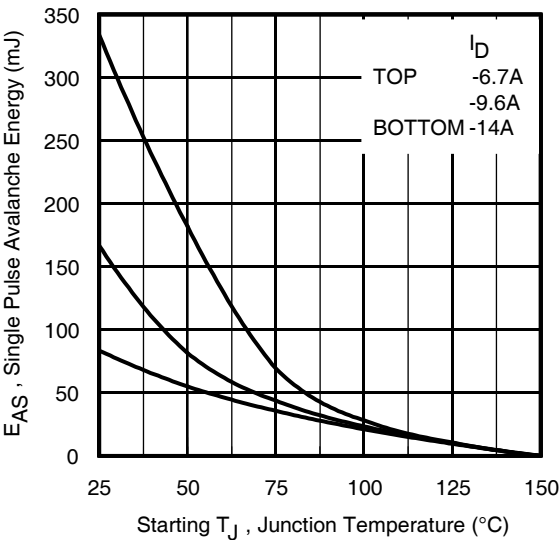


Fig 13. Maximum Avalanche Energy vs. Drain Current

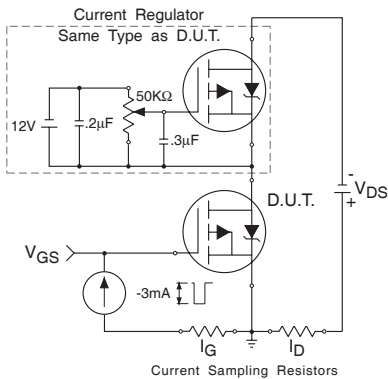
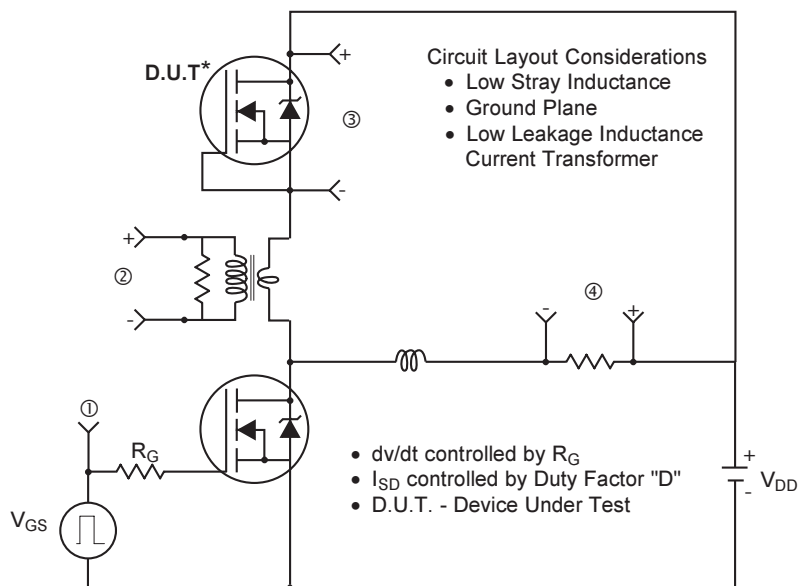


Fig 14b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

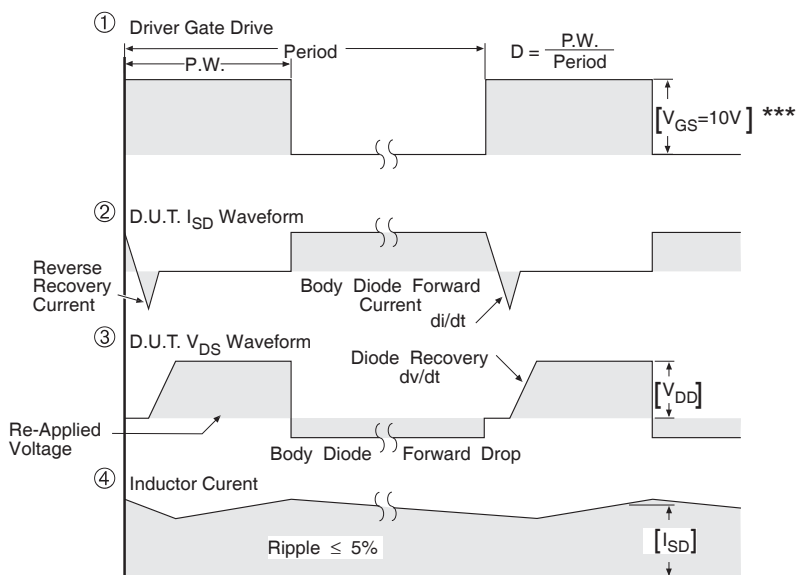
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

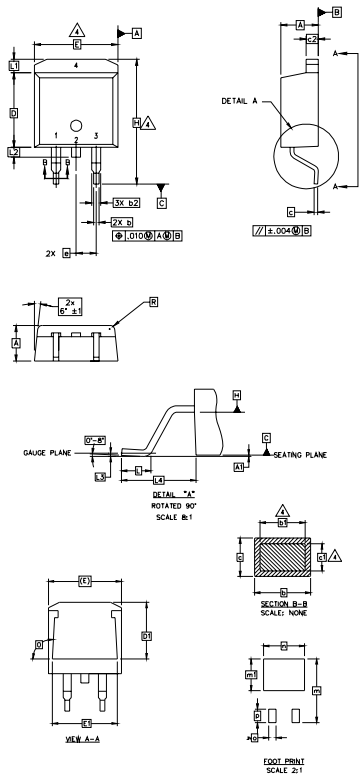
Fig 15. For P-Channel HEXFETS

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)

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- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	0.00	0.254	.000	.010	
b	0.51	0.89	.020	.035	
b1	1.14	1.78	.045	.070	
c	0.38	0.74	.015	.029	4
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.51	9.65	.335	.380	
D1	6.86		.270		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

DIODES

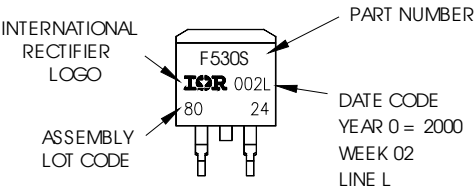
- 1.- ANODE *
- 2, 4.- CATHODE
- 3.- ANODE

* PART DEPENDENT.

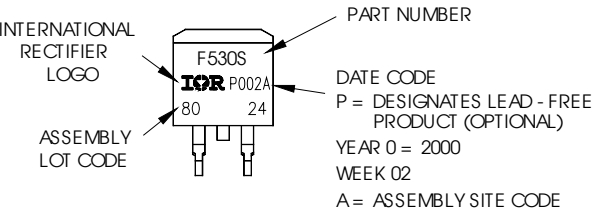
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON VV02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead - Free"



OR

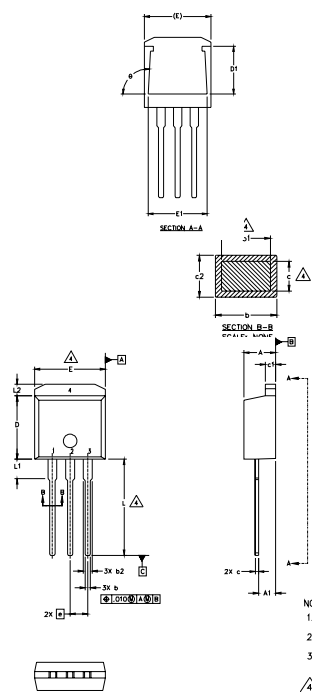


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TO-262 Package Outline

Dimensions are shown in millimeters (inches)

IRF9540NS/LPbF



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

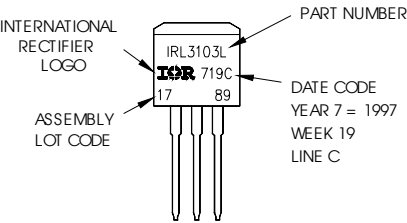
HEXFET	IGBT
1.- GATE	1 - GATE
2.- DRAIN	2 - COLLECTOR
3.- SOURCE	3 - EMITTER
4.- DRAIN	

- NOTES:
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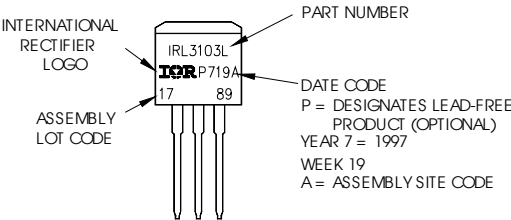
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line
position indicates "Lead-Free"



OR

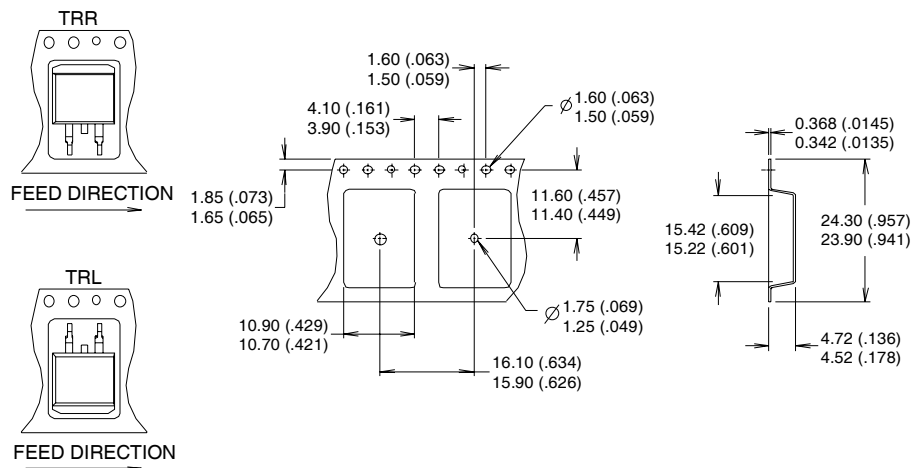


IRF9540NS/LPbF

D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)

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- NOTES :
1. COMFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 09/05

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>