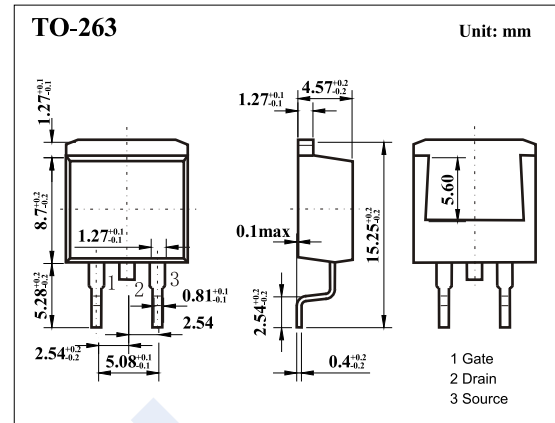
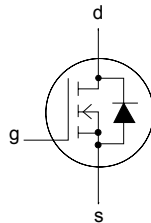


N-Channel MOSFET

IRF840S (KRF840S)

■ Features

- $V_{DS} (V) \approx 500V$
- $I_D = 8 A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 0.85 \Omega$ ($V_{GS} = 10V$)
- Fast switching
- Low thermal resistance



■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_a = 25^\circ C$	I_D	8	A
	$T_a = 100^\circ C$		5.1	
Pulsed Drain Current		I_{DM}	32	
Avalanche Current		I_{AR}	8	W
Power Dissipation	$T_c = 25^\circ C$	P_D	125	
	$T_a = 25^\circ C$		3.1	
Non-Repetitive Avalanche Energy (Note.1)		E_{AS}	510	mJ
Repetitive Avalanche Energy		E_{AR}	13	
Peak Diode Recovery dv/dt (Note.2)		dv/dt	3.5	V/ns
Thermal Resistance Junction- to-Ambient		R_{thJA}	60	$^\circ C/W$
Thermal Resistance Junction to Mounting Base		R_{thJB}	0.85	
Junction Temperature		T_J	150	$^\circ C$
Storage Temperature Range		T_{stg}	-55 to 150	

Note.1: $L = 14mH$, $I_{AS} = 8A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ C$.

Note.2: $I_{SD} \leq 8 A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, Starting $T_J \leq 25^\circ C$.

N-Channel MOSFET

IRF840S (KRF840S)

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =250 μA, V _{GS} =0V	500			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =500V, V _{GS} =0V			25	μA
		V _{DS} =400V, V _{GS} =0V, T _J =125°C			250	
Gate-Body Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250 μA	2		4	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =4.8A (Note.1)			0.85	Ω
Forward Transconductance	g _{FS}	V _{DS} =50V, I _D =4.8A (Note.1)	4.9			S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1MHz		1300		pF
Output Capacitance	C _{oss}			310		
Reverse Transfer Capacitance	C _{rss}			120		
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =400V, I _D =8A			63	nC
Gate Source Charge	Q _{gs}				9.3	
Gate Drain Charge	Q _{gd}				32	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25in.) from package and center of die contact		4.5		nH
Internal Source Inductance	L _S			7.5		
Turn-On DelayTime	t _{d(on)}	V _{DD} = 250 V, I _D = 8 A, R _g = 9.1Ω, R _D = 31Ω (Note.1)		14		ns
Turn-On Rise Time	t _r			23		
Turn-Off DelayTime	t _{d(off)}			49		
Turn-Off Fall Time	t _f			20		
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 8A, dI/dt = 100A/μs			970	μs
Body Diode Reverse Recovery Charge	Q _{rr}				8.9	
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p-n junction diode.			8	A
Pulsed Diode Forward Current	I _{SM}				32	
Diode Forward Voltage	V _{SD}	I _S =8A, V _{GS} =0V, T _J = 25°C			2	V

Note.1: Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

N-Channel MOSFET

IRF840S (KRF840S)

■ Typical Characteristics

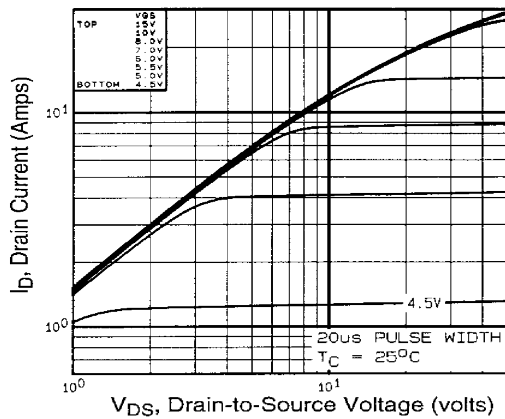


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

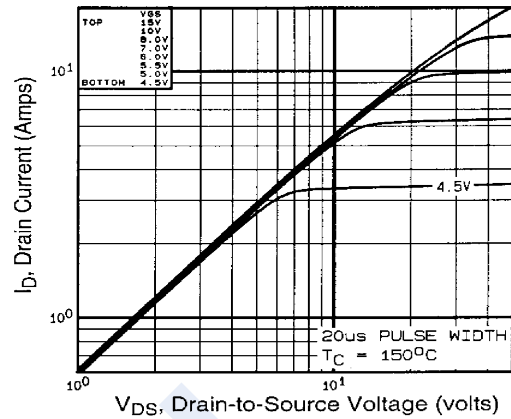


Fig 2. Typical Output Characteristics,
 $T_C=150^\circ\text{C}$

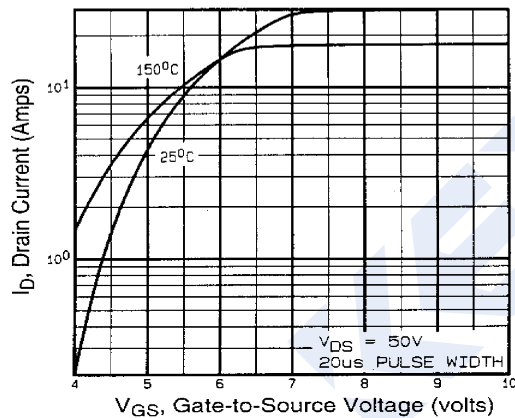


Fig 3. Typical Transfer Characteristics

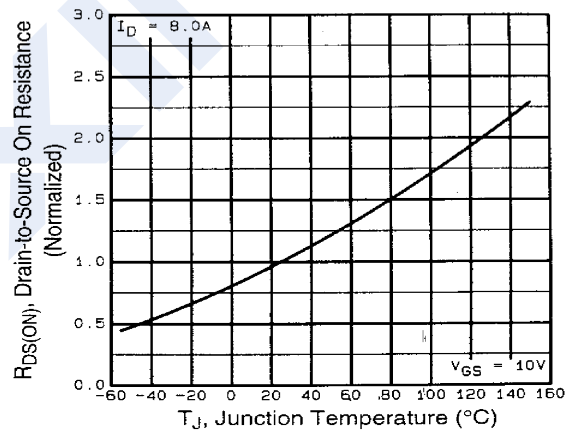


Fig 4. Normalized On-Resistance
Vs. Temperature

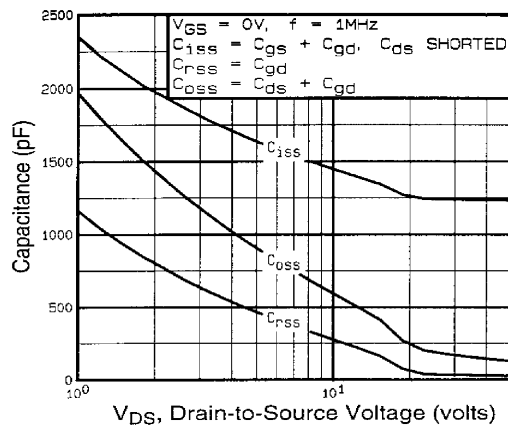


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

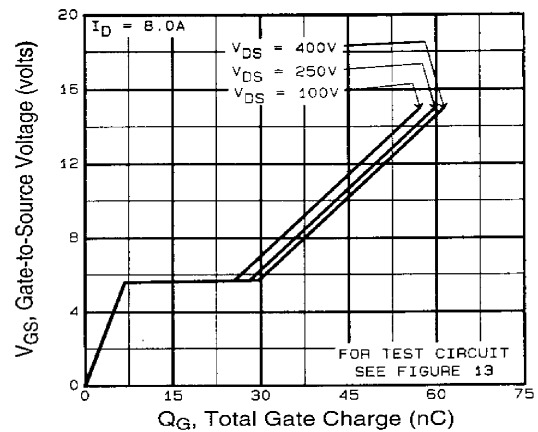


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

N-Channel MOSFET

IRF840S (KRF840S)

■ Typical Characteristics

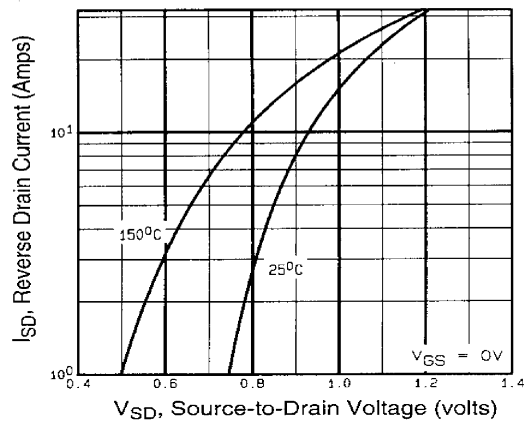


Fig 7. Typical Source-Drain Diode Forward Voltage

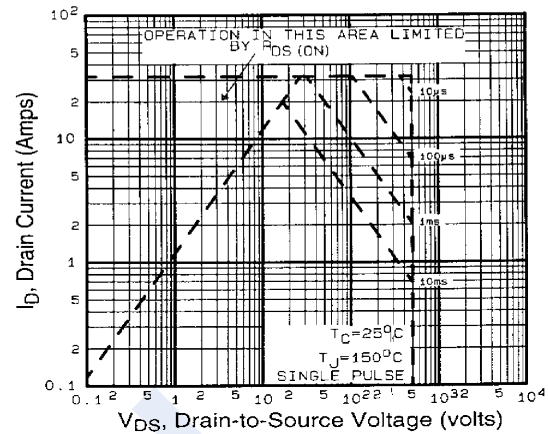


Fig 8. Maximum Safe Operating Area

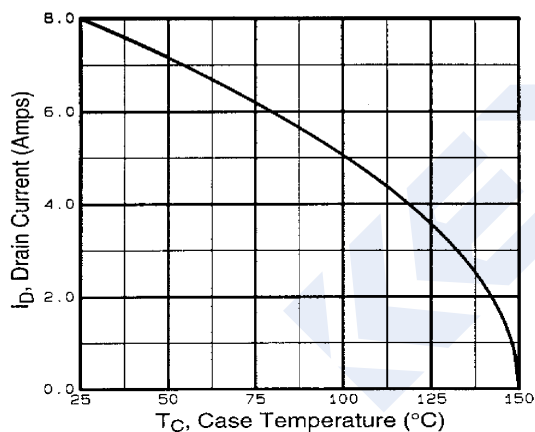


Fig 9. Maximum Drain Current Vs. Case Temperature

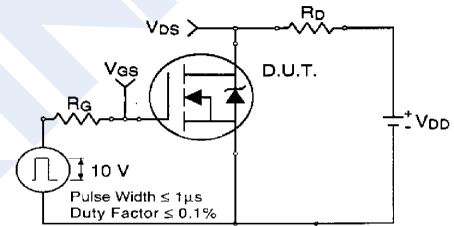


Fig 10a. Switching Time Test Circuit

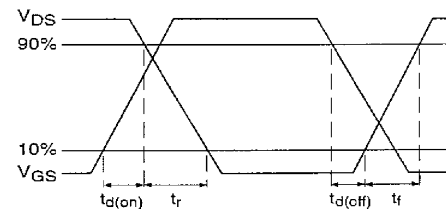


Fig 10b. Switching Time Waveforms

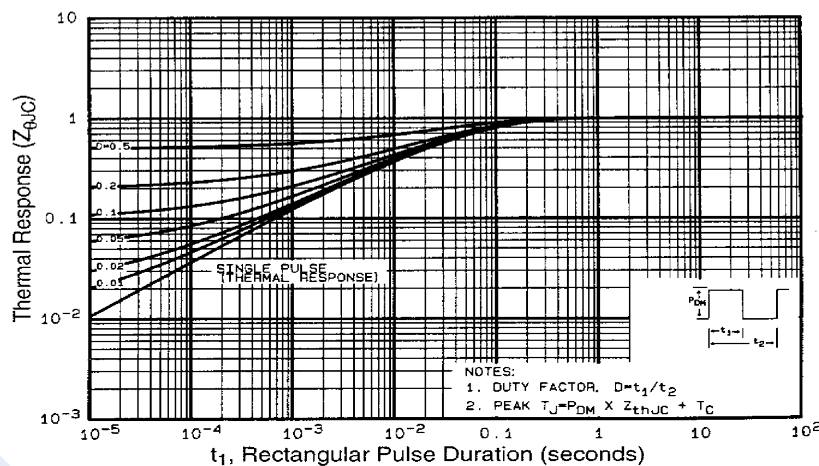


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

N-Channel MOSFET

IRF840S (KRF840S)

■ Typical Characteristics

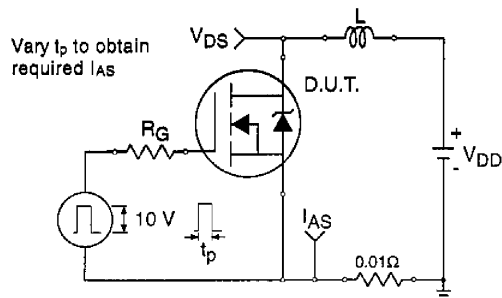


Fig 12a. Unclamped Inductive Test Circuit

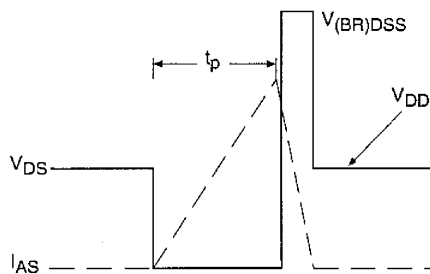


Fig 12b. Unclamped Inductive Waveforms

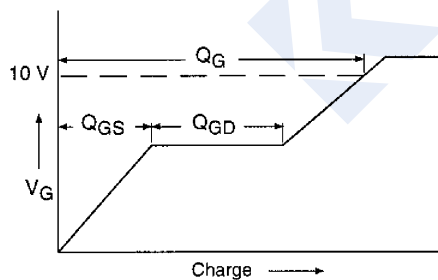


Fig 13a. Basic Gate Charge Waveform

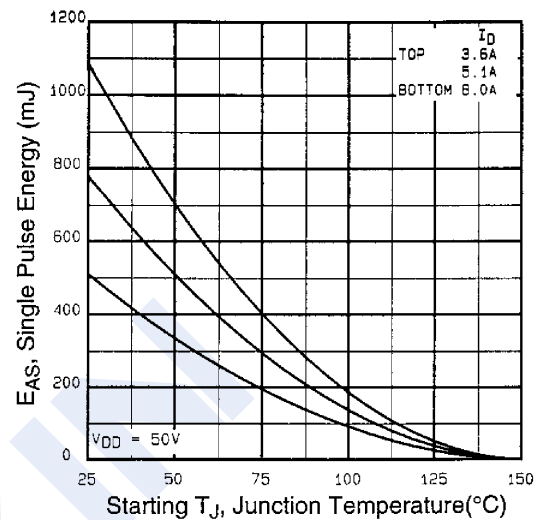


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

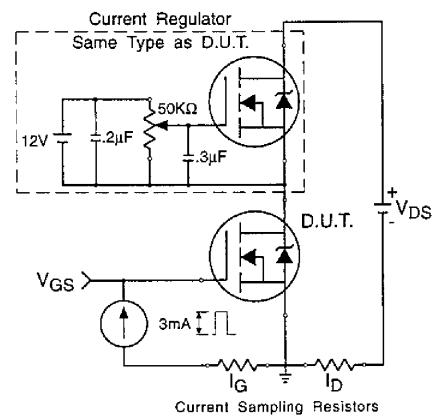


Fig 13b. Gate Charge Test Circuit