

IRF830

Power Field Effect Transistor N-Channel Enhancement Mode



- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ to Minimize On-Losses, Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use with Inductive Loads

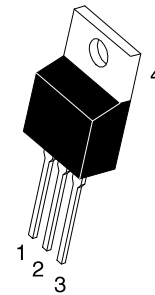
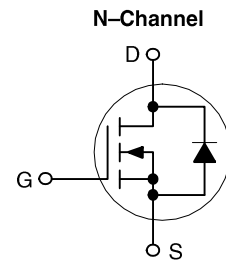
POWER FET
4.5 AMPERES
500 VOLTS
 $R_{DS(on)} = 1.5 \Omega$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	500	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 M\Omega$)	V_{DGR}	500	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current	I_D		Adc
Continuous, $T_C = 25^\circ$		4.5	
Continuous, $T_C = 100^\circ C$		3.0	
Peak, $T_C = 25^\circ C$		18	
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6	Watts W/ $^\circ C$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance			$^\circ C/W$
— Junction-to-Case	$R_{\theta JC}$	1.67	
— Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	300	$^\circ C$



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PIN ASSIGNMENT	
1	Gate
2	Drain
3	Source
4	Drain

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc)	V _{(BR)DSS}	500	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0 Vdc) (V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	—	0.2 1.0	mAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)	I _{GSS(f)}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)	I _{GSS(r)}	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA)	V _{GS(th)}	2.0	4.0	Vdc
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 2.5 Adc)	R _{DS(on)}	—	1.5	Ohm
On-State Drain Current (V _{GS} = 10 V) (V _{DS} ≥ 6.75 Vdc)	I _{D(on)}	4.5	—	Adc
Forward Transconductance (V _{DS} ≥ 6.75 Vdc, I _D = 2.5 Adc)	g _{FS}	2.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	800	pF
Output Capacitance		C _{oss}	—	200	
Reverse Transfer Capacitance		C _{rss}	—	60	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{DD} = 200 Vdc, I _D = 2.5 Apk, R _G = 15 Ω)	t _{d(on)}	—	30	ns
Rise Time		t _r	—	30	
Turn-Off Delay Time		t _{d(off)}	—	55	
Fall Time		t _f	—	30	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 10 Vdc, I _D = Rated I _D)	Q _g	22 (Typ)	30	nC
Gate-Source Charge		Q _{gs}	12 (Typ)	—	
Gate-Drain Charge		Q _{gd}	10 (Typ)	—	

SOURCE-DRAIN DIODE CHARACTERISTICS (1)

Forward On-Voltage	(I _S = Rated I _D , V _{GS} = 0)	V _{SD}	1.1 (Typ)	1.6	Vdc
Forward Turn-On Time		t _{on}	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	450 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

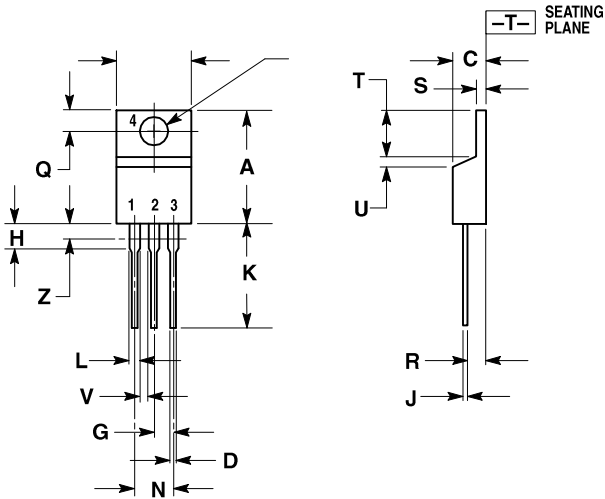
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _D	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _S	7.5 (Typ)	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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PACKAGE DIMENSIONS

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- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN