

HEXFET® Power MOSFET for DC-DC Converters

- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- 100% Tested for R_g
- Lead-Free

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Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRF7811W has been optimized for all parameters that are critical in synchronous buck converters including R_{DS(on)}, gate charge and C_{dv/dt}-induced turn-on immunity. The IRF7811W offers particularly low R_{DS(on)} and high C_{dv/dt} immunity for synchronous FET applications.

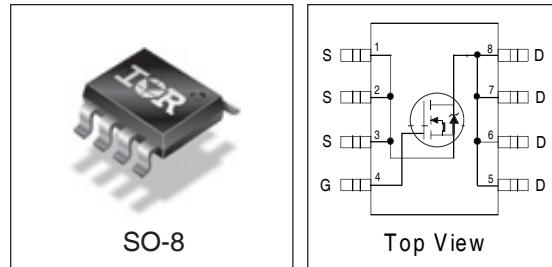
The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 3W is possible in a typical PCB mount application.

Absolute Maximum Ratings

Parameter	Symbol	IRF7811W	Units
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±12	
Continuous Drain or Source Current (V _{GS} ≥ 4.5V)	I _D	14	A
		13	
Pulsed Drain Current①	I _{DM}	109	
Power Dissipation	P _D	3.1	W
		3.0	
Junction & Storage Temperature Range	T _J , T _{STG}	–55 to 150	°C
Continuous Source Current (Body Diode)	I _S	3.8	A
Pulsed Source Current①	I _{SM}	109	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	R _{θJA}	40	°C/W
Maximum Junction-to-Lead	R _{θJL}	20	°C/W



DEVICE CHARACTERISTICS⑤

	IRF7811W
R _{DS(on)}	9.0mΩ
Q _G	18nC
Q _{sw}	5.5nC
Q _{oss}	12nC

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Electrical Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30	–	–	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source on Resistance	$R_{DS(on)}$		9.0	12	m Ω	$V_{GS} = 4.5V, I_D = 15A$ ②
Gate Threshold Voltage	$V_{GS(th)}$	1.0			V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source Leakage Current	I_{DSS}			30	μA	$V_{DS} = 24V, V_{GS} = 0$
				150		$V_{DS} = 24V, V_{GS} = 0,$ $T_j = 100^\circ C$
Gate-Source Leakage Current	I_{GSS}			± 100	nA	$V_{GS} = \pm 12V$
Total Gate Chg Cont FET	Q_G		18	24	nC	$V_{GS}=5.0V, I_D=15A, V_{DS}=16V$
Total Gate Chg Sync FET	Q_G		15.6			$V_{GS} = 5V, V_{DS} < 100mV$
Pre-Vth Gate-Source Charge	Q_{GS1}		6.0			$V_{DS} = 16V, I_D = 15A$
Post-Vth Gate-Source Charge	Q_{GS2}		1.4			
Gate to Drain Charge	Q_{GD}		4.1			
Switch Chg($Q_{GS2} + Q_{GD}$)	Q_{SW}		5.5			
Output Charge	Q_{OSS}		12			$V_{DS} = 16V, V_{GS} = 0$
Gate Resistance	R_G		2.0	4.0	Ω	
Turn-on Delay Time	$t_{d(on)}$		11		ns	$V_{DD} = 16V, I_D = 15A$
Rise Time	t_r		11			$V_{GS} = 5.0V$
Turn-off Delay Time	$t_{d(off)}$		29			Clamped Inductive Load
Fall Time	t_f		9.9			
Input Capacitance	C_{iss}	–	2335	–	pF	$V_{DS} = 16V, V_{GS} = 0$
Output Capacitance	C_{oss}	–	400	–		
Reverse Transfer Capacitance	C_{rss}	–	119	–		

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}			1.25	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge④	Q_{rr}		45		nC	$di/dt \sim 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$		41		nC	$di/dt = 700A/\mu s$ (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$

- Notes:**
- ① Repetitive rating; pulse width limited by max. junction temperature.
 - ② Pulse width $\leq 400 \mu s$; duty cycle $\leq 2\%$.
 - ③ When mounted on 1 inch square copper board
 - ④ Typ = measured - Q_{oss}
 - ⑤ Typical values of $R_{DS(on)}$ measured at $V_{GS} = 4.5V, Q_G, Q_{SW}$ and Q_{OSS} measured at $V_{GS} = 5.0V, I_F = 15A$.

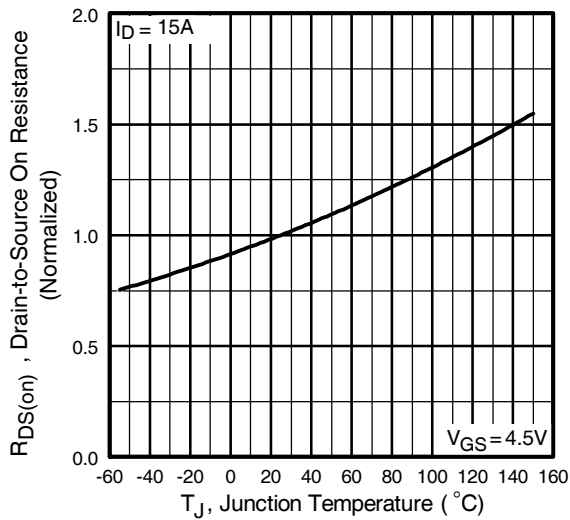


Fig 1. Normalized On-Resistance
Vs. Temperature

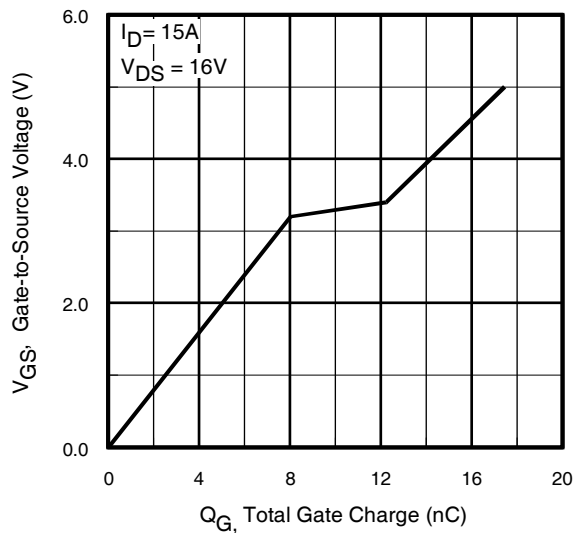


Fig 2. Typical Gate Charge Vs.
Gate-to-Source Voltage

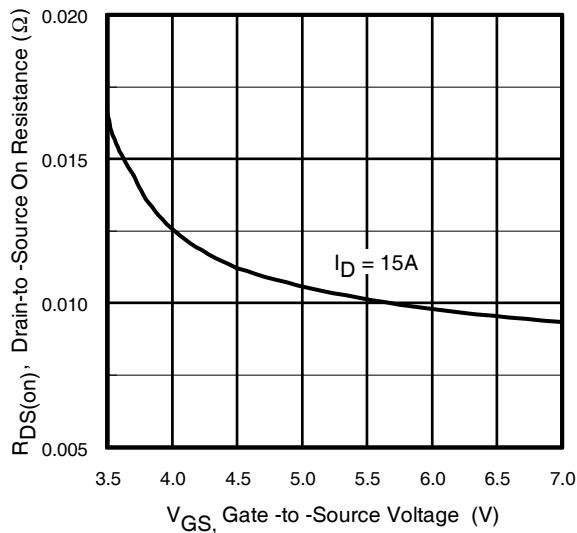


Fig 3. On-Resistance Vs. Gate Voltage

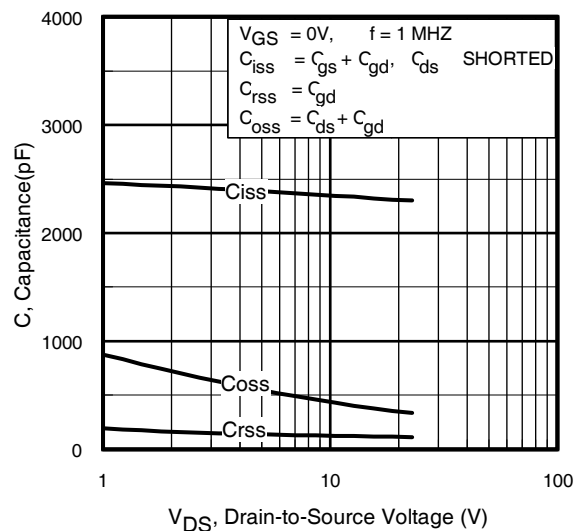


Fig 4. Typical Capacitance Vs.
Drain-to-Source Voltage

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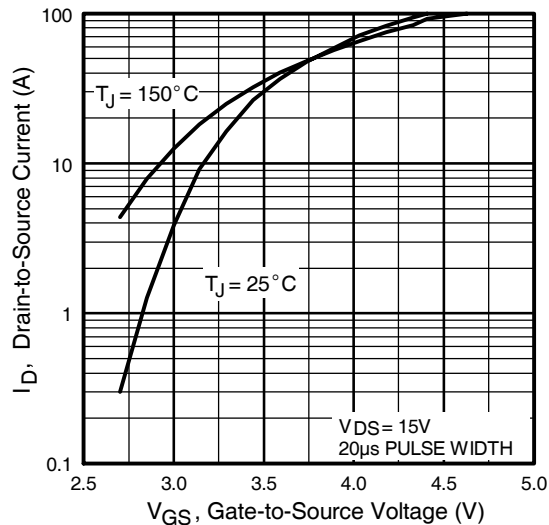


Fig 5. Typical Transfer Characteristics

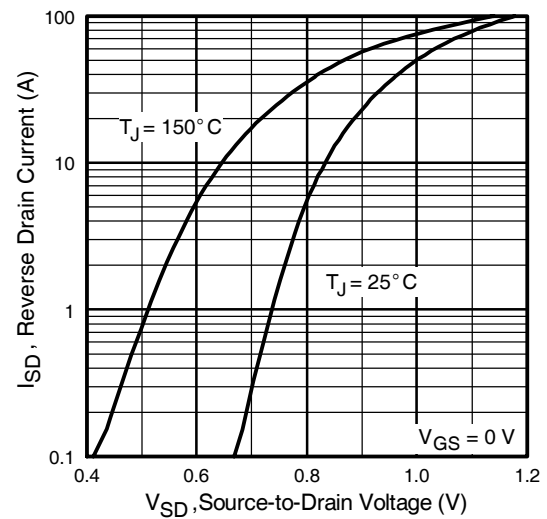


Fig 6. Typical Source-Drain Diode Forward Voltage

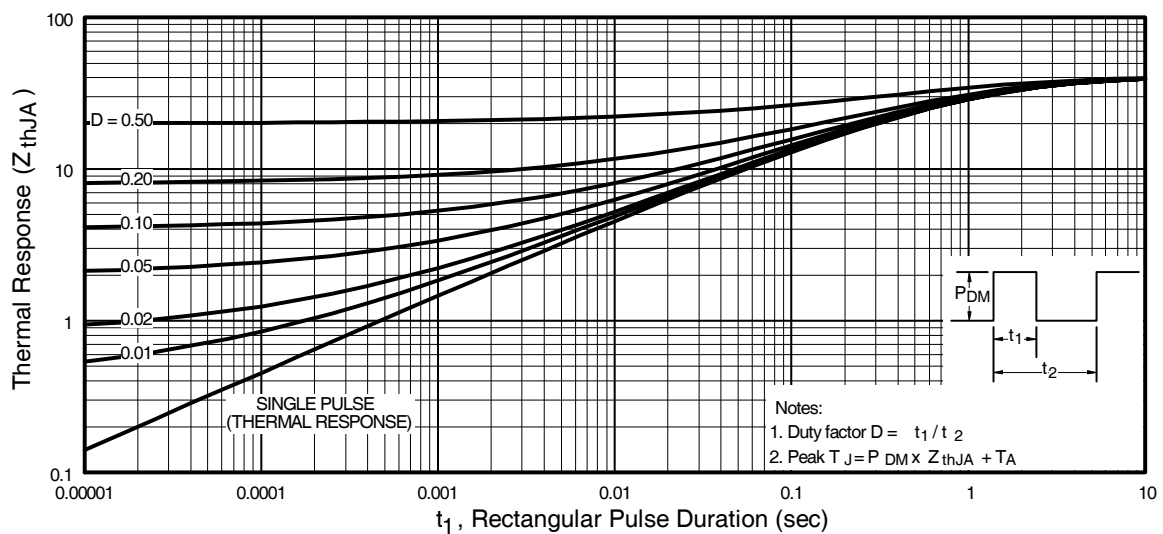
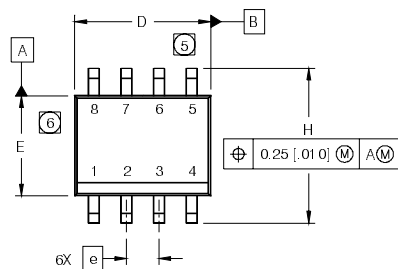


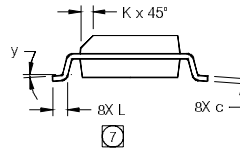
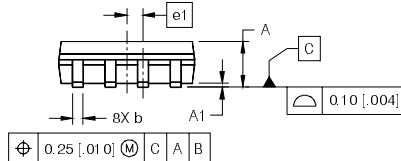
Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SO-8 Package Outline

Dimensions are shown in millimeters (inches)



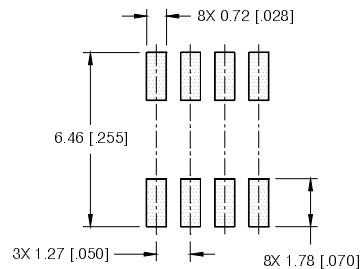
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

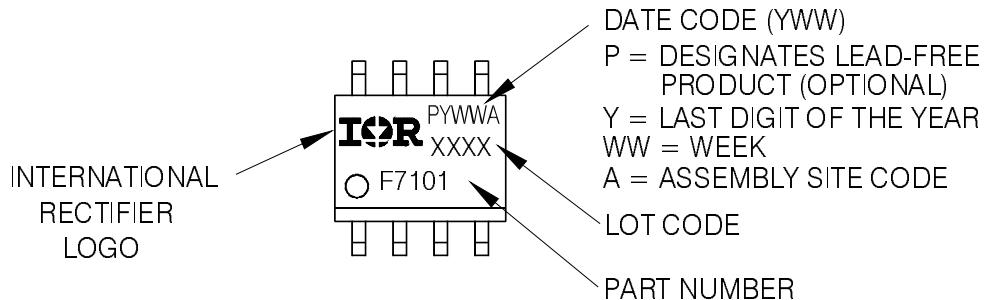
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

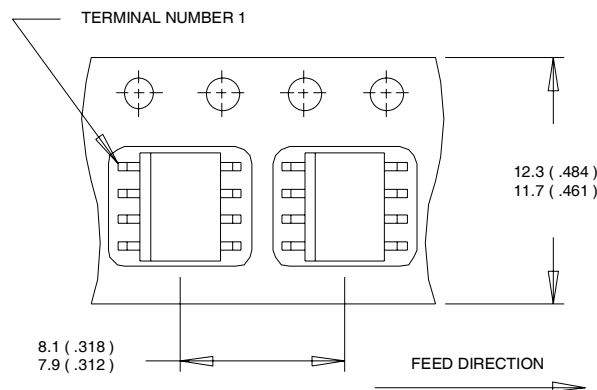


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SO-8 Tape and Reel

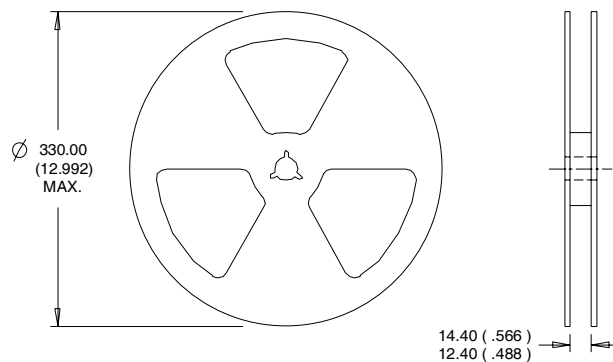
Dimensions are shown in millimeters (inches)

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NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.

This product has been designed and qualified for the consumer market.

Qualifications Standards can be found on IR's Web site.

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