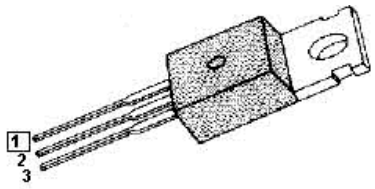
IRF634A
Advanced Power MOSFET

FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Extended Safe Operating Area
- Lower Leakage Current:10μA (Max.)@VDS=250V
- Lower $R_{DS(ON)}$: 0.327 Ω(Typ.)

BV_{DSS}=250V
$R_{DS(on)}$=0.45Ω
I_D=8.1A

TO-220



1. Gate 2. Drain 3.Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	250	V
I_D	Continuous Drain Current (Tc=25°C)	8.1	A
	Continuous Drain Current (Tc=100°C)	5.1	
I_{DM}	Drain Current-Pulsed (1)	32	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (2)	205	mJ
I_{AR}	Avalanche Current (1)	8.1	A
E_{AR}	Repetitive Avalanche Energy (1)	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	4.8	V/ns
P_D	Total Power Dissipation (Tc=25°C) Linear Derating Factor	74 0.59	W W/°C
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
TL	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

Thermal Resistance

Symbol	characteristic	Typ.	Max.	Units
$R_{\Theta JC}$	Junction-to-Case	-	1.69	°C/W
$R_{\Theta CS}$	Case-to-Sink	0.5	-	
$R_{\Theta JA}$	Junction-to-Ambient	-	62.5	

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	250	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	-	0.29	-	V/℃	I_D=250μA **See Fig 7**
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	V_{DS}=5V, I_D=250μA
I_{GSS}	Gate-Source Leakage, Forward	-	-	100	nA	V_{GS}=30V
	Gate-Source Leakage, Reverse	-	-	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	-	-	10	μA	V_{DS}=250V
		-	-	100		V_{DS}=200V, T_C=125℃
$R_{DS(on)}$	Static Drain-Source On-State Resistance	-	-	0.45	Ω	V_{GS}=10V, I_D=4.05A (4)
g_{fs}	Forward Transconductance	-	6.1	-	Ʊ	V_{DS}=40V, I_D=4.05A (4)
C_{iss}	Input Capacitance	-	730	950	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
C_{oss}	Output Capacitance	-	110	130		See Fig 5
C_{rss}	Reverse Transfer Capacitance	-	50	60		
$t_{d(on)}$	Turn-On Delay Time	-	13	40	ns	V_{DD}=125V, I_D=8.1A,
t_r	Rise Time	-	14	40		R_G=12 Ω
$t_{d(off)}$	Turn-off Delay Time	-	53	120		**See Fig 13** (4) (5)
t_f	Fall Time	-	21	50		
Q_g	Total Gate Charge	-	30	40	nC	V_{DS}=200V, V_{GS}=10V, I_D=8.1A
Q_{gs}	Gate-Source Charge	-	5.8	-		See Fig 6 & Fig 12 (4)(5)
Qgd	Gate-Drain (.Miller) Charge	-	13.5	-		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
Is	Continuous Source Current	-	-	8.1	A	Integral reverse pn-diode
I_{SM}	Pulsed-Source Current (1)	-	-	32		In the MOSFET
V_{SD}	DiodeForward Voltage (4)	-	-	1.5	V	T_J=25°C, Is=8.1A, V_{GS}=0V
trr	Reverse Recovery Time	-	190	-	ns	T_J=25°C, I_F=8.1A
Qrr	Reverse Recovery Charge	-	1.28	-	μC	di_F/dt=100A/μs (4)

Notes:

(1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
(2) L=5mH, I_{AS}=8.1A, V_{DD}=50V, R_G=27 Ω, Starting T_J=25°C
(3) I_{SD}≤8.1A, di/td≤210A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25°C
(4) Pulse Test: Pulse Width = 250μs, Duty Cycle ≤2%
(5) Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

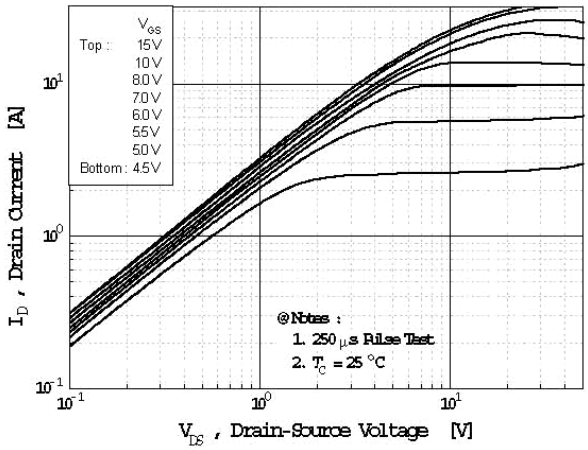


Fig 2. Transfer Characteristics

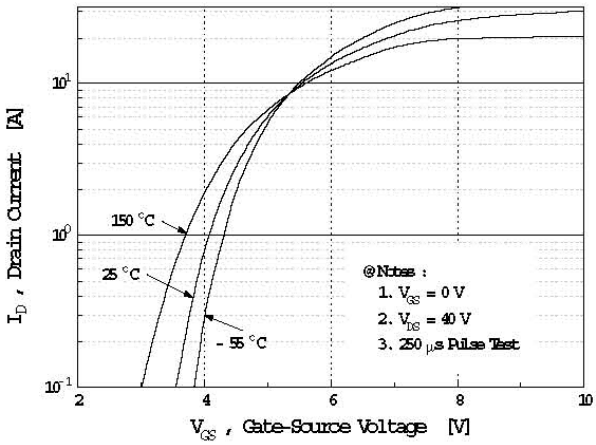


Fig 3. On-Resistance vs. Drain Current

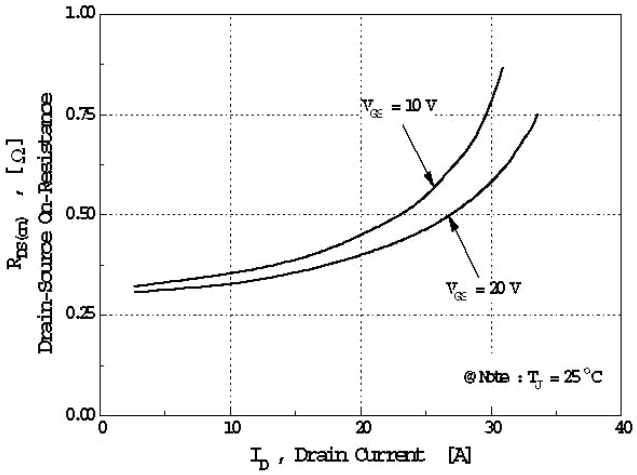


Fig 4. Source-Drain Diode Forward Voltage

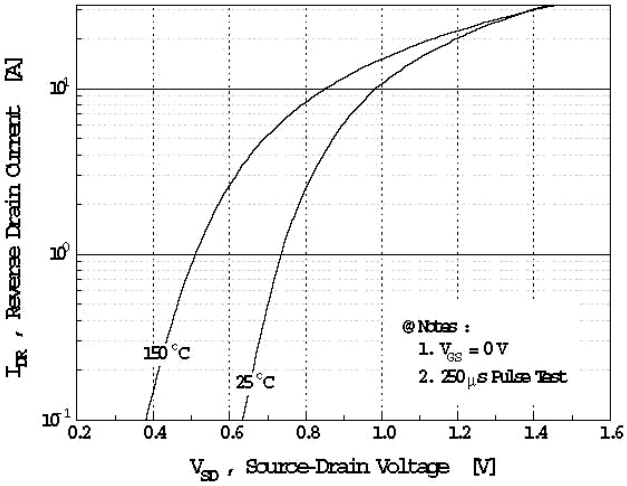


Fig 5. Capacitance vs. Drain-Source Voltage

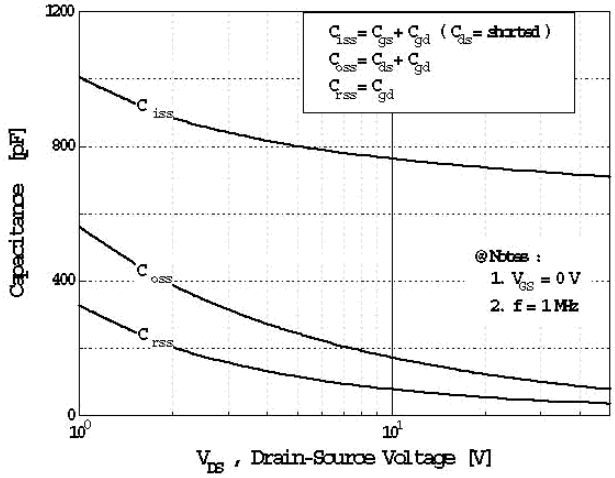


Fig 6. Gate Charge vs. Gate-Source Voltage

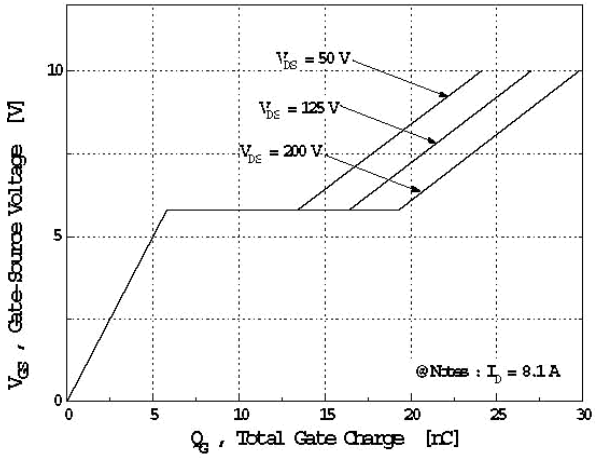


Fig 7. Breakdwon voltage vs. Temperature

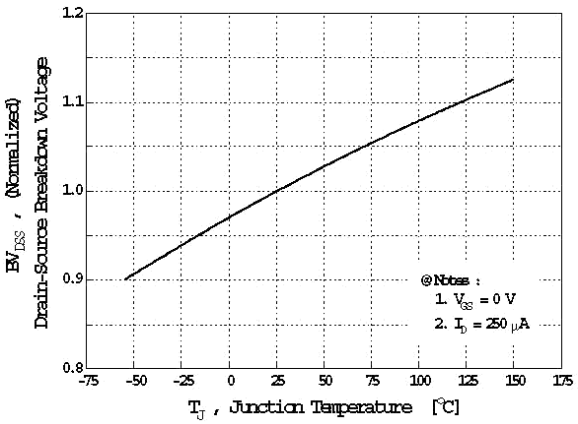


Fig 8. On-Resistance vs. Temperature

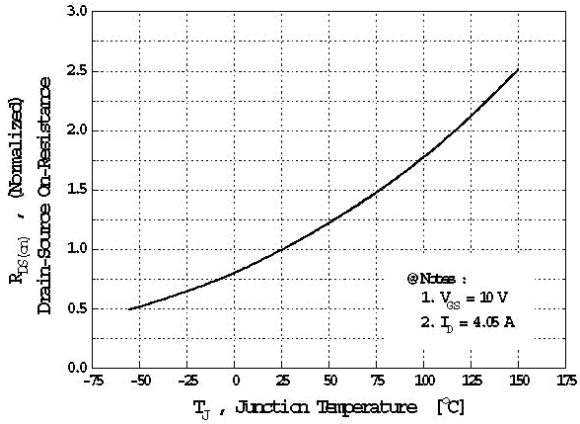


Fig 9. Max. Safe Operating Area

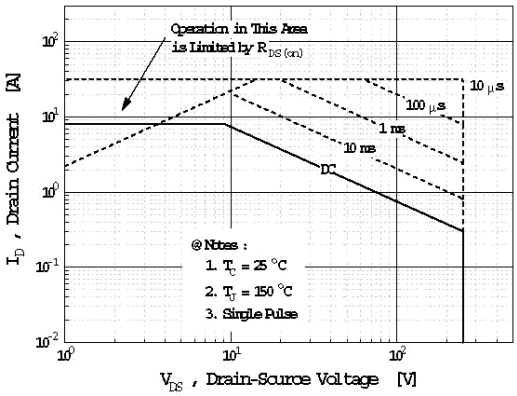


Fig 10. Max. Drain Current vs. Case Temperature

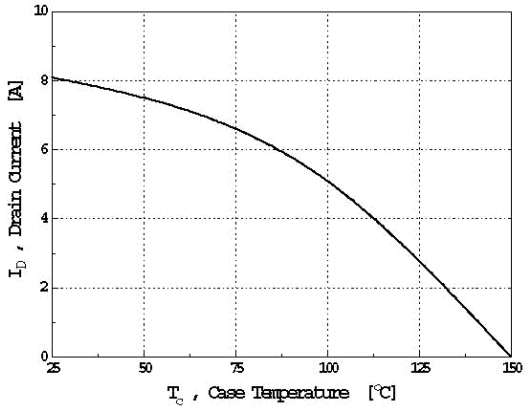


Fig 11. Thermal Response

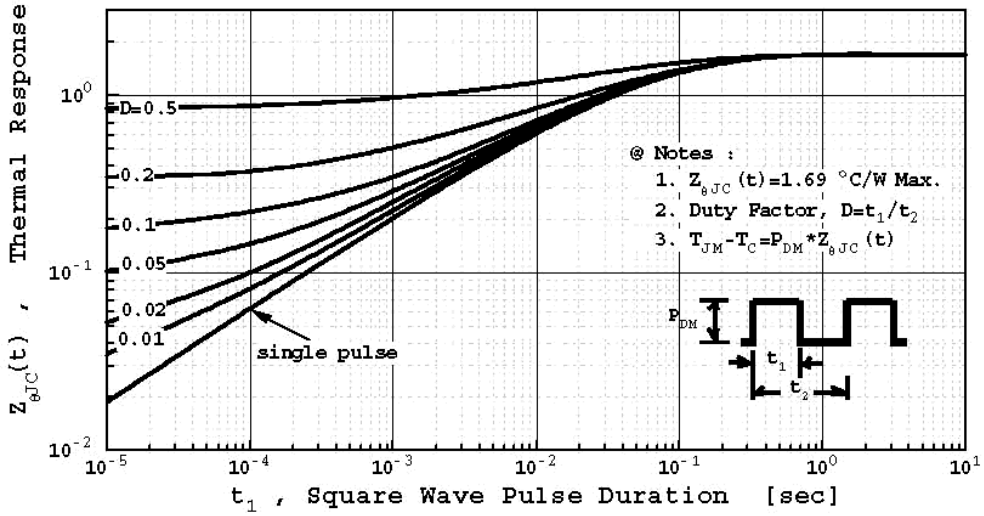


Fig 12. Gate Charge Test Circuit & Waveform

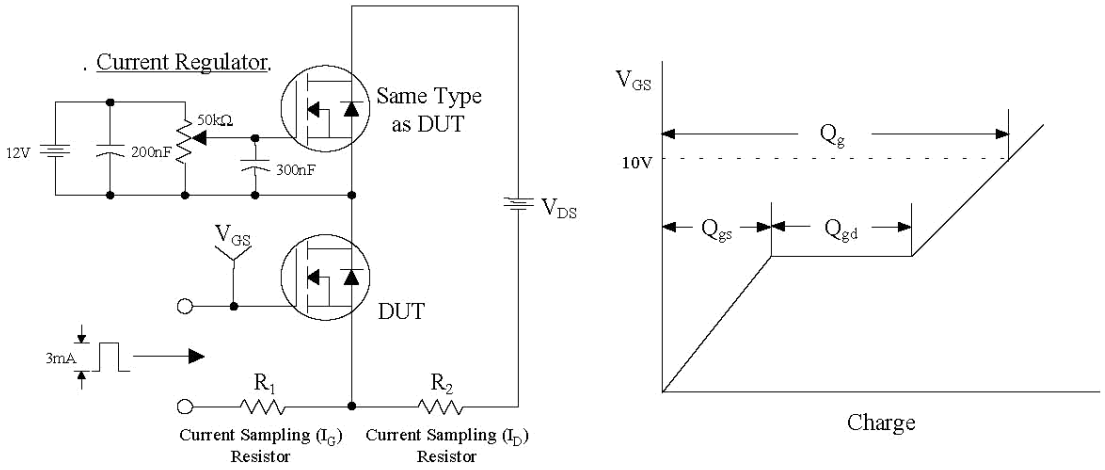


Fig 13. Resistive Switching Test Circuit & Waveforms

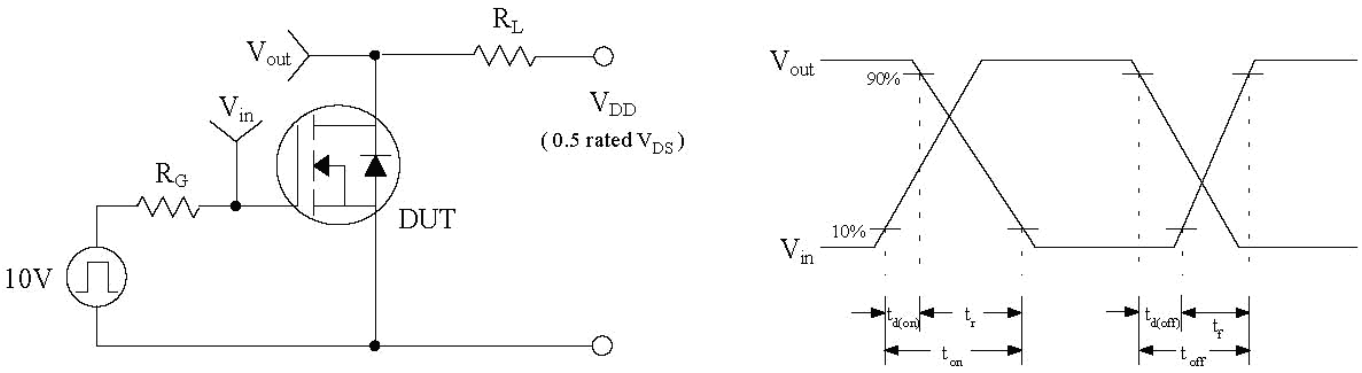


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

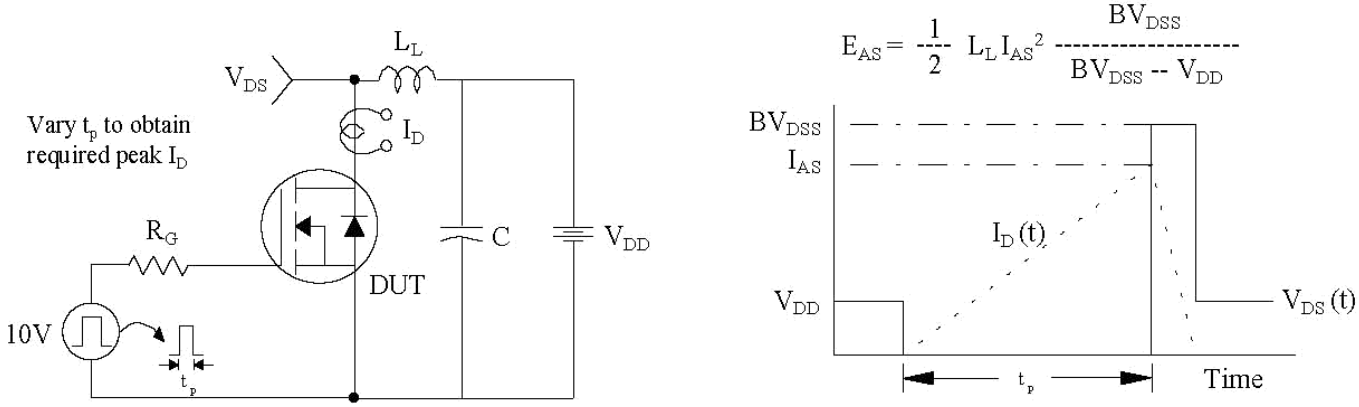


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms