

IR2125Z

CURRENT LIMITING SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +400V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 12 to 18V
- Undervoltage lockout
- Current detection and limiting loop to limit driven power transistor current
- Error lead indicates fault conditions and programs shutdown time
- Output in phase with input

Product Summary

V_{OFFSET}	400V max.
I_O+/-	1A / 2A
V_{OUT}	12 - 18V
V_{CSt}	230 mv
t_{on/off} (typ.)	150 & 150 ns

Description

The IR2125Z is a high voltage, high speed power MOSFET and IGBT driver with over-current limiting protection circuitry. Proprietary GVIC and latch immune CMOS technologies enable ruggedized minilithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction.

The protection circuitry detects over-current in the driven power transistor and limits the gate drive voltage. Cycle by cycle shutdown is programmed by an external capacitor which directly controls the time interval between detection of the over-current limiting conditions and latched shutdown. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 400 volts.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Units
V _B	High Side Floating Supply Voltage	-0.3	V _S + 20	V
V _S	High Side Floating Supply Offset Voltage	-5	400	
V _{HO}	High Side Floating Output Voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Logic Supply Voltage	-0.3	20	
V _{ERR}	Error Signal Voltage	-0.3	V _{CC} + 0.3	
V _{CS}	Current Sense Voltage	V _S - 0.3	V _B + 0.3	
V _{IN}	Logic Input Voltage	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P _D	Package Power Dissipation @ T _A ≤ +25°C	—	1.0	W
R _{qJA}	Thermal Resistance, Junction to Ambient	—	100	°C/W
T _J	Junction Temperature	-55	125	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset ratings are tested with all supplies biased at 15V differential.

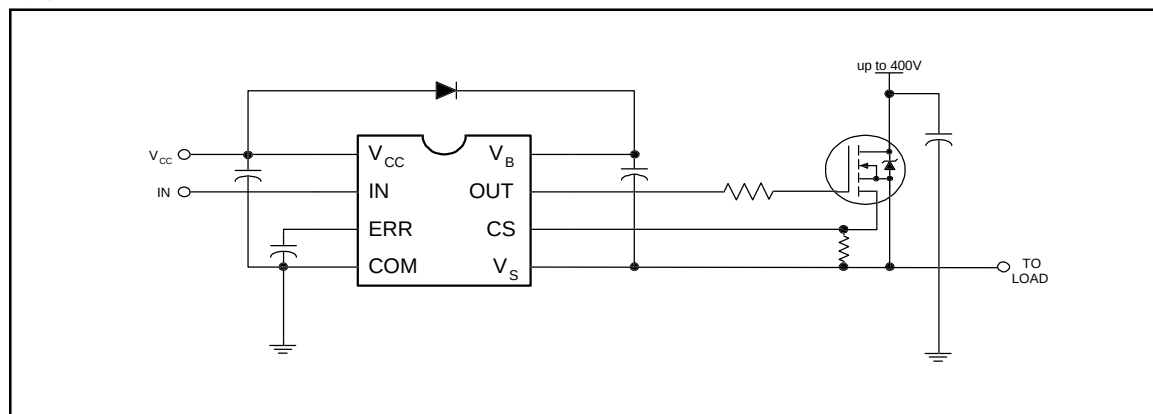
Symbol	Parameter	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	$V_S + 12$	$V_S + 18$	V
V_S	High Side Floating Supply Offset Voltage	-5	400	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	12	18	
V_{IN}	Logic Input Voltage	V_{SS}	V_{CC}	
V_{ERR}	Error Signal Voltage	V_{SS}	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_B	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, and C_L = 3300 PF and T_a = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3 through 6.

		Tj = 25°C			Tj = -55 to 125°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Max.	Units	Test Conditions
ton	Turn-On Propagation Delay	—	150	200	—	270	ns	VS = 0V to 400V CL = 3300pf
t _{off}	Turn-Off Propagation Delay	—	150	300	—	330		
tr	Turn-On Rise Time	—	43	60	—	80		
tf	Turn-Off Fall Time	—	26	35	—	50		
tcs	CS to output shutdown propagation delay	—	0.7	1.2	—	1.4	μs	VS = 0V TO 400V C _{err} = 270pf
t _{sd}	Shutdown Propagation Delay	—	1.7	2.2	—	2.5		
t _{err}	CS to ERR pull-up propagation time	—	9	22	—	25		

Typical Connection



Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V and $T_a = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. V_O and I_O parameters are referenced to V_S .

Symbol	Parameter	$T_j = 25^\circ\text{C}$			$T_j = -55 \text{ to } 125^\circ\text{C}$		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
I_{LK}	Offset Supply Leakage Current	—	—	50	—	250	μA	$V_B = V_S = 400\text{V}$
I_{QBS}	Quiescent V_{BS} Supply Current	—	400	1000	—	1300		$I_N = CS = 0\text{V}$, or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	700	1200	—	1500		$I_N = CS = 0\text{V}$, or 5V
I_{IN}^+	Logic "1" Input Bias Current	—	4	25	—	30		$I_N = 5\text{V}$
I_{IN}^-	Logic "0" Input Bias Current	—	—	1.0	—	1.0		$I_N = 0\text{V}$
I_{CS}^+	"High" CS Bias Current	—	6	15	—	30		$CS = 3\text{V}$
I_{CS}^-	"Low" CS Bias Current	—	—	1.0	—	1.0		$CS = 0\text{V}$
V_{IH}	Logic "1" Input Voltage	—	—	—	3.0	—	V	$V_{CC} = 10 \text{ TO } 20\text{V}$
V_{IL}	Logic "0" Input Voltage	—	—	—	—	0.8		
V_{ERR}^+	Logic "1" ERR Input Voltage	—	—	—	2.2	—		
V_{ERR}^-	Logic "0" ERR Input Voltage	—	—	—	—	0.8		
V_{CSTH}^+	CS Input Positive Going Threshold	150	230	320	—	—	mV	$10\text{V} < V_{CC} < 20\text{V}$
V_{CSTH}^-	CS Input Positive Going Threshold	130	200	300	—	—		$10\text{V} < V_{CC} < 20\text{V}$
V_{BSUV}^+	V_{BS} Supply Overvoltage Positive Going Threshold	8.5	9.3	10	—	—	V	
V_{BSUV}^-	V_{BS} Supply Undervoltage Negative Going Threshold	7.7	8.5	9.0	—	—		
V_{BSOV}^+	V_{BS} Supply Overvoltage Positive Going Threshold	19.8	21.5	23	—	—		
V_{BSOV}^-	V_{BS} Supply Undervoltage Negative Going Threshold	19.1	20.8	22.4	—	—		
V_{CCUV}^+	V_{CC} Supply Overvoltage Positive Going Threshold	8.3	8.8	9.6	—	—		
V_{CCUV}^-	V_{CC} Supply Undervoltage Negative Going Threshold	7.3	8.1	8.7	—	—		
V_{CCOV}^+	V_{CC} Supply Overvoltage Positive Going Threshold	20	21.2	23	—	—		
V_{CCOV}^-	V_{CC} Supply Undervoltage Negative Going Threshold	19.3	20.7	22.5	—	—		
I_{ERR}	ERR Timing Charge Current	40	100	130	—	—	μA	$I_N = 5\text{V}$, $CS = 3\text{V}^+$ $ERR < V_{ERR}^+$
I_{ERR}^+	ERR Pull-up Current	8.0	15	—	—	—	mA	$I_N = 5\text{V}$, $CS = 3\text{V}^+$ $ERR > V_{ERR}^+$
I_{ERR}^-	ERR Pull-down Current	16	30	—	—	—		$I_N = 0\text{V}$
V_{OH}	High Level Output Voltage	$V_B - 0.1$	—	—	$V_B - 0.1$	—	V	$I_N = 5\text{V}$, $I_O = 0\text{A}$
V_{OL}	Low Level Output Voltage	—	—	$V_S + 0.1$	—	$V_S + 0.1$		$I_N = 0\text{V}$, $I_O = 0\text{A}$
$R_{on,ON}$	Output High on Resistance	—	9	—	—	—	Ω	
$R_{on,OFF}$	Output Low on Resistance	—	3	—	—	—		

International
IOR Rectifier

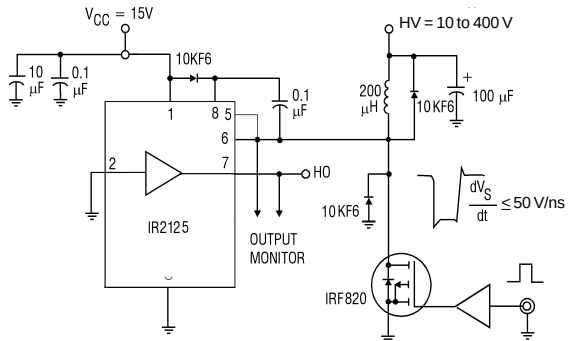


Figure 2. Floating Supply Voltage Transient Test Circuit

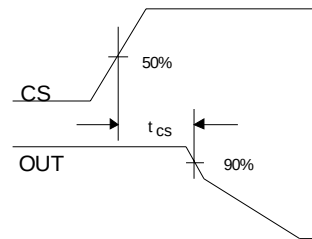


Figure 4. ERR Shutdown Waveform Definitions

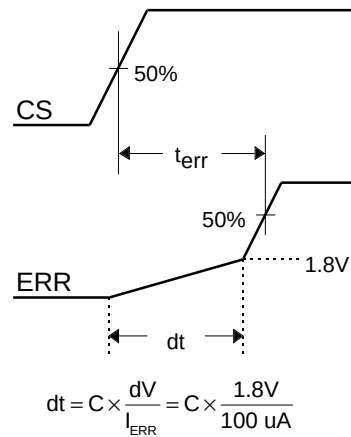


Figure 6. CS to ERR Waveform Definitions

$$dt = C \times \frac{dV}{I_{ERR}} = C \times \frac{1.8V}{100 \text{ uA}}$$

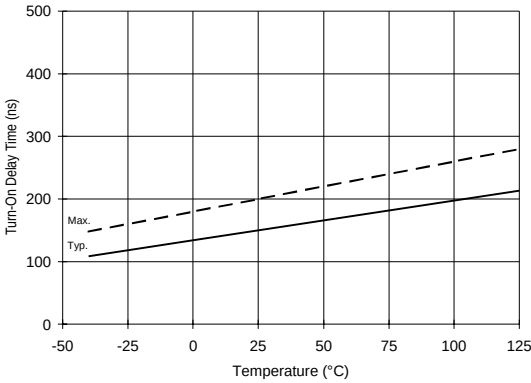


Figure 7A. Turn-On Time vs. Temperature

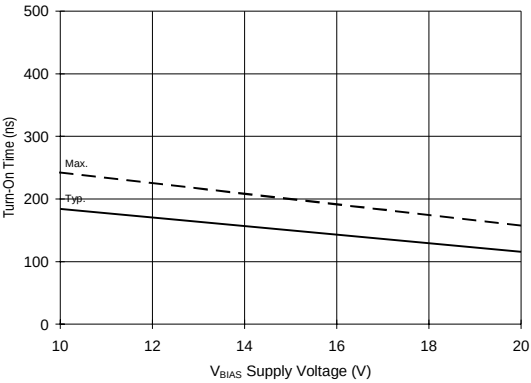


Figure 7B. Turn-On Time vs. Voltage

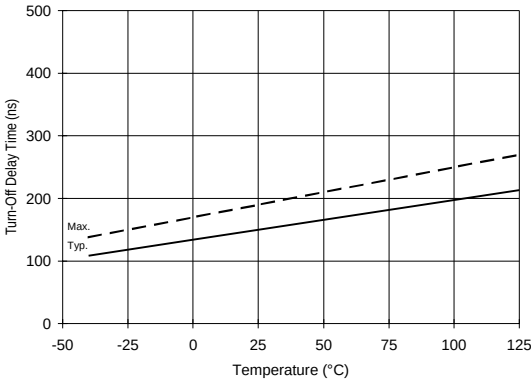


Figure 8A. Turn-Off Time vs. Temperature

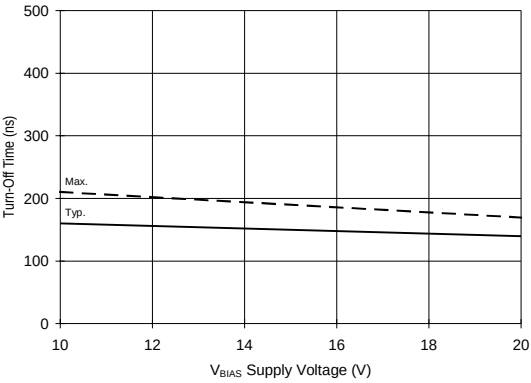


Figure 8B. Turn-Off Time vs. Voltage

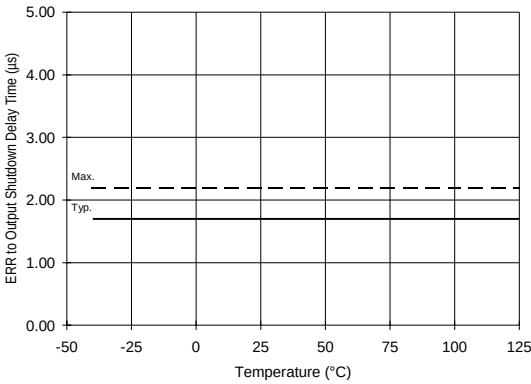


Figure 9A. ERR to Output Shutdown vs. Temperature

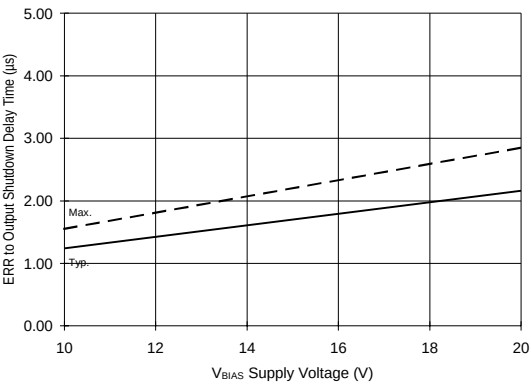


Figure 9B. ERR to Output Shutdown vs. Voltage

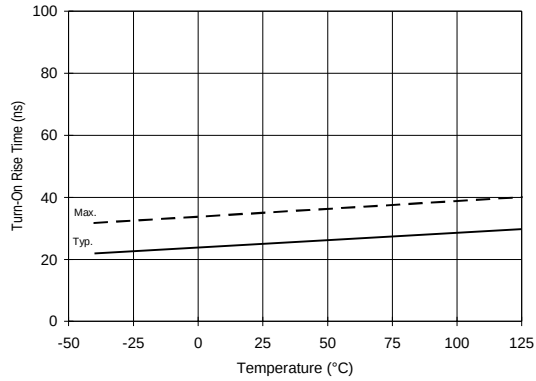


Figure 10A. Turn-On Rise Time vs. Temperature

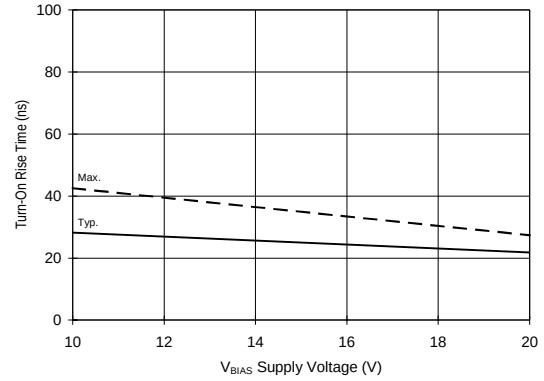


Figure 10B. Turn-On Rise Time vs. Voltage

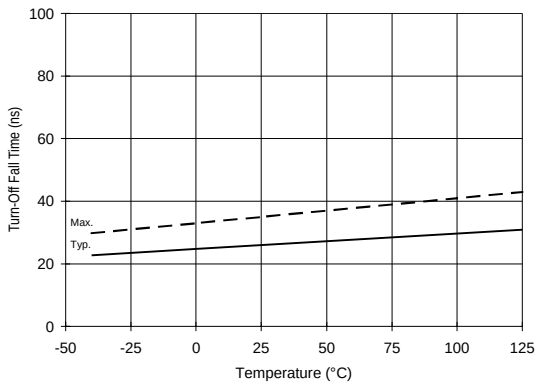


Figure 11A. Turn-Off Fall Time vs. Temperature

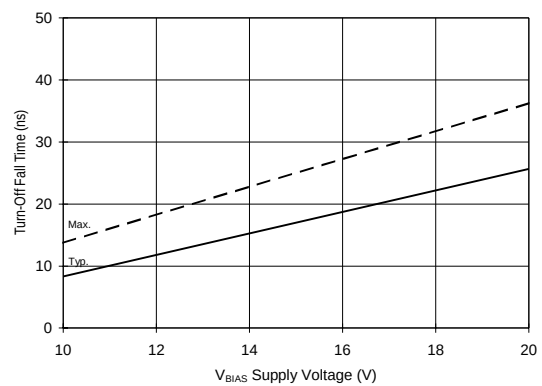


Figure 11B. Turn-Off Fall Time vs. Voltage

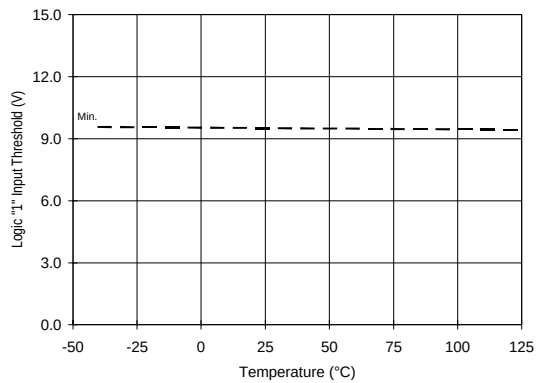


Figure 12A. Logic "1" Input Threshold vs. Temperature

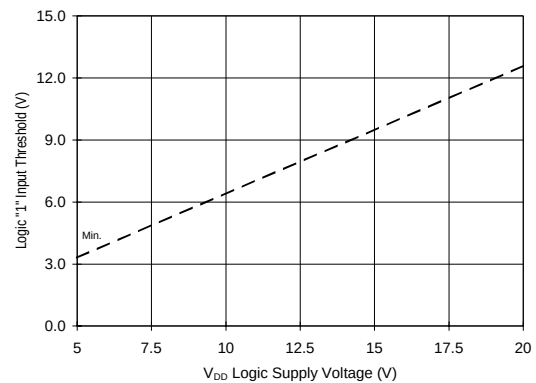


Figure 12B. Logic "1" Input Threshold vs. Voltage

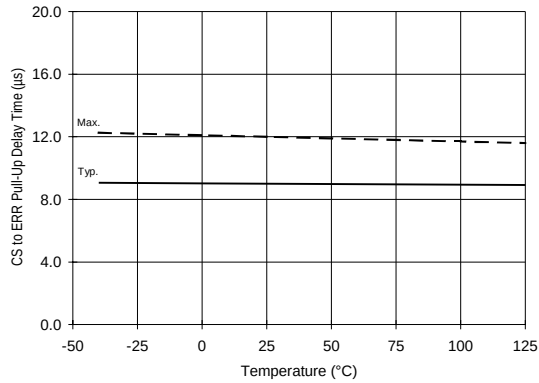


Figure 13A. CS to ERR Pull-Up vs. Temperature

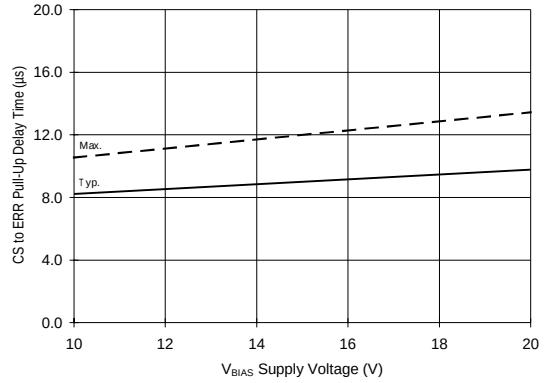


Figure 13B. CS to ERR Pull-Up vs. Voltage

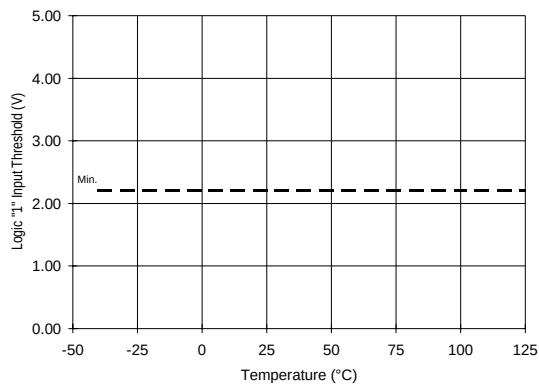


Figure 14A. Logic "1" Input Threshold vs. Temperature

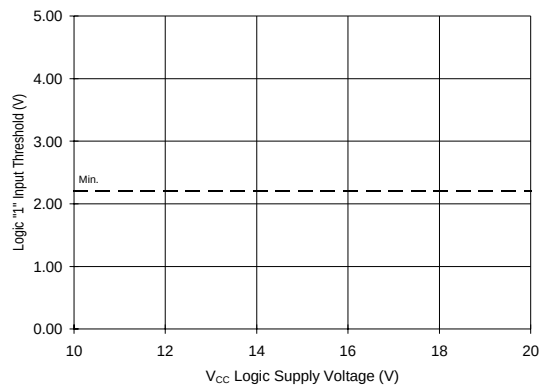


Figure 14B. Logic "1" Input Threshold vs. Voltage

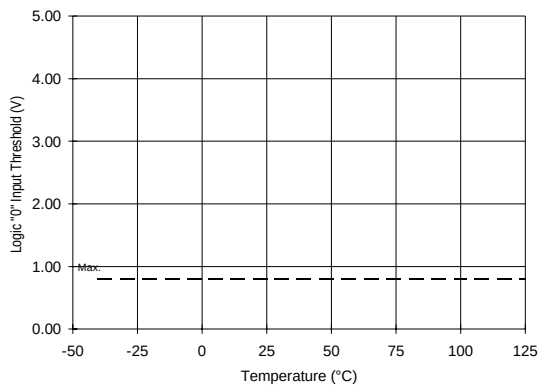


Figure 15A. Logic "0" Input Threshold vs. Temperature

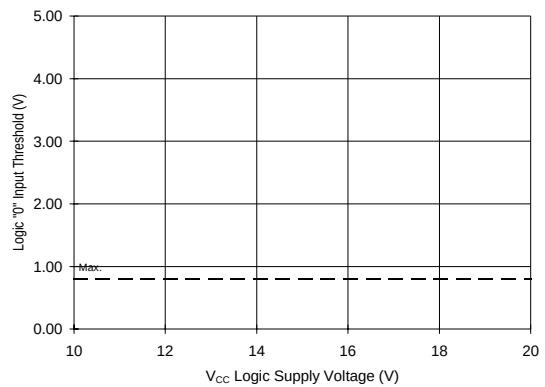


Figure 15B. Logic "0" Input Threshold vs. Voltage

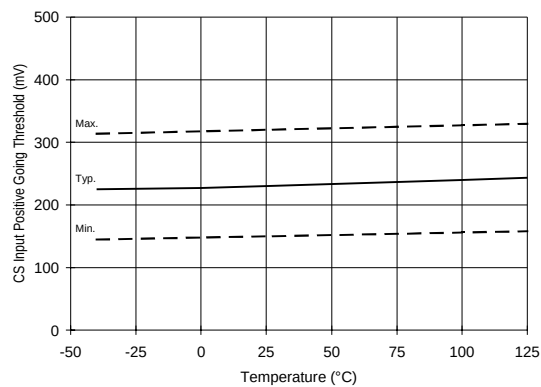


Figure 16A. CS Input Threshold (+) vs. Temperature

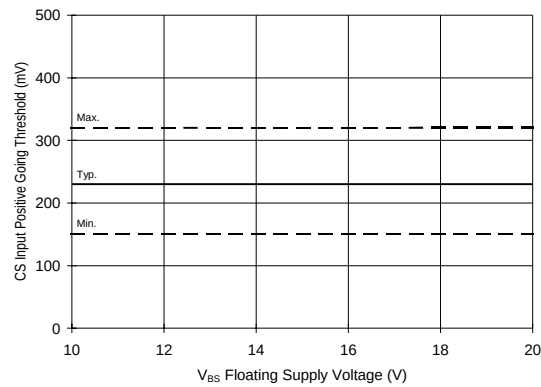


Figure 16B. CS Input Threshold (+) vs. Voltage

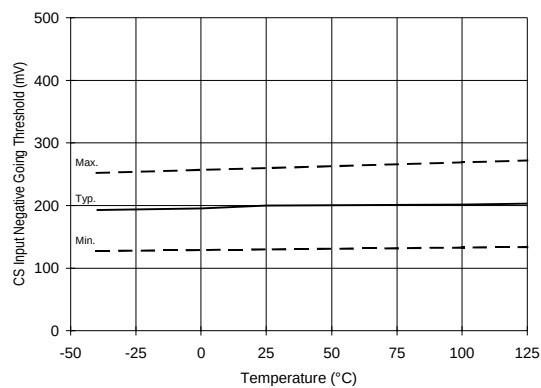


Figure 17A. CS Input Threshold (-) vs. Temperature

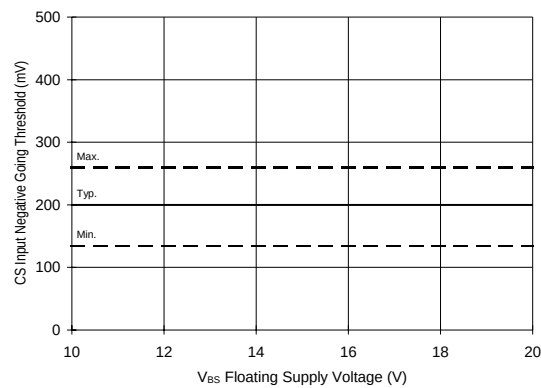


Figure 17B. CS Input Threshold (-) vs. Voltage

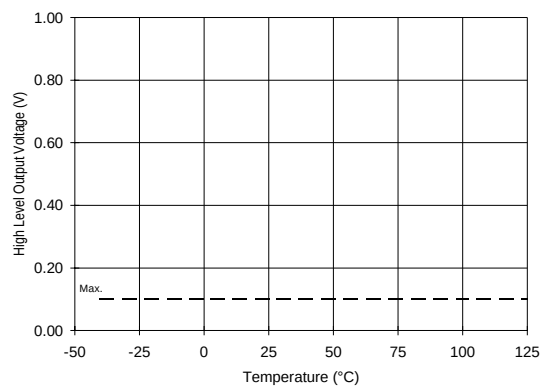


Figure 18A. High Level Output vs. Temperature

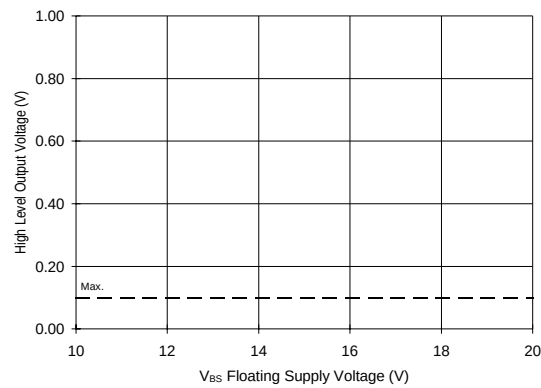


Figure 18B. High Level Output vs. Voltage

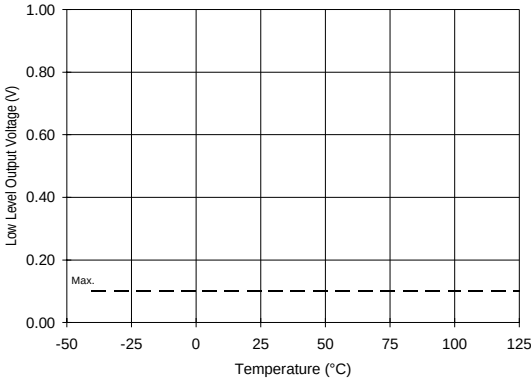


Figure 19A. Low Level Output vs. Temperature

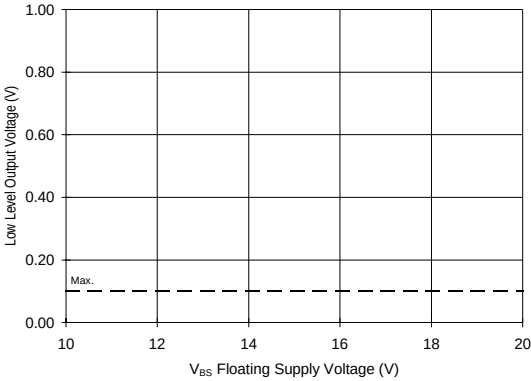


Figure 19B. Low Level Output vs. Voltage

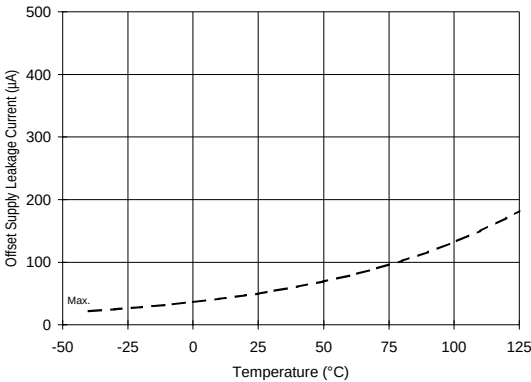


Figure 20A. Offset Supply Current vs. Temperature

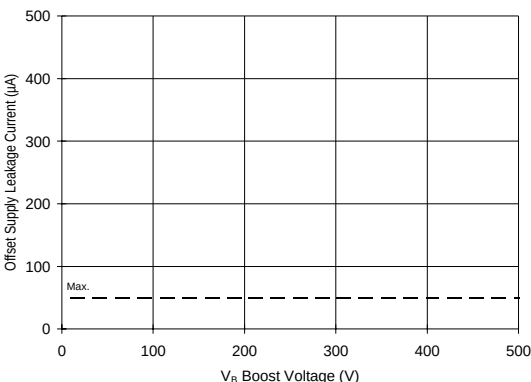


Figure 20B. Offset Supply Current vs. Voltage

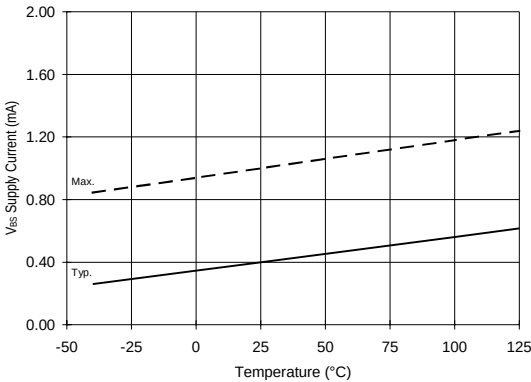


Figure 21A. V_{BS} Supply Current vs. Temperature

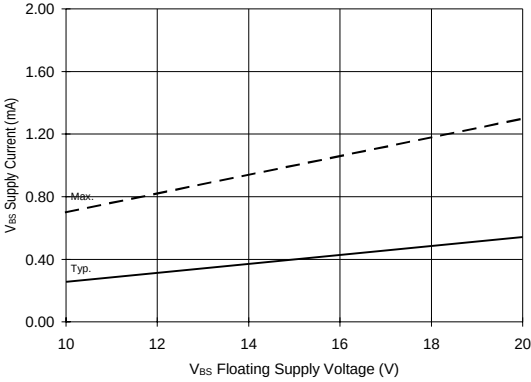


Figure 21B. V_{BS} Supply Current vs. Voltage

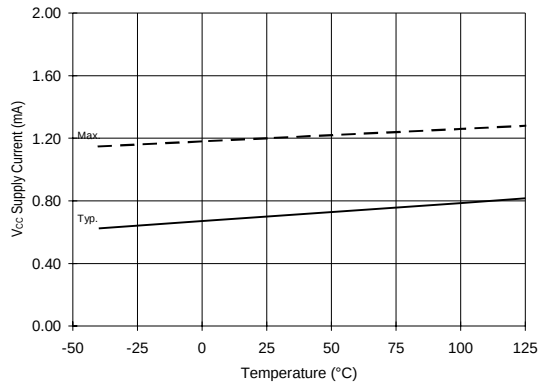


Figure 22A. V_{CC} Supply Current vs. Temperature

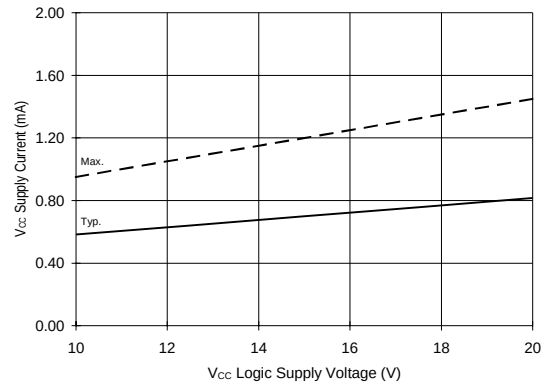


Figure 22B. V_{CC} Supply Current vs. Voltage

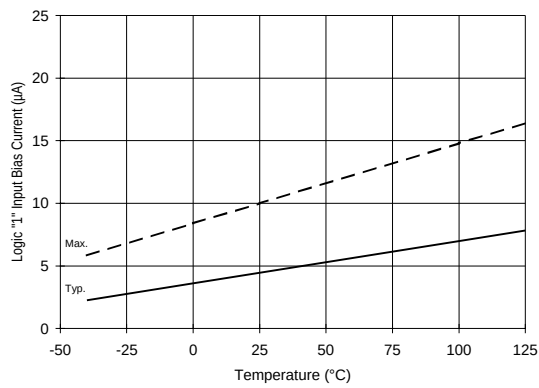


Figure 23A. Logic "1" Input Current vs. Temperature

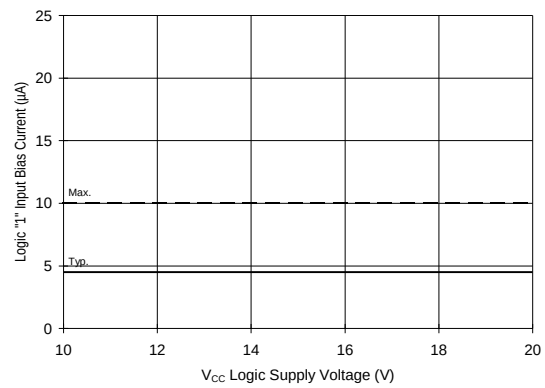


Figure 23B. Logic "1" Input Current vs. Voltage

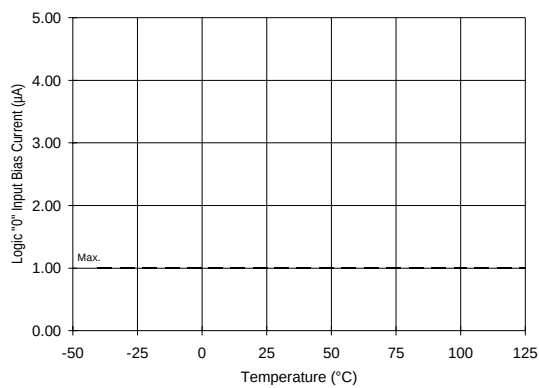


Figure 24A. Logic "0" Input Current vs. Temperature

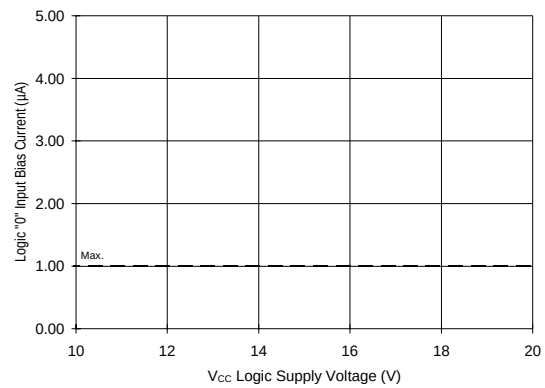


Figure 24B. Logic "0" Input Current vs. Voltage

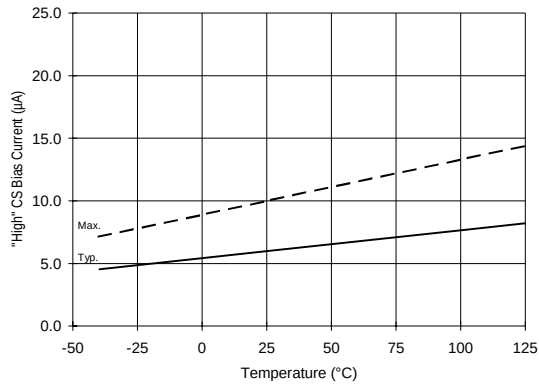


Figure 25A. "High" CS Bias Current vs. Temperature

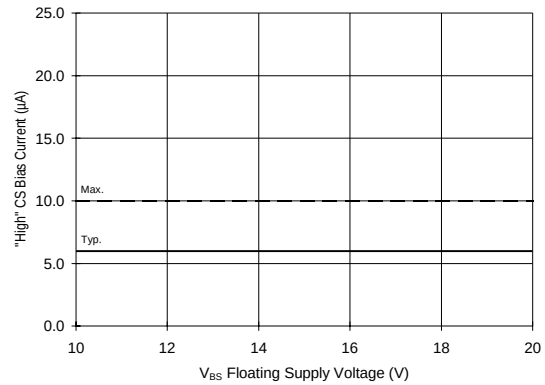


Figure 25B. "High" CS Bias Current vs. Voltage

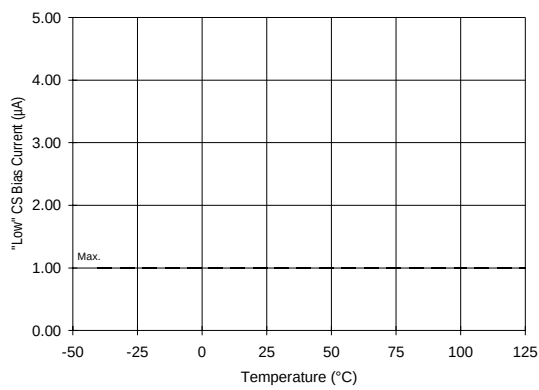


Figure 26A. "Low" CS Bias Current vs. Temperature

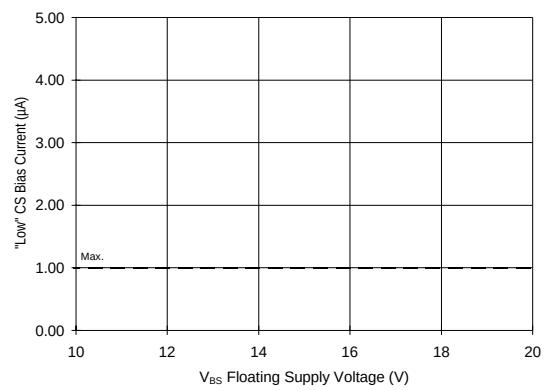


Figure 26B. "Low" CS Bias Current vs. Voltage

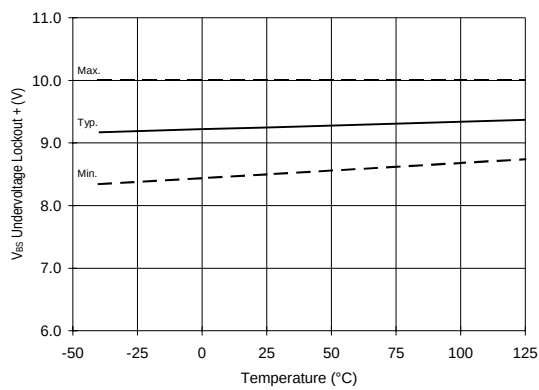


Figure 27. V_{BS} Undervoltage Lockout (+) vs. Temperature

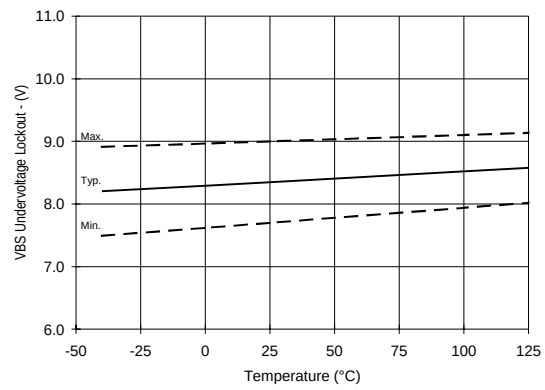


Figure 28. V_{BS} Undervoltage Lockout (-) vs. Temperature

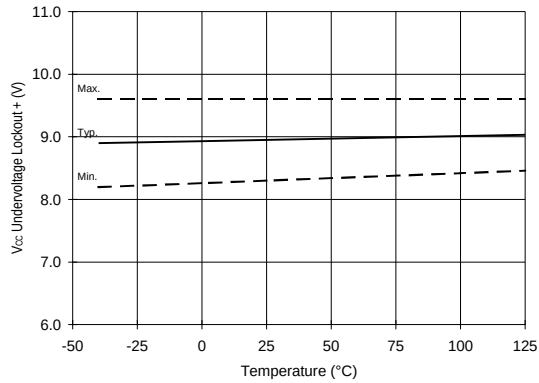


Figure 29. V_{CC} Undervoltage (+) vs. Temperature

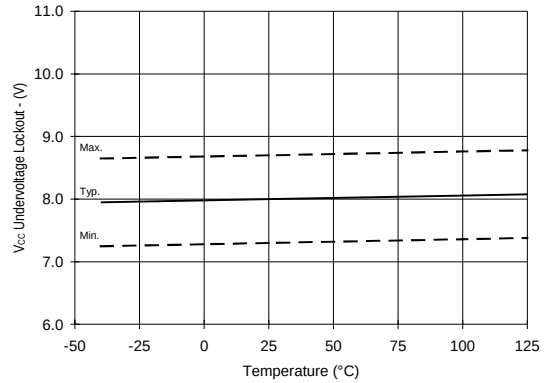


Figure 30. V_{CC} Undervoltage (-) vs. Temperature

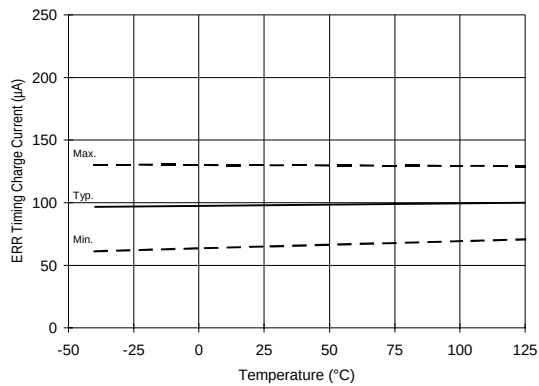


Figure 31A. ERR Timing Charge Current vs. Temperature

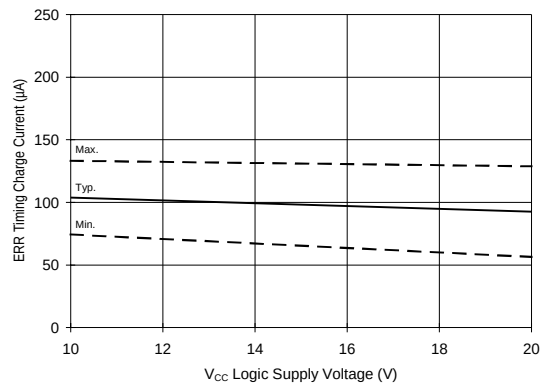


Figure 31B. ERR Timing Charge Current vs. Voltage

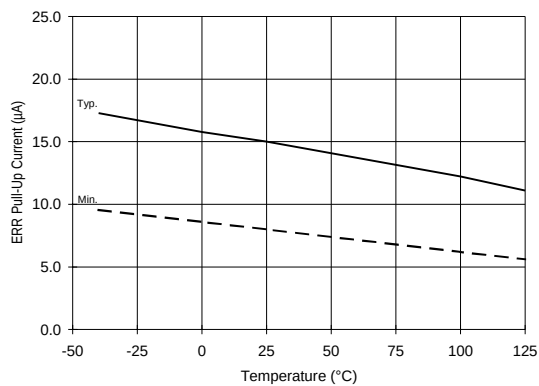


Figure 32A. ERR Pull-Up Current vs. Temperature

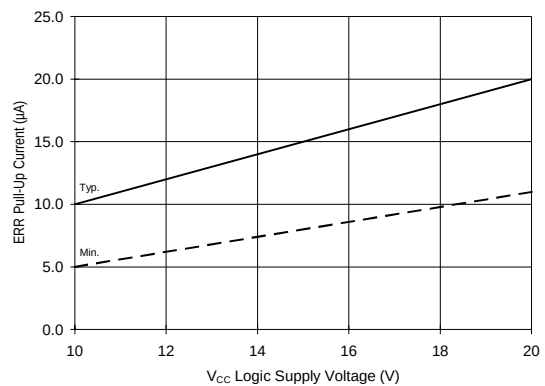


Figure 32B. ERR Pull-Up Current vs. Voltage

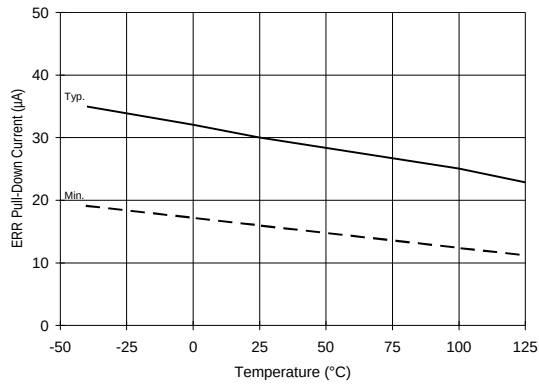


Figure 33A. ERR Pull-Down Current vs. Temperature

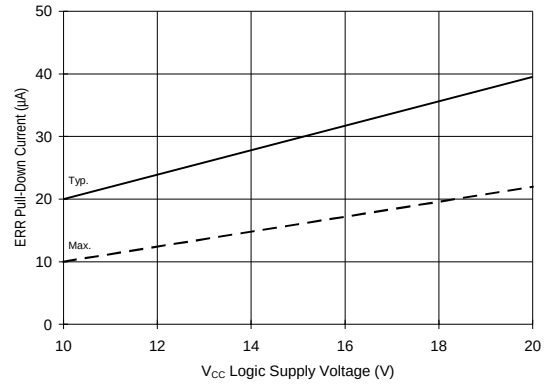


Figure 33B. ERR Pull-Down Current vs. Voltage

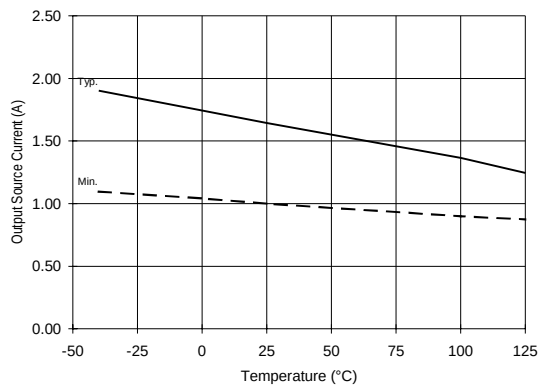


Figure 34A. Output Source Current vs. Temperature

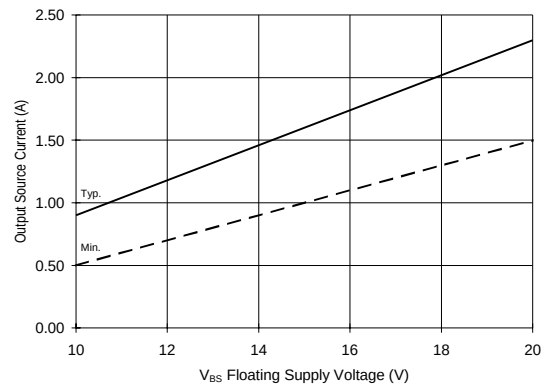


Figure 34B. Output Source Current vs. Voltage

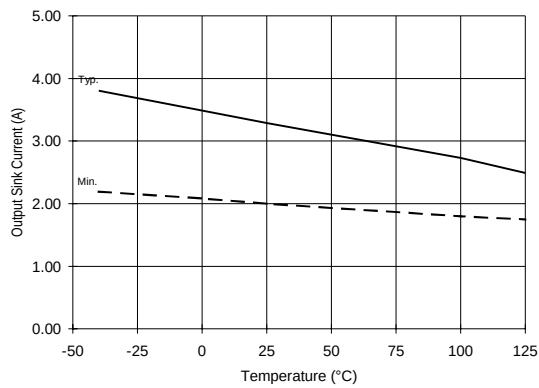


Figure 35A. Output Sink Current vs. Temperature

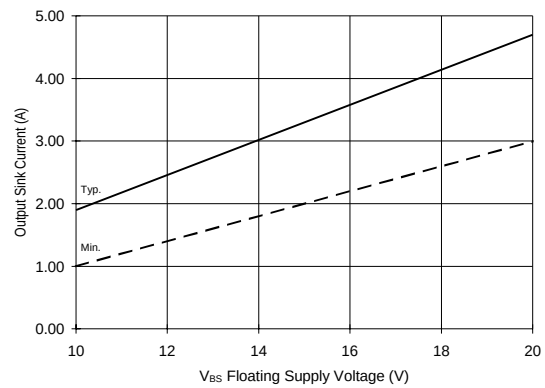


Figure 35B. Output Sink Current vs. Voltage

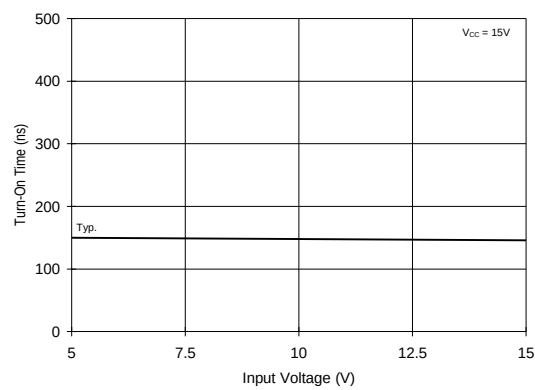


Figure 36A. Turn-On Time vs. Input Voltage

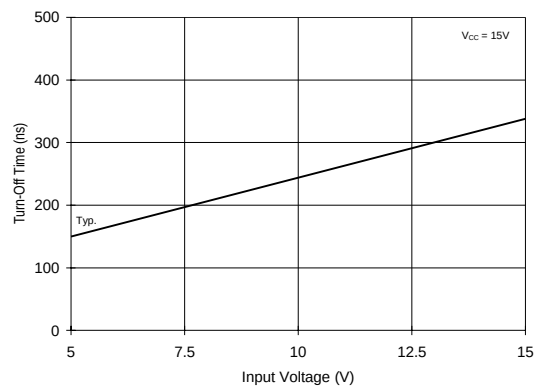


Figure 36B. Turn-Off Time vs. Input Voltage

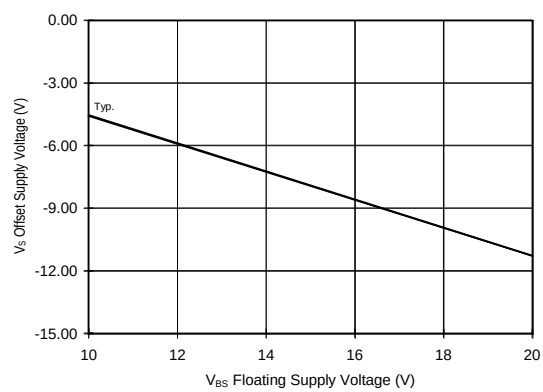


Figure 37. Maximum V_S Negative Offset vs. Supply Voltage

[illegible]

Symbol	Description
V _{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO
ERR	Serves multiple functions; status reporting, linear mode timing and cycle by cycle logic shutdown
COM	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
CS	Current sense input to current sense comparator

International
IOR Rectifier

LEAD ASSIGNMENTS

Pin	IR2153Z	IR2153Z
8	V _B	V _B
7	OUT	HO
6	CS	V _S
5	V _S	LO
1	V _{CC}	V _{CC}
2	IN	R _T
3	ERR	C _T
4	V _{SS}	COM

NOTES:

- DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AA.

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Data and specifications subject to change without notice. 05/01