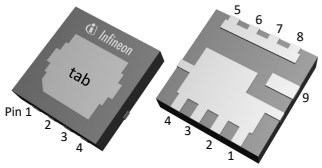
MOSFET

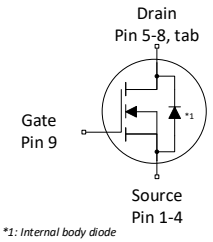
PG-WHTFN-9 (3x3)

OptiMOS™ 5 Power-Transistor, 80 V



Features

- Optimized for high performance SMPS, e.g. synchronous rectification
- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$@10V	4.6	mΩ
$R_{DS(on),max}$@4.5V	5.9	mΩ
I_D	99	A
Q_{oss}	39	nC
Q_G (0V...4.5V)	19	nC

Part number	Package	Marking	Related links
IQE046N08LM5CGSC	PG-WHTFN-9	R	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	99	A	V_{GS}=10 V, T_C=25 °C
				70		V_{GS}=10 V, T_C=100 °C
				62		V_{GS}=4.5 V, T_C=100 °C
				15.6		V_{GS}=10 V, T_A=25°C, R_{thJA}=60°C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	396	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	170	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	100	W	T_C=25 °C
				2.5		T_A=25 °C, R_{thJA}=60 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.9	1.5	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		0.7	-		
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5)]	R_{thJA}		-	60		

[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	V_{DS}=V_{GS}, I_D=47 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	4.0	4.6	mΩ	V_{GS}=10 V, I_D=20 A
			5.2	5.9		V_{GS}=4.5 V, I_D=10 A
Gate resistance	R_G	-	0.6	0.9	Ω	-
Transconductance [6]	g_{fs}	-	62	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=20 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	2500	3250	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance [7]	C_{oss}		390	507		
Reverse transfer capacitance [7]	C_{rss}		26	47		
Turn-on delay time	$t_{d(on)}$	-	5.2	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		2.6			
Turn-off delay time	$t_{d(off)}$		18			
Fall time	t_f		4.4			

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$		4.3	-	nC	
Gate to drain charge [9)]	Q_{gd}		6.4	9.6	nC	
Switching charge	Q_{sw}		9.1	-	nC	
Gate charge total [9)]	Q_g		19	24	nC	
Gate plateau voltage	$V_{plateau}$		2.8	-	V	
Gate charge total	Q_g	-	38	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	39	51	nC	V_{DS}=40 V, V_{GS}=0 V

[8)] See "Gate charge waveforms" for parameter definition

[9)] Defined by design. Not subject to production test.

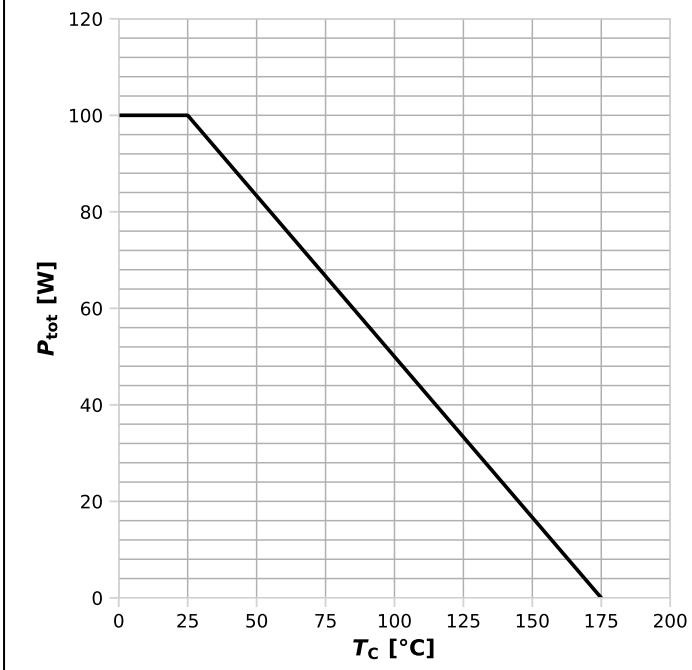
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	83	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			396		
Diode forward voltage	V_{SD}	-	0.83	1.0	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	32	64	ns	V_R=40 V, I_F=20 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}		26	52	nC	
Reverse recovery time [10)]	t_{rr}	-	18	36	ns	V_R=40 V, I_F=20 A, di_F/dt=1000 A/µs
Reverse recovery charge [10)]	Q_{rr}		129	258	nC	

[10)] Defined by design. Not subject to production test.

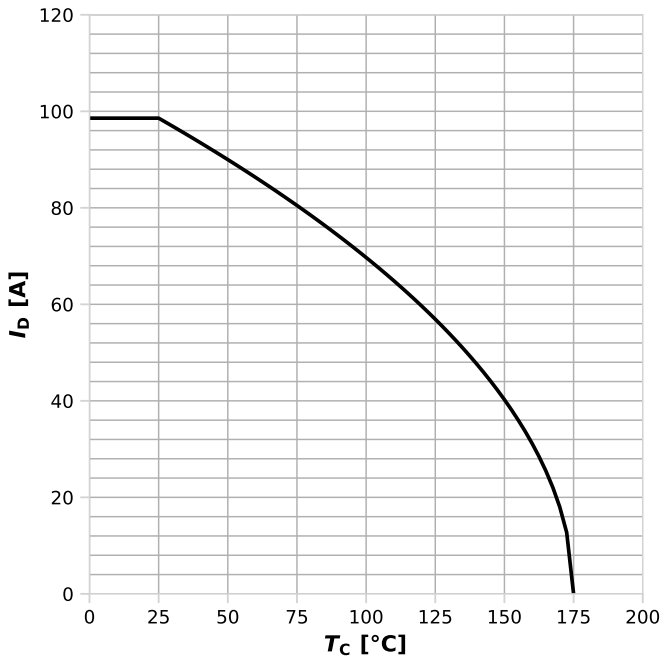
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



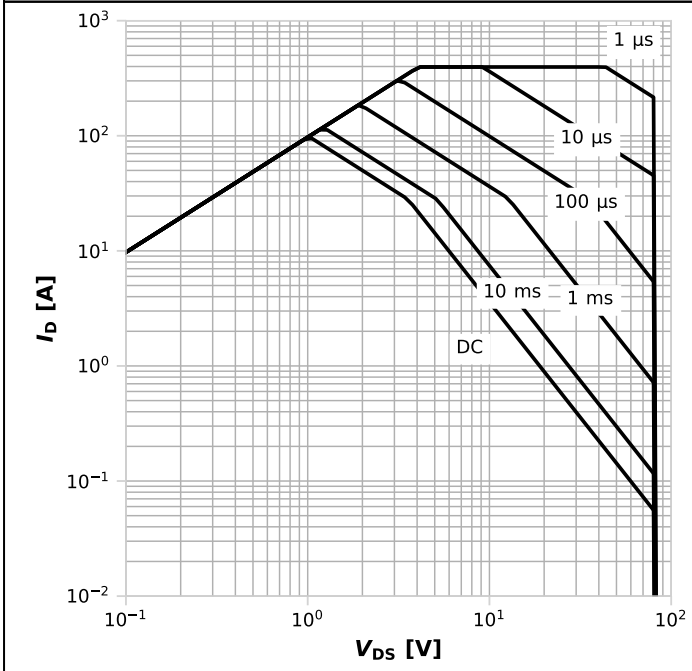
P_{tot}=f(T_C)

Diagram 2: Drain current



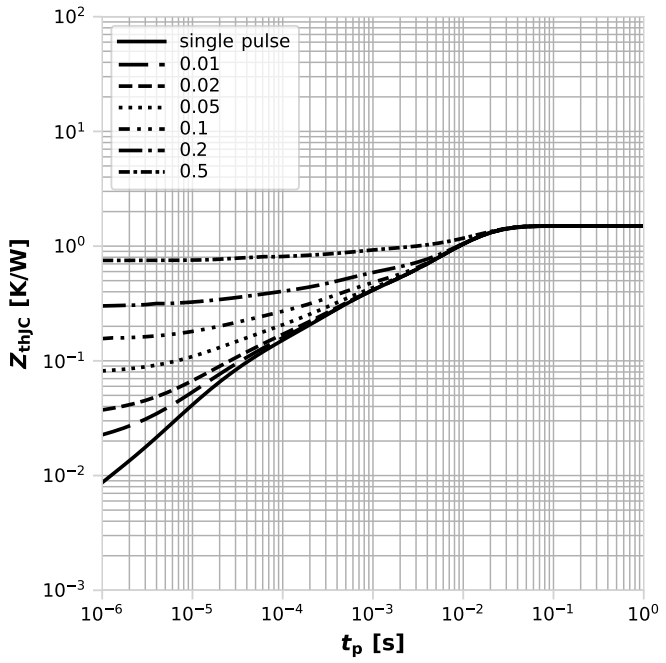
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



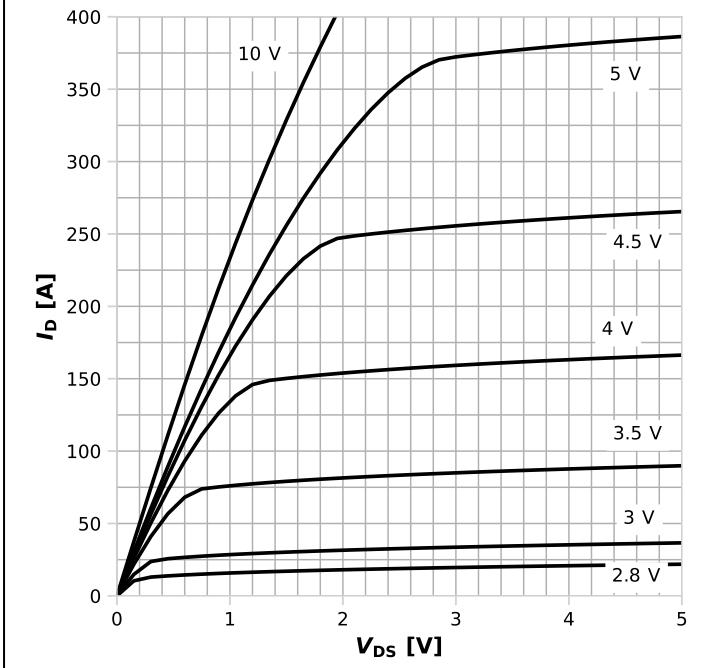
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



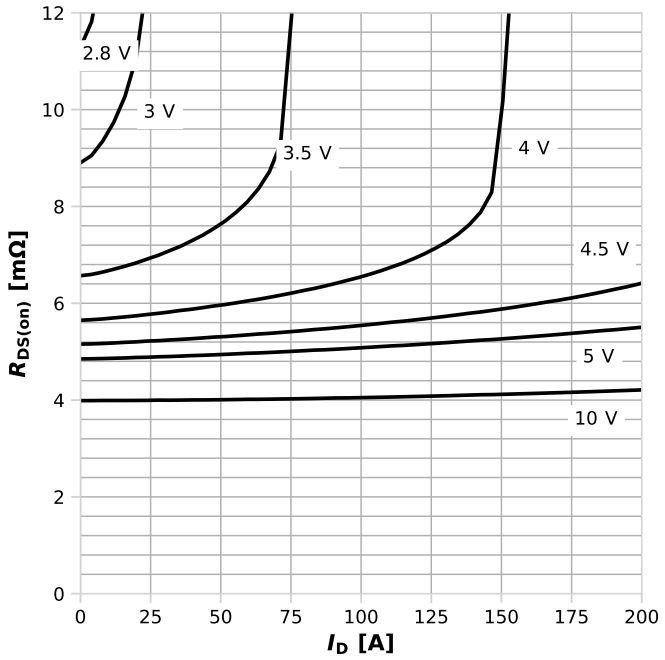
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



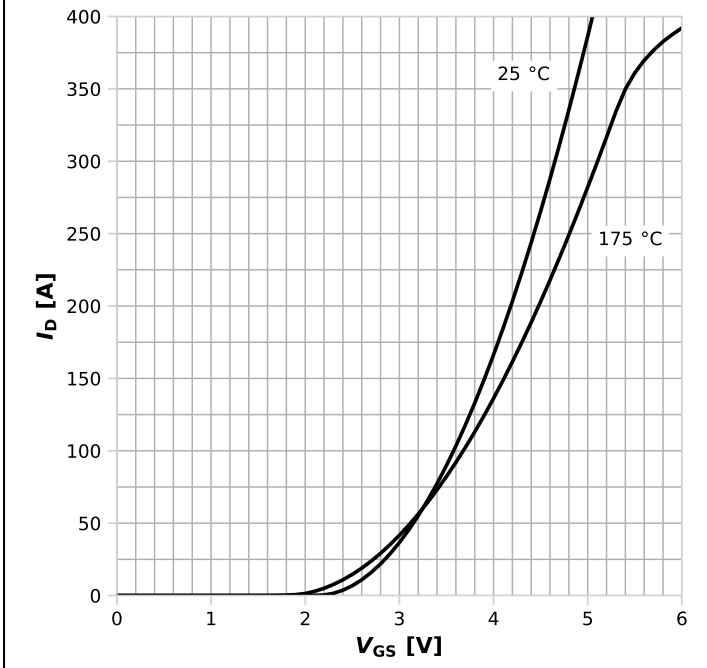
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



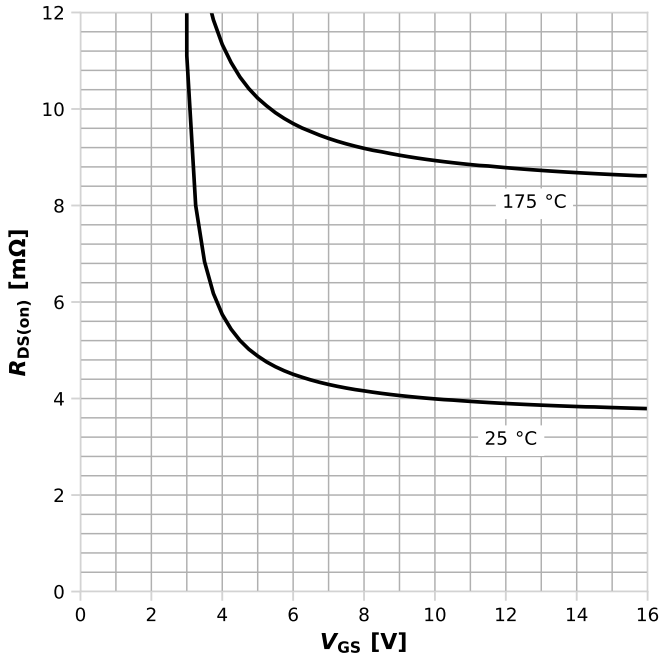
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



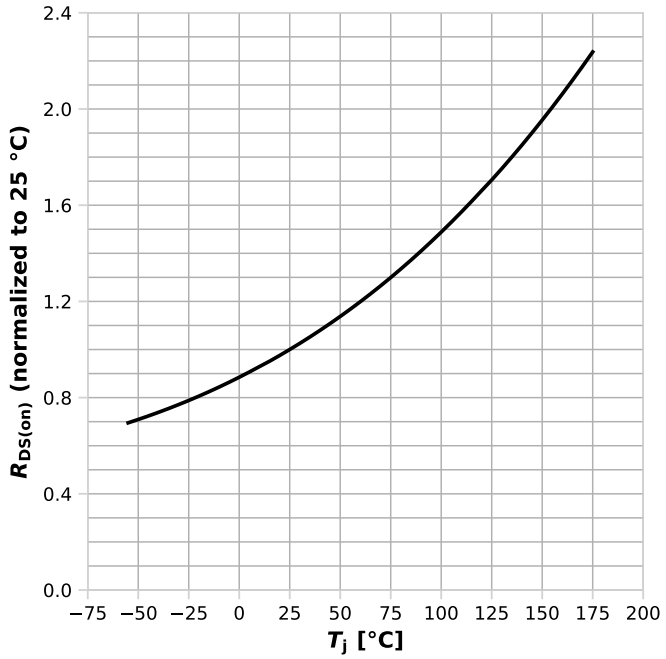
I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



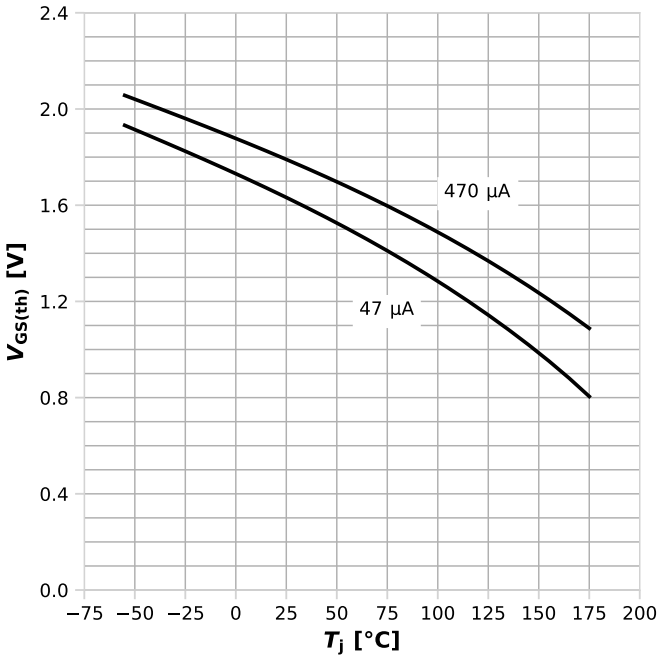
$R_{DS(on)}$=f(V_{GS}), I_D=20 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



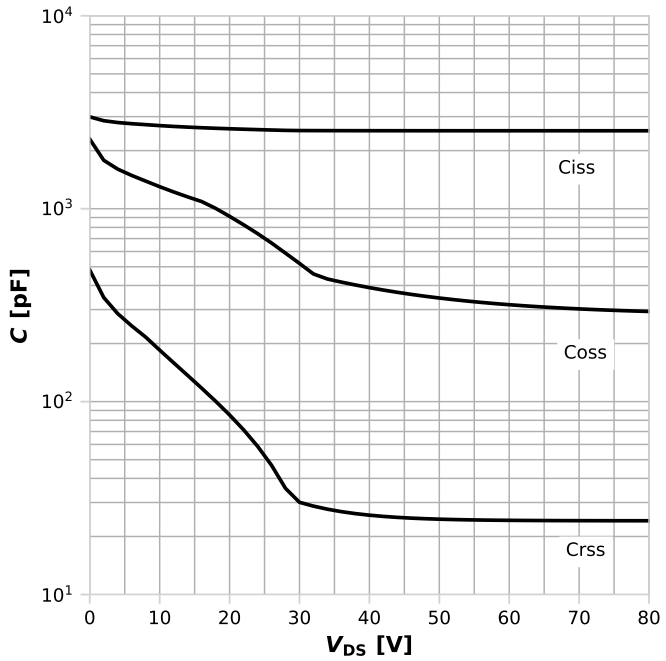
$R_{DS(on)}$=f(T_j), I_D=20 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



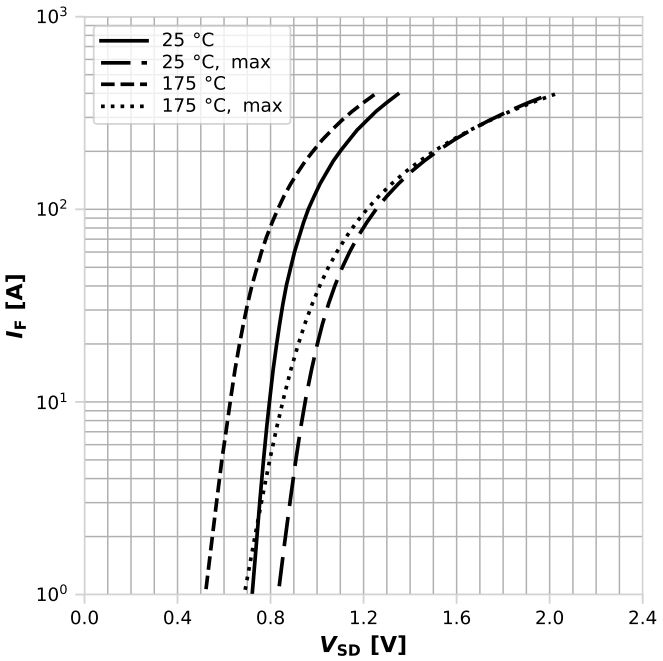
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

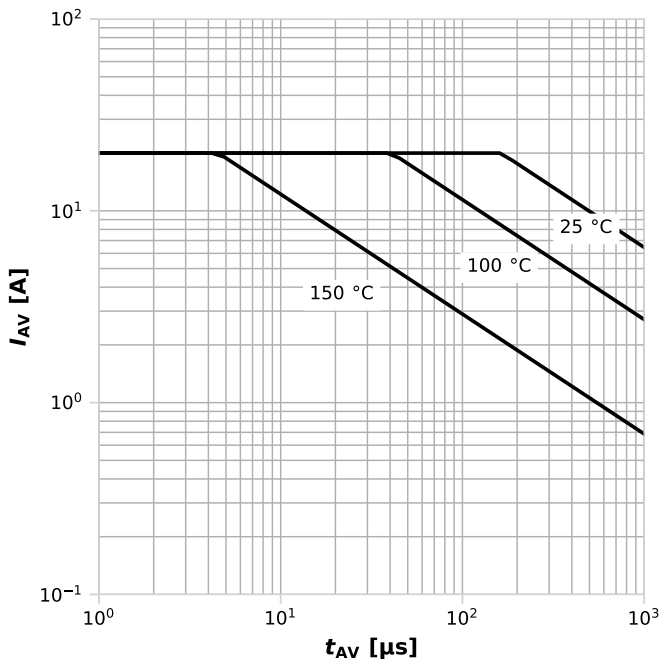
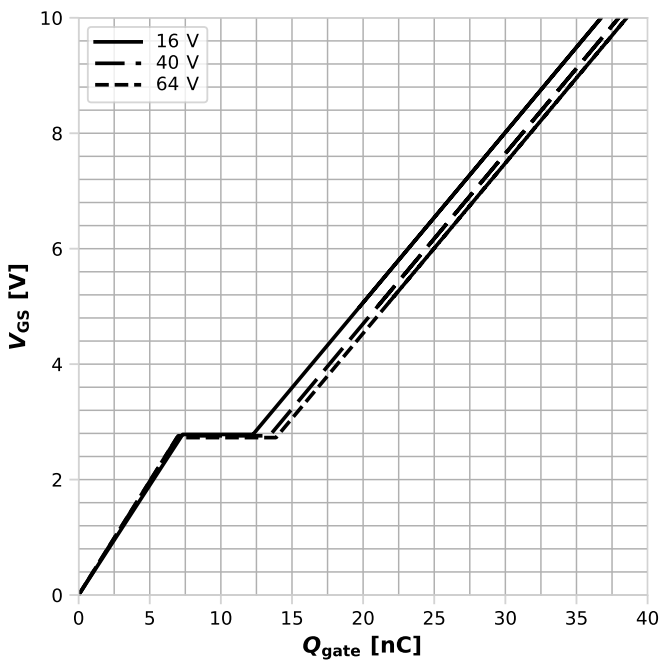
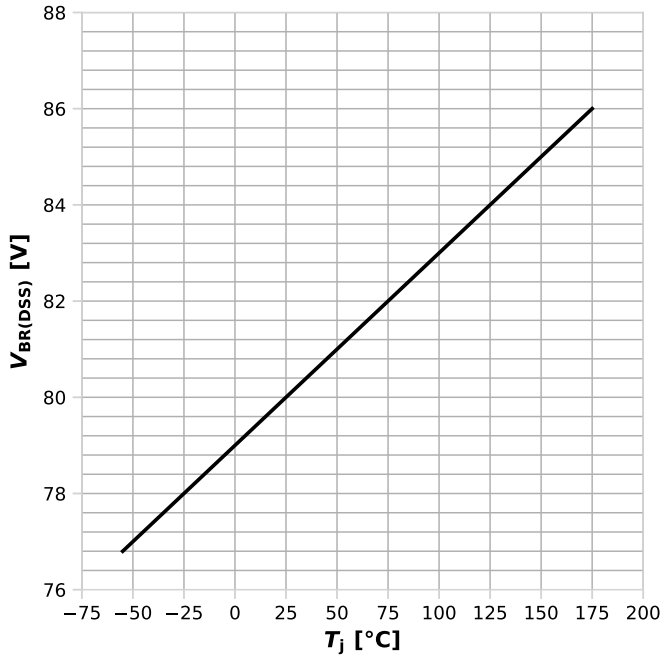
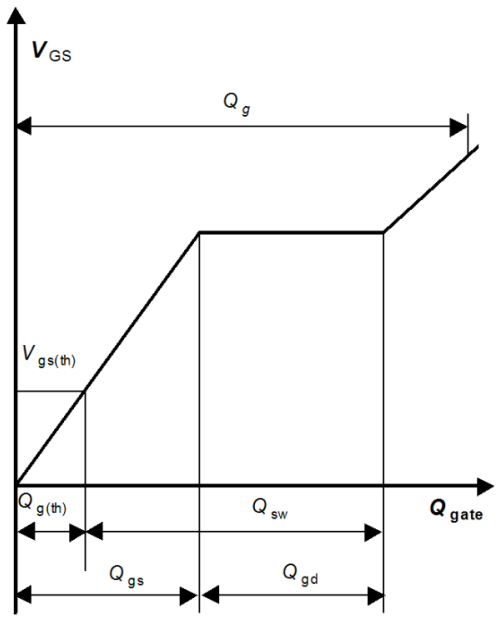
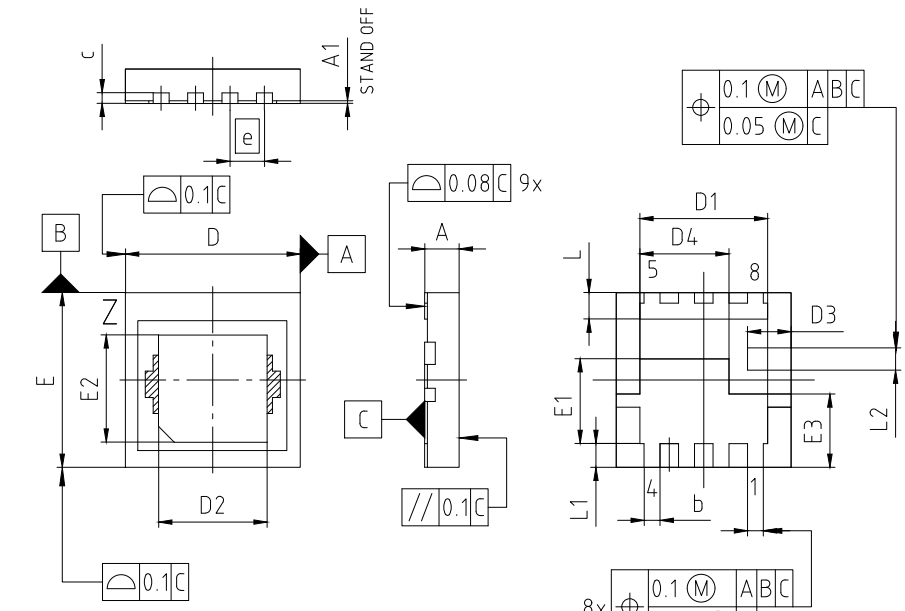
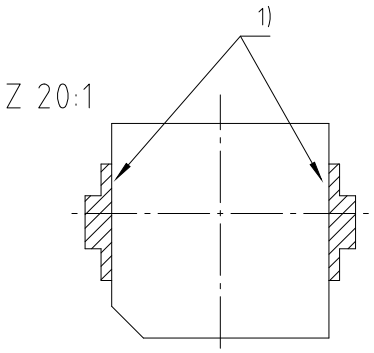
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=20 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-WHTFN-9-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.55	0.75
A1	0	0.05
b	0.20	0.40
c	0.10	0.30
D	3.20	3.40
D1	2.31	2.51
D2	1.95	2.25
D3	0.73	0.93
D4	1.58	1.78
E	3.20	3.40
E1	1.50	1.70
E2	1.93	2.23
E3	1.285	1.485
e	0.65	
L	0.40	0.60
L1	0.35	0.55
L2	0.32	0.52



1) NOT PART OF SPECIFIED HEATSINK AREA -
SHAPE MIGHT VARY DEPENDING ON HEATSINK DESIGN

Figure 1 Outline PG-WHTFN-9, dimensions in mm

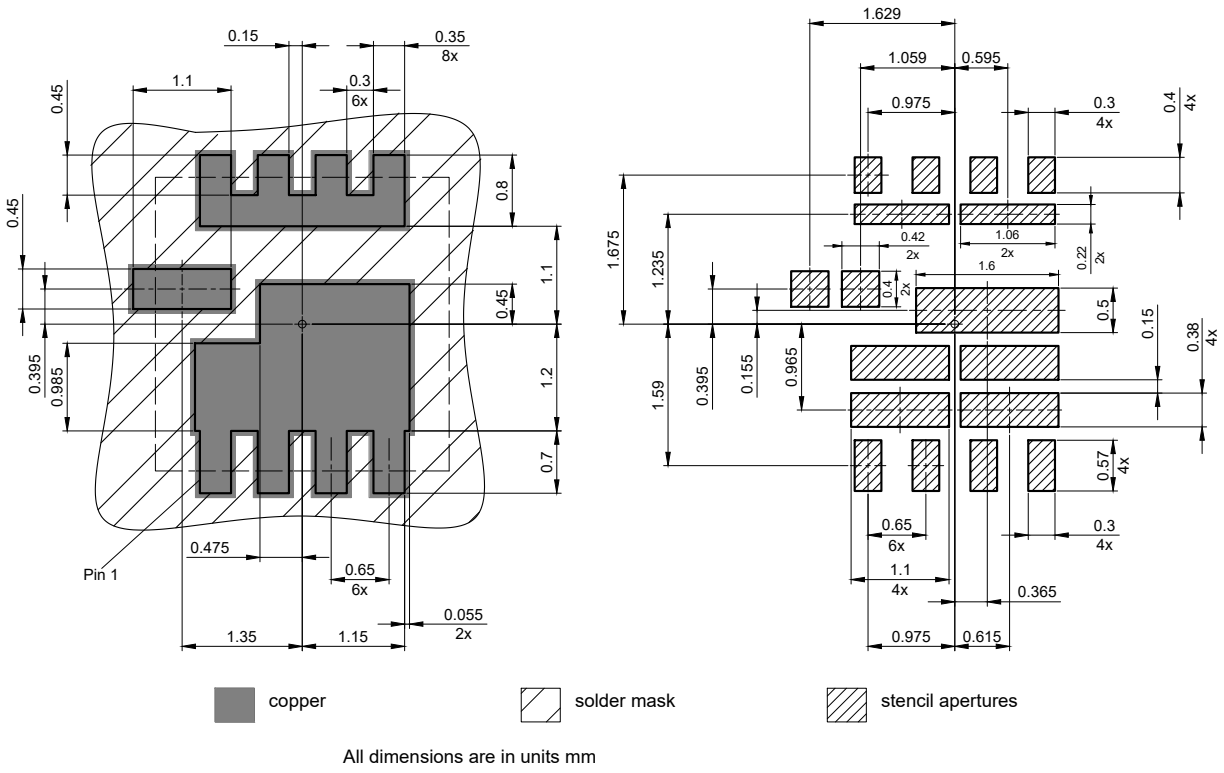


Figure 2 Footprint drawing PG-WHTFN-9, dimensions in mm

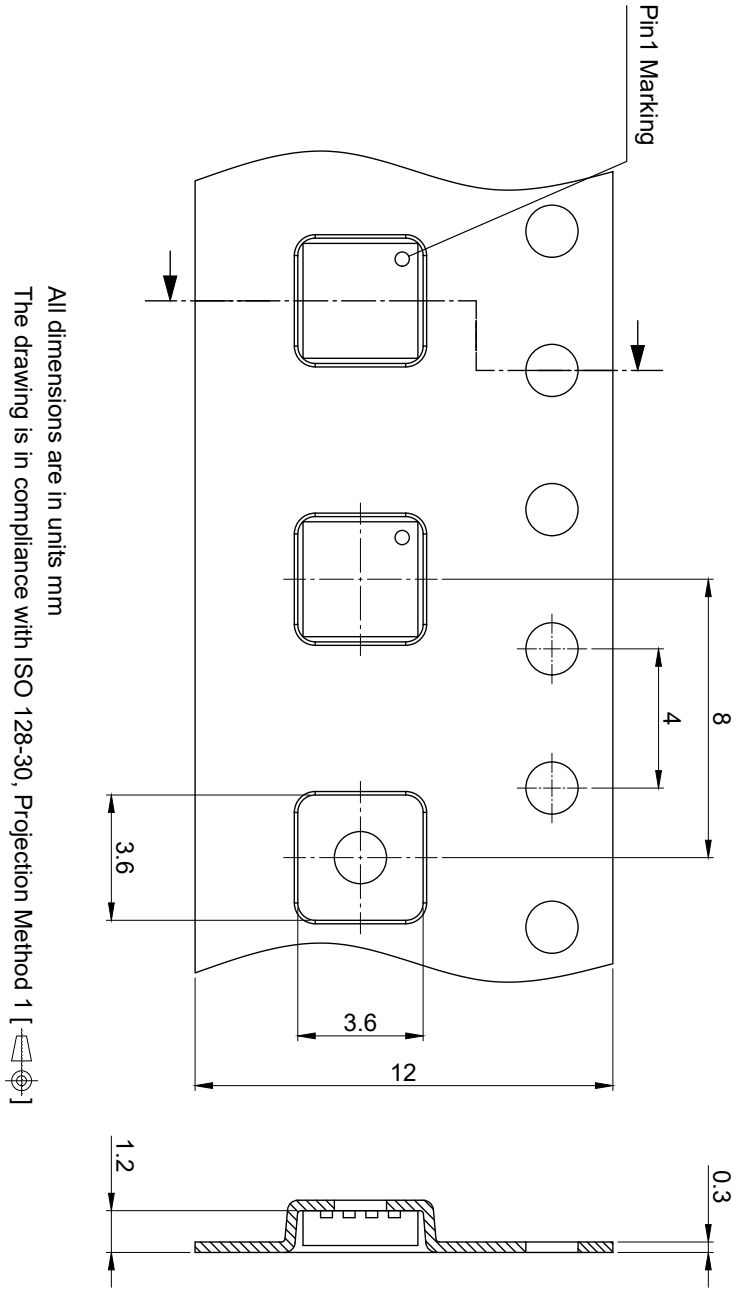


Figure 3 Packaging variant PG-WHTFN-9, dimensions in mm

Revision history

IQE046N08LM5CGSC

Revision 2025-03-04, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2023-01-12	Release of final version
2.1	2025-03-04	Updated POD with latest PG-WHTFN-9-1 Package

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