

OptiMOS™ -5 Power-Transistor



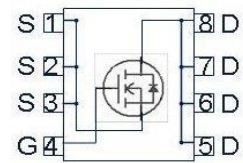
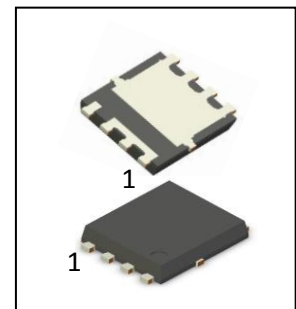
Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	4.2	mΩ
I_D	70	A

PG-TDSON-8-33



Type	Package	Marking
IPC70N04S5L-4R2	PG-TDSON-8-33	5N04L4R2

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	70	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}$ ²⁾	53	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	280	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=35\text{ A}$	32	mJ
Avalanche current, single pulse ⁴⁾	I_{AS}	-	70	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	50	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	3.0	K/W
Thermal resistance, junction - ambient	R_{thJA}	6 cm ² cooling area ³⁾	-	-	50	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=17\mu A$	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=35A$	-	4.4	6.1	m Ω
		$V_{GS}=10V, I_D=35A$	-	3.4	4.2	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	1230	1600	pF
Output capacitance	C_{oss}		-	280	364	
Reverse transfer capacitance	C_{rss}		-	20	30	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=70A, R_{G,ext}=3.5\Omega$	-	3	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	11	-	
Fall time	t_f		-	6	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32V, I_D=70A,$ $V_{GS}=0 \text{ to } 10V$	-	3.5	4.6	nC
Gate to drain charge	Q_{gd}		-	4.7	7.1	
Gate charge total	Q_g		-	22	30	
Gate plateau voltage	$V_{plateau}$		-	3	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	70	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	280	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=35A,$ $T_J=25^\circ C$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20V, I_F=50A,$ $di_F/dt=100A/\mu s$	-	30	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	18	-	nC

¹⁾ Current is limited by package; with an $R_{thJC} = 3K/W$ the chip is able to carry 75A at 25°C.

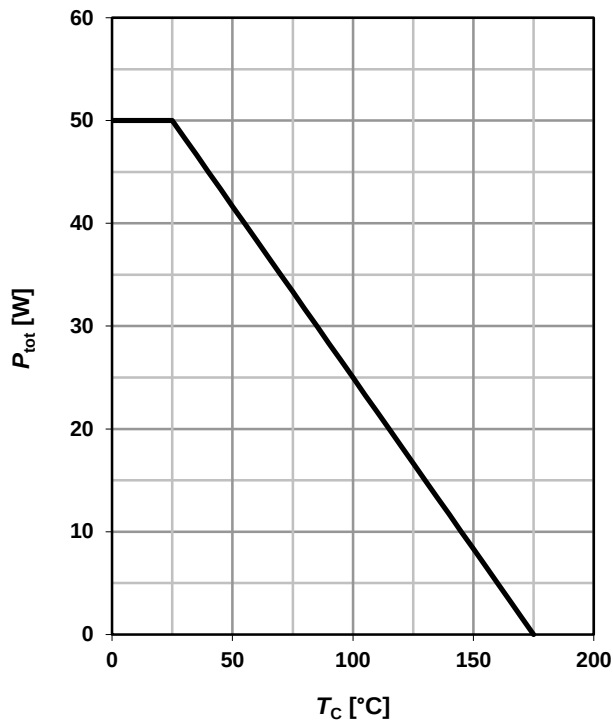
²⁾ The parameter is not subject to production test- verified by design/characterization.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ The device is tested in production with an avalanche current of 60 A.

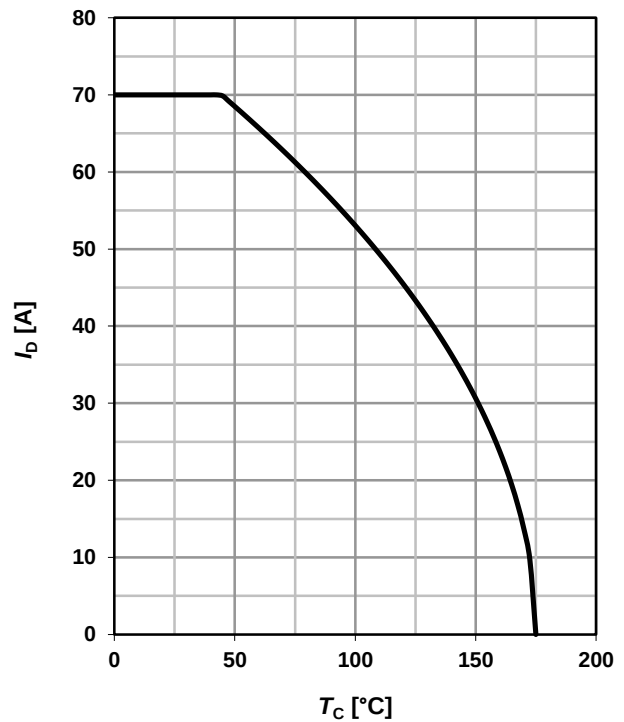
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



2 Drain current

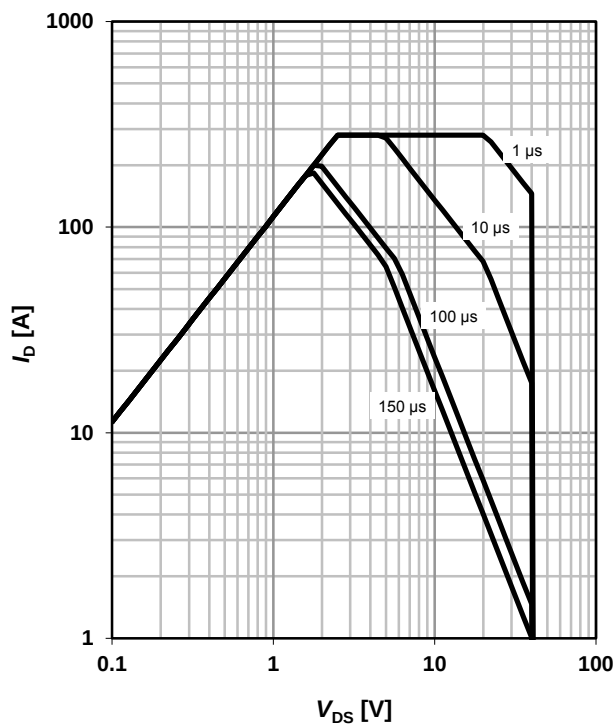
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

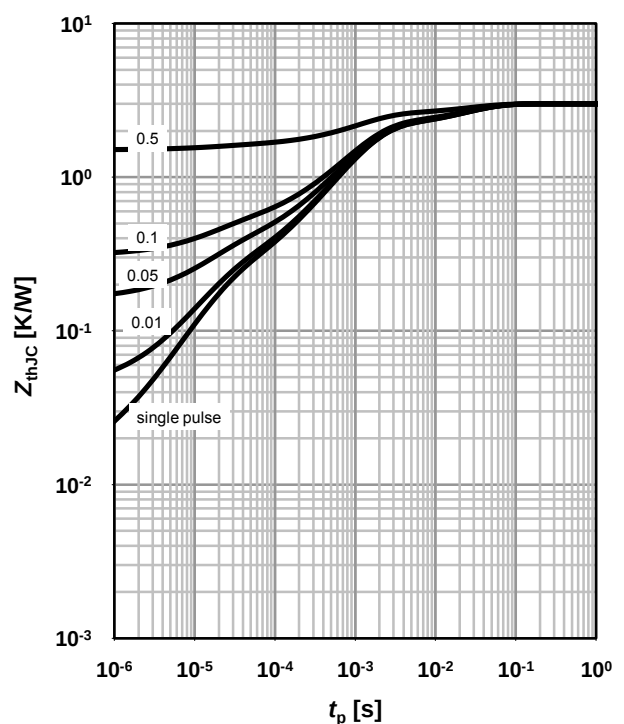
parameter: t_p



4 Max. transient thermal impedance

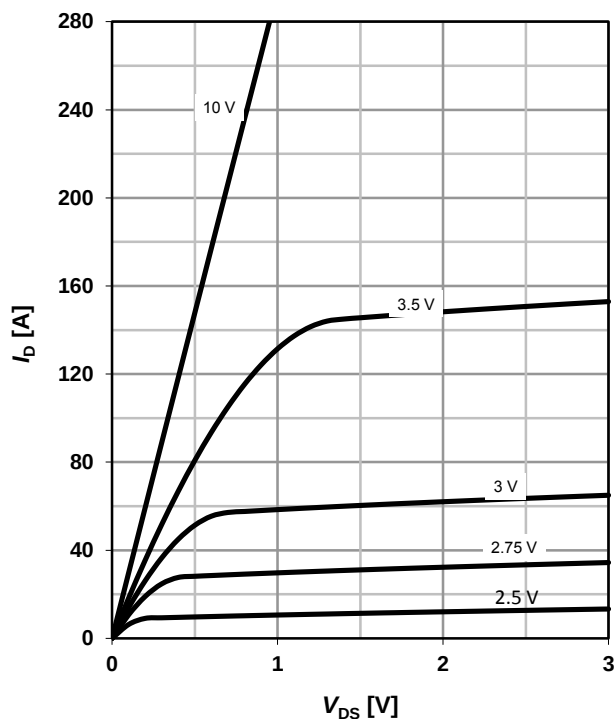
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



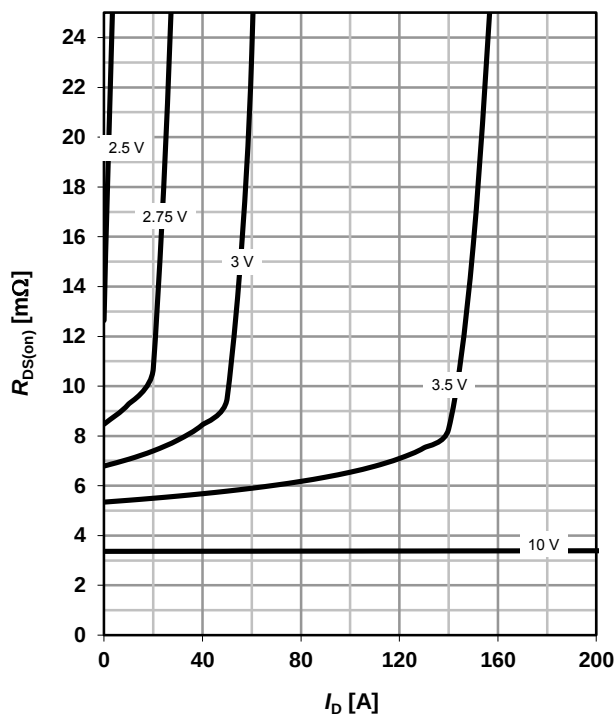
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


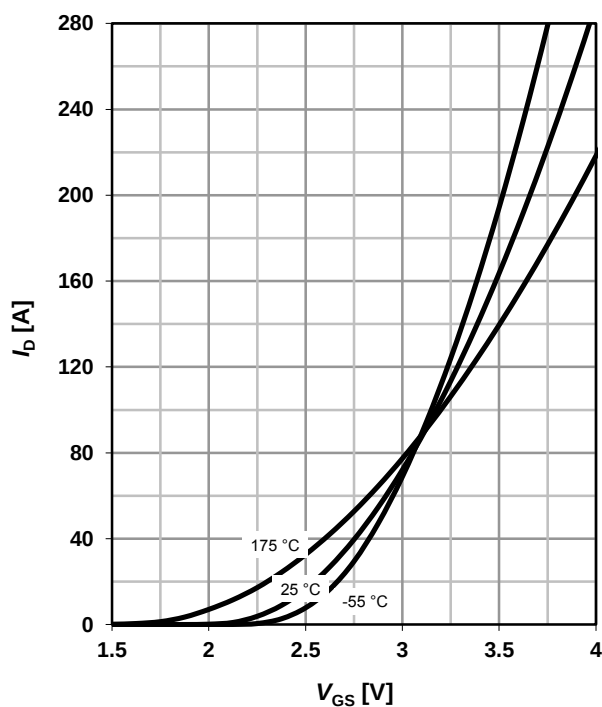
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

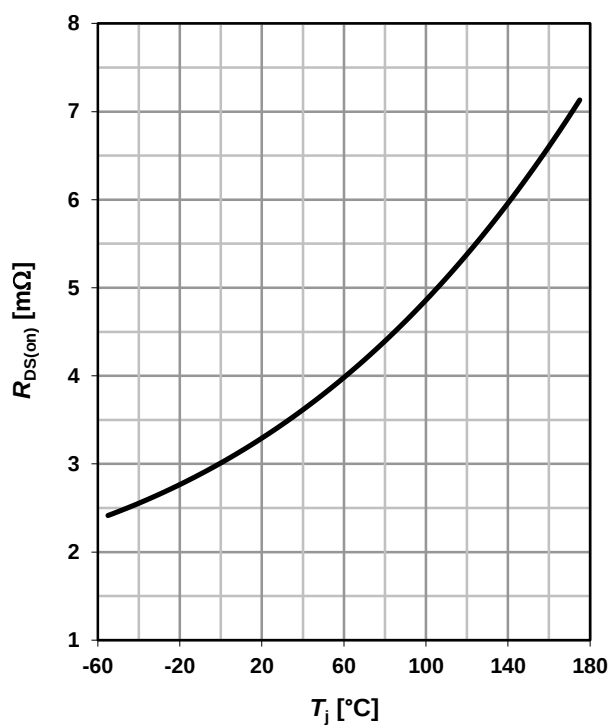
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$

parameter: T_j


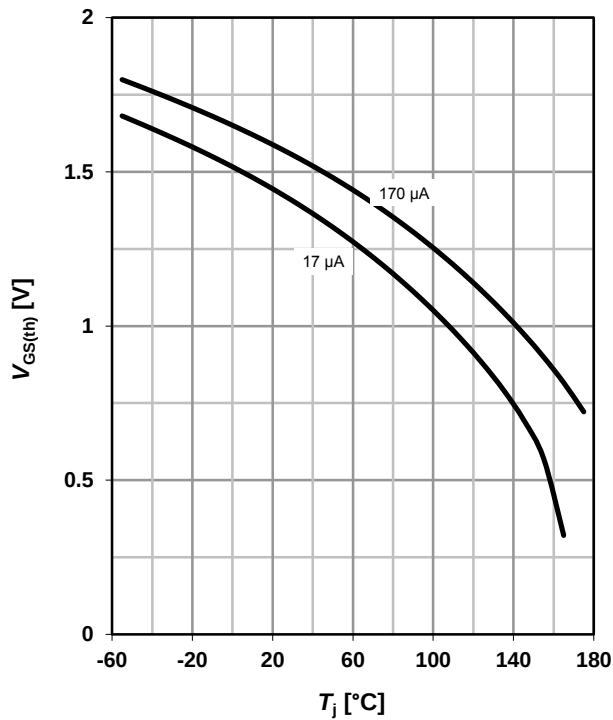
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 35\text{A}; V_{GS} = 10\text{V}$


9 Typ. gate threshold voltage

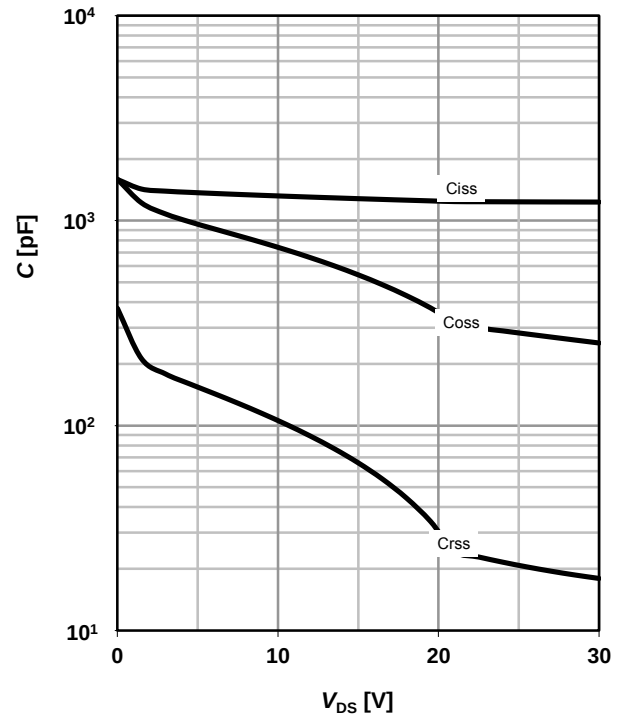
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

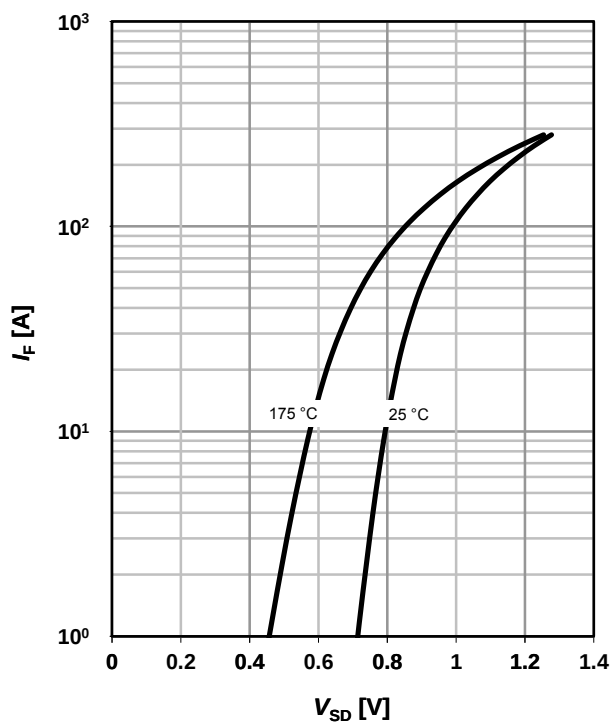
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

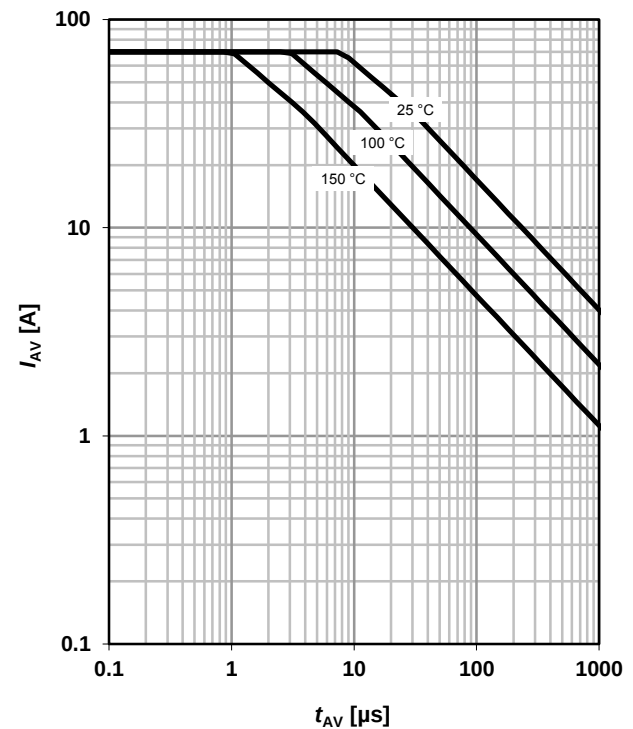
parameter: T_j



12 Avalanche characteristics

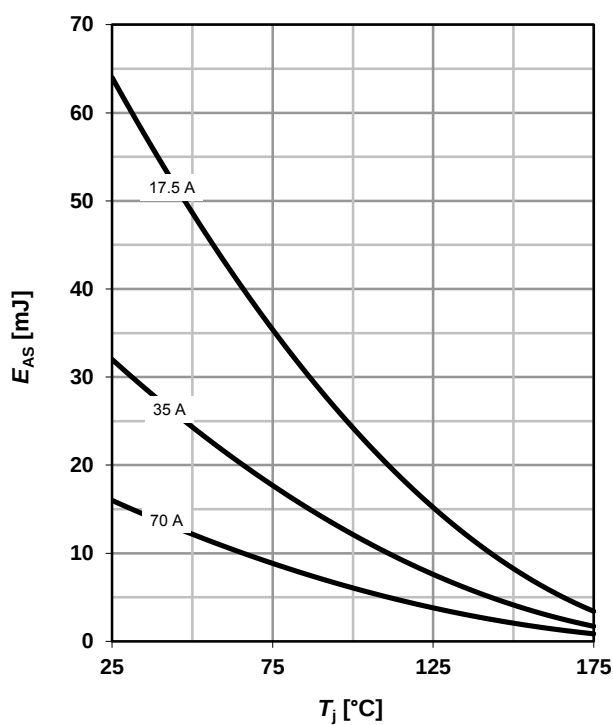
$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$



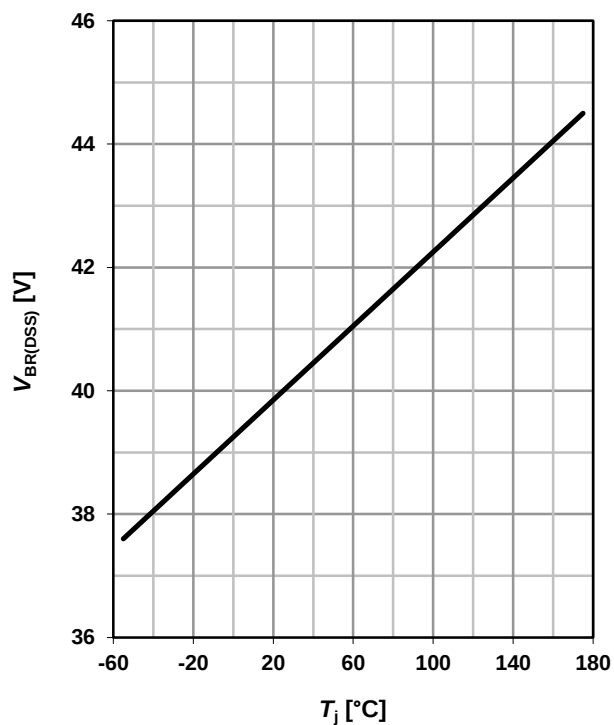
13 Avalanche energy

$$E_{AS} = f(T_j)$$



14 Drain-source breakdown voltage

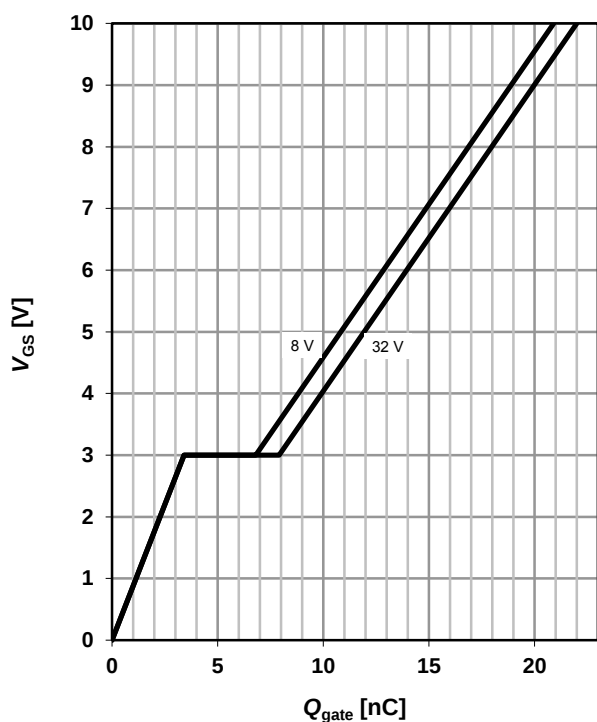
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



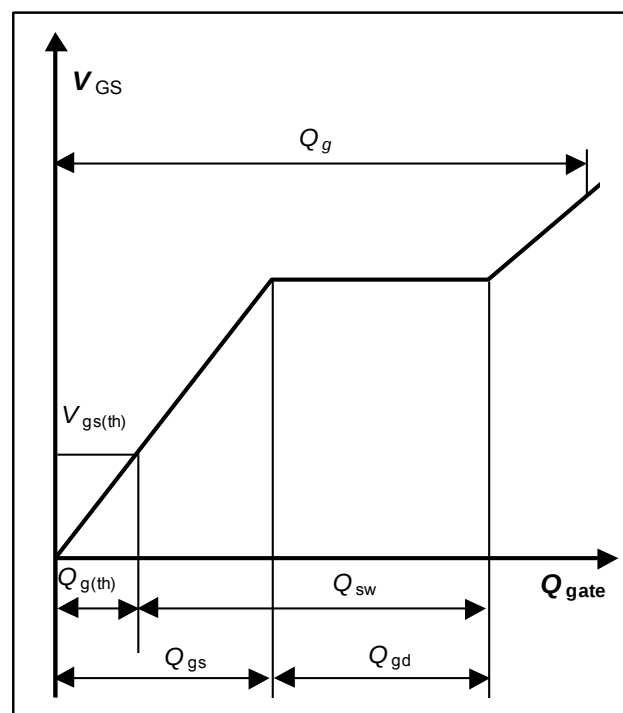
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 70 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	06.12.2016	Final Data Sheet