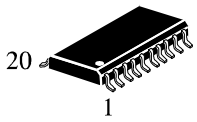
8-BIT MICROCONTROLLER WITH 2K BYTES BUILD-IN PROGRAMMABLE FLASH

Description



The IN90S2313DW is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture additionally equipped by EEPROM & analog comparators .

IC are purposed for usage in consumer devices, telecommunications, industrial control, transport and others.

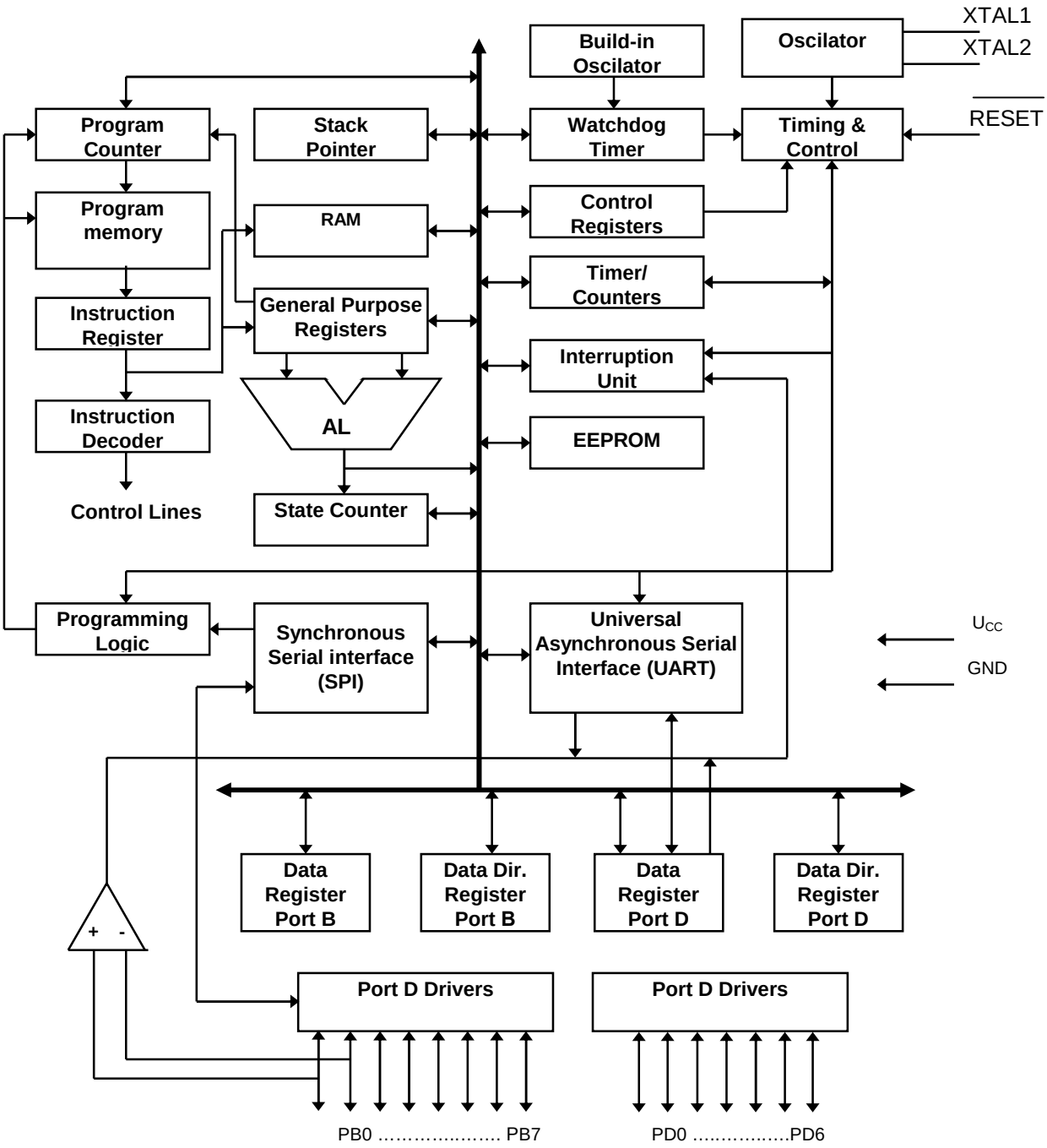
Functionally ICs is compatible to AT90S2313 (ATMEL).

ICs is assembled in SO-20 package **MS-013AC**.

Functions & features:

- Up to 1 MIPS performance (1 million instructions per second) for 1MHz clock;
- Programm memory 2K bytes (not less 1000 Write/Erase Cycles);
- Data memory on the base of 128 byte static RAM;
- Data memory on the base of 128 byte EEPROM(not less 100000 Write/Erase Cycles);
- Programming Lock for Program and Data Security;
- 2 mode of serial programming are available:parallel by means of programmer & serial (direct) by means of Serial Interface;
- Few types of synchronization: external clock external resonator (piezoceramic or quartz);
- Low Power Idle and Power Down Modes;
- Supply voltage U_{CC} =2.7 … 6.0 B;
- Clock frequency f_C up to 10 MHz;
- Operating temperature range -40 … +85°C.

Block Diagram



Pin Description Table

Pin number	Symbol	Description
01	$\overline{\text{RESET}}$	Reset input
02	PD0/RxD	0 bit of port D I/O pin - data receiver (UART)
03	PD1/TxD	1st bit of port D I/O pin / data transmitter (UART)
04	XTAL2	Output from the inverting oscillator amplifier.
05	XTAL1	Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
06	PD2/INT0	2nd bit of port D I/O pin / external interruption 0
07	PD3/INT1	3rd bit of port D I/O pin / external interruption 1
08	PD4/T0	4th bit of port D I/O pin / timer counter input 0
09	PD5/T1	5th bit of port D I/O pin / timer counter input 1
10	GND	Common pin
11	PD6/ICP	6th bit port D I/O pin / timer counter latch
12	PB0/AIN0	0 bit of port B I/O pin / comparator positive input
13	PB1/AIN1	1st bit of port B I/O pin / comparator negative input
14	PB2	2nd bit port B I/O pin
15	PB3/OCI	3rd bit of port B I/O pin / timer counter output
16	PB4	4th bit of port B I/O pin
17	PB5/MOSI	5th bit of port B I/O pin / serial interface (SPI) data input
18	PB6/MISO	6th bit of port B I/O pin / serial interface (SPI) data output
19	PB7/SCK	7th bit of port B I/O pin / serial interface (SPI) clock input
20	U_{CC}	Supply voltage pin

Notes

1 UART – Universal Asynchronous Receiver/Transmitter

2 SPI – Serial Peripheral Interface

Maximum Ratings & Recommended Operating Conditions (Ta= -40…+85 ºC)

Parameter, unit		Symbol	Recommended operating conditions		Maximum rate	
			min	max	min	max
Supply voltage, V		**U_{CC}**	2,7	6,0	-0,3	6,6
XTAL1 pin low level input voltage, V		U_{IL1}	-0,5	0,1	-1,0	-
XTAL1 pin high level input voltage, V		U_{IH1}	$0,7U_{CC}$	U_{CC}+0,5	-	7,1
Low level input voltage (all pins except XTAL1), V		U_{IL2}	-0,5	$0,3U_{CC}$	-1,0	-
High level input voltage (all pins except XTAL1 & $\overline{\text{RESET}}$), V		U_{IH2}	$0,6U_{CC}$	U_{CC}+0,5	-	7,1
$\overline{\text{RESET}}$ pin high level input voltage, V		U_{IH3}	$0,85U_{CC}$	U_{CC}+0,5	-	13,0
PB0-PB2 pins low level input voltage, V		U_{IL1}	-0,5	$0,3U_{CC}$	-1,0	-
PB0-PB2 pins high level input voltage, V		U_{IH3}	$0,6U_{CC}$	U_{CC}+0,5	-	
Clock frequency, MHz	U_{CC}=2,7-4,0 B	f		4		
	U_{CC}=4,0-6,0 V			10		

Electric parameters

(U_{CC}= 4,0 … 6,0 V.)

Parameter, Unit	Symbol	Min	Max	Mode	Ambient temperature
Low level output voltage, V -ports B, D	U_{OL}	-	0,6	U_{CC}=5 V I_{OL}=20 mA	25±10 –40…85
	U_{OL1}	-	0,5	U_{CC}=3 V I_{OL}=10 mA	
High level output voltage, V - ports B, D	U_{OH}	4,3	-	U_{CC}=5 V I_{OH}= -3 mA	
	U_{OH1}	2,3		U_{CC}=3 V I_{OH}= -1,5 mA	
Low level input current, μA - ports B, D	I_{IL}	-	| –1,5 |	U_{CC}=6 V U_{IN}=0 V	
High level input current, μA - ports B, D	I_{IH}	-	980	U_{CC}=6 V U_{IN}=U_{CC}	
$\overline{\text{RESET}}$ pin resistance , kOhm	R_{RST}	100	500	U_{CC}=5 V	
PB0-PB2 pin resistance, kOhm	$R_{I/O}$	35	120	U_{CC}=5 V	
Comparator input current nA	I_{ACLK}		|±50|	U_{CC}=5 V U_{IN}=U_{CC} or U_{IN}=0V	
Active mode dynamic consumption current, mA	I_{CCO}	-	3,0	U_{CC}=3 V f_C=4 MHz	
Idle mode consumption current, mA	I_{CCOS}	-	1,0	U_{CC}=3 V f_C=4 MHz	
Power Down Mode with watchdog consumption current, μA	I_{CC1}	-	15.0	U_{CC}=3 V	
Power Down Mode without watchdog consumption current, μA	I_{CC2}	-	2.0	U_{CC}=3 V	
Comparator input bias voltage, mV	U_{ACIO}	-	40	U_{CC}=5.0 V U_{IN}= U_{CC}/2±20 mV	
Comparator delay, ns	t_{ACPD}	-	500	U_{CC}=4.0 V	
	t_{ACPD1}	-	750	U_{CC}=2.7 V	

Instruction Set Summary

Logic instructions

N°	Mnemonics	Descriptrion	Operation	Clock	Flags
1	AND Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	1	Z,N,V,S
2	ANDI Rd, K	Logical AND Register and Constant	Rd ← Rd • K	1	Z,N,V,S
3	EOR Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	1	Z,N,V,S
4	OR Rd, Rr	Logical OR Registers	Rd ← Rd ∨ Rr	1	Z,N,V,S
5	ORI Rd, K	Logical OR Register and Constant	Rd ← Rd ∨ K	1	Z,N,V,S
6	COM Rd	One's Complement	Rd ←$FF - Rd	1	Z,C,N,V,S
7	NEG Rd	Two's Complement	Rd ←$00 - Rd	1	Z,C,N,V,H,S
8	CLR Rd	Clear Register	Rd ← Rd ⊕ Rd	1	Z,N,V,S
9	SER Rd	Set Register	Rd ←$FF	1	—
10	TST Rd	Test for Zero or Minus	Rd • Rd	1	Z,N,V,S
11	SWAP Rd	Swap Nibbles in GPR	Rd (3..0) ← Rd (7..4), Rd (7..4) ← Rd (3..0)	1	—

Arithmetic instructions

N°	Mnemonics	Descriptrion	Operation	Clock	Flags
1	ADD Rd, Rr	Add two Registers	Rd ← Rd + Rr	1	Z,C,N,V,H,S
2	ADC Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	1	Z,C,N,V,H,S
3	ADIW Rd, K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	2	Z,C,N,V,S
4	SUB Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	1	Z,C,N,V,H,S
5	SUBI Rd, K	Subtract Constant from Register	Rd ← Rd - K	1	Z,C,N,V,H,S
6	SBC Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	1	Z,C,N,V,H,S
7	SBCI Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	1	Z,C,N,V,H,S
8	SBIW Rd, K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	2	Z,C,N,V,S
9	DEC Rd	Decrement of GPR	Rd ← Rd - 1	1	Z,N,V,S
10	INC Rd	Increment of GPR	Rd ← Rd + 1	1	Z,N,V,S
11	ASR Rd	Arithmetic Shift Right	Rd (n) ← Rd (n+1), n = 0..6, Rd(7) ← Rd(7)	1	Z,C,N,V,S
12	LSL Rd	Logical Shift Left	Rd (n+1) ← Rd (n), Rd(0) ← 0	1	Z,C,N,V,H,S
13	LSR Rd	Logical Shift Right	Rd (n) ← Rd (n+1), Rd(7) ← 0	1	Z,C,N,V,S
14	ROL Rd	Rotate Left Through Carry	Rd(0) ← C, Rd (n+1) ← Rd (n), C ← Rd (7)	1	Z,C,N,V,H,S
15	ROR Rd	Rotate Right Through Carry	Rd(7) ← C, Rd (n) ← Rd (n+1), C ← Rd (0)	1	Z,C,N,V,S

Bit operations instructions

N°	Mnemonics	Descriptrion	Operation	Clock	Flags
1	CBR Rd, K	Clear Bit(s) in GPR	Rd ← Rd • ($FF - K)	1	Z,N,V,S
2	SBR Rd, K	Set Bit(s) in GPR	Rd ← Rd ∨ K	1	Z,N,V,S
3	CBI A, b	Clear Bit in I/O Register	A.b ← 0	2	—
4	SBI A, b	Set Bit in I/O Register	A.b ← 1	2	—
5	BCLR s	Flag Clear	SREG.s ← 0	1	SREG.s
6	BSET s	Flag Set	SREG.s ← 1	1	SREG.s
7	BLD Rd, b	Bit load from flag T (SPEG) to GPR	Rd.b ← T	1	—
8	BST Rr, b	Bit store from flag T (SPEG) to GPR	T ← Rd.b	1	T
9	CLC	Clear Carry	C ← 0	1	C
10	SEC	Set Carry	C ← 1	1	C
11	CLN	Clear Negative Flag	N ← 0	1	N
12	SEN	Set Negative Flag	N ← 1	1	N
13	CLZ	Clear Zero Flag	Z ← 0	1	Z
14	SEZ	Set Zero Flag	Z ← 1	1	Z
15	CLI	Global Interrupt Disable	I ← 0	1	I
16	SEI	Global Interrupt Enable	I ← 1	1	I
17	CLS	Clear Signed Test Flag	S ← 0	1	S
18	SES	Set Signed Test Flag	S ← 1	1	S
19	CLV	Clear Twos Complement Overflow	V ← 0	1	V
20	SEV	Set Twos Complement Overflow	V ← 1	1	V
21	CLT	Clear T in SREG	T ← 0	1	T
22	SET	Set T in SREG	T ← 1	1	T
23	CLH	Clear Half Carry Flag in SREG	H ← 0	1	H
24	SEH	Set Half Carry Flag in SREG	H ← 1	1	H

Data transfer instructions

N°	Mnemonics	Descriptrion	Operation	Clock	Flags
1	MOV Rd, Rr	Move Between GPR	Rd ← Rr	1	—
2	LDI Rd, K	Load Immediate	Rd ← K	1	—
3	LD Rd, X	Load Indirect	Rd ← [X]	2	—
4	LD Rd, X+	Load Indirect and Post-Inc.	Rd ← [X], X ← X+1	2	—
5	LD Rd, -X	Load Indirect and Pre-Dec.	X ← X-1, Rd ← [X]	2	—
6	LD Rd, Y	Load Indirect	Rd ← [Y]	2	—
7	LD Rd, Y+	Load Indirect and Post-Inc.	Rd ← [Y], Y ← Y+1	2	—
8	LD Rd, -Y	Load Indirect and Pre-Dec.	Y ← Y-1, Rd ← [Y]	2	—
9	LDD Rd, Y+q	Load Indirect with Displacement	Rd ← [Y+q]	2	—
10	LD Rd, Z	Load Indirect	Rd ← [Z]	2	—
11	LD Rd, Z+	Load Indirect and Post-Inc.	Rd ← [Z], Z ← Z+1	2	—
12	LD Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z-1, Rd ← [Z]	2	—
13	LDD Rd, Z+q	Load Indirect with Displacement	Rd ← [Z+q]	2	—
14	LDS Rd, k	Load Direct from RAM	Rd ← [k]	2	—
15	ST X, Rr	Store Indirect	[X] ← Rr	2	—
16	ST X+, Rr	Store Indirect and Post-Inc.	[X] ← Rr, X ← X+1	2	—
17	ST -X, Rr	Store Indirect and Pre-Dec.	X ← X-1, [X] ← Rr	2	—
18	ST Y, Rr	Store Indirect	[Y] ← Rr	2	—
19	ST Y+, Rr	Store Indirect and Post-Inc.	[Y] ← Rr, Y ← Y+1	2	—
20	ST -Y, Rr	Store Indirect and Pre-Dec.	Y ← Y-1, [Y] ← Rr	2	—
21	STD Y+q, Rr	Store Indirect with Displacement	[Y+q] ← Rr	2	—
22	ST Z, Rr	Store Indirect	[Z] ← Rr	2	—
23	ST Z+, Rr	Store Indirect and Post-Inc.	[Z] ← Rr, Z ← Z+1	2	—
24	ST -Z, Rr	Store Indirect and Pre-Dec.	Z ← Z-1, [Z] ← Rr	2	—
25	STD Z+q, Rr	Store Indirect with Displacement	[Z+q] ← Rr	2	—
26	STS k, Rr	Store Direct to SRAM	[k] ← Rr	2	—
27	LPM	Load Program Memory	R0 ← {Z}	3	—
28	IN Rd, A	In Port	Rd ←A	1	—
29	OUT A, Rr	Out Port	A ← Rr	1	—
30	PUSH Rr	Push Register on Stack	STACK ← Rr	2	—
31	POP Rd	Pop Register from Stack	Rd ← STACK	2	—

Control transfer instructions

N°	Mnemonics	Descriptrion	Operation	Clock	Flags
1	RJMP k	Relative Jump	PC ← PC + k + 1	2	—
2	IJMP	Indirect Jump to (Z)	PC ← Z	2	—
3	RCALL	Relative Subroutine Call	PC ← PC + k + 1	3	—
4	ICALL	Indirect Call to (Z)	PC ← Z	3	—
5	RET	Subroutine Return	PC ← STACK	4	—
6	RETI	Interrupt Return	PC←STACK	4	I
7	CP Rd, Rr	Compare	Rd - Rr	1	Z,N,V,C,H,S
8	CPC Rd, Rr	Compare with Carry	Rd - Rr - C	1	Z,N,V,C,H,S
9	CPI Rd, K	Compare Register with Immediate	Rd - K	1	Z,N,V,C,H,S
10	CPSE Rd, Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	1/2/3	—
11	SBRC Rr,b	Skip if Bit in GPR Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	1/2/3	—
12	SBRS Rr,b	Skip if Bit in GPR is Set	if (Rr(b)=1) PC ← PC + 2 or 3	1/2/3	—
13	SBIC A,b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	1/2/3	—
14	SBIS A,b	Skip if Bit in I/O Register is Set	if (R(b)=1) PC ← PC + 2 or 3	1/2/3	—
15	BRBC s,k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC + k + 1	1/2	—
16	BRBS s,k	Branch if Status Flag Set	if (Z = 1) then PC ← PC + k + 1	1/2	—
17	BRCS k	Branch if Carry Set	if (Z = 0) then PC ← PC + k + 1	1/2	—
18	BRCC k	Branch if Carry Cleared	if (C = 1) then PC ← PC + k + 1	1/2	—
19	BREQ k	Branch if Equal	if (C = 0) then PC ← PC + k + 1	1/2	—
20	BRNE k	Branch if Not Equal	If (Z = 0,) then PC ← PC + k + 1	1/2	—
21	BRSH k	Branch if Same or Higher	if (C = 0), then PC ← PC + k + 1	1/2	—
22	BRLO k	Branch if Lower	if (C = 1), then PC ← PC + k + 1	1/2	—
23	BRMI	Branch if Minus	if (N = 1), then PC ← PC + k + 1	1/2	—
24	BRPL	Branch if Plus	if (N = 0), then PC ← PC + k + 1	1/2	—
25	BRGE	Branch if Greater or Equal, Signed	if (N ⊕ V) = 0, then PC ← PC + k + 1	1/2	—
26	BRLT	Branch if Less Than Zero, Signed	if (N ⊕ V) = 1, then PC ← PC + k + 1	1/2	—
27	BRHS	Branch if Half Carry Flag Set	if (C = 0) then PC ← PC + k + 1	1/2	—
28	BRHC	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	1/2	—
29	BRTS	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	1/2	—
30	BRTC	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	1/2	—
31	BRVS	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	1/2	—
32	BRVC	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	1/2	—
33	BRID	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	1/2	—
34	BRIE	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	1/2	—

Control instructions

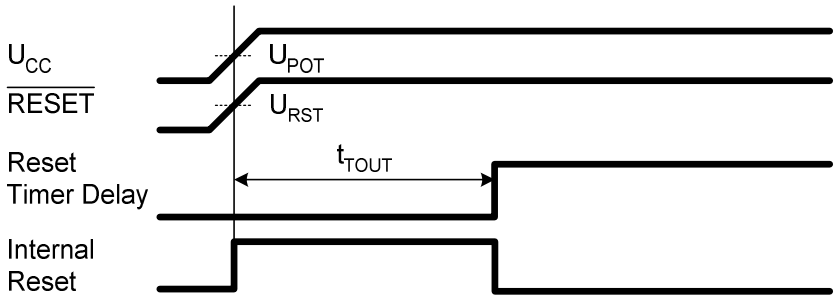
N°	Mnemonics	Descriptrion	Operation	Clock	Flags
1	NOP	No Operation	-	1	—
2	SLEEP	Sleep	See section 4.3	3	—
3	WDR	Watchdog Reset	See section 6.10	1	—

Symbols descriptions

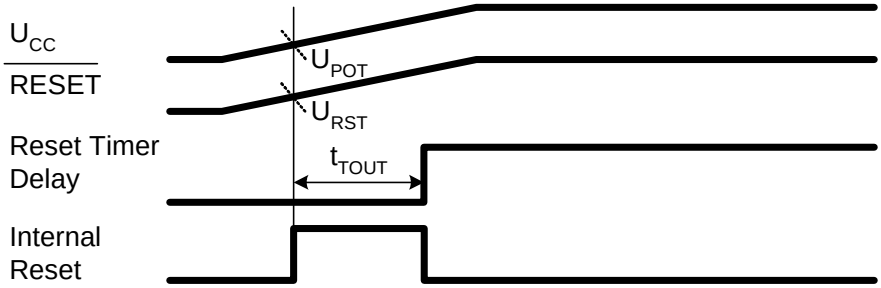
N	Symbol	Description
		State counter
1	SREG	MCU state counter
2	C	Carry Flag
3	Z	Zero Flag
4	N	Negative Flag
5	V	Twos Complement Overflow Flag
6	S	Signed Flag, S = N ⊕ V
7	H	Half Carry Flag
8	T	Пользовательский флаг
9	I	Global Interrupt Enable Flag
		Registers & Operands
1	Rd	Register receiver (sometimes Register Source) in Register File
2	Rr	Register Source in Register File
3	K	Costant (data)
4	k	Address — Constant
5	b	GPR Bit Number or PBB (0...7)
6	s	State Counter Bit Number SREG (0...7)
7	X,Y,Z	Pointers (X = R27:R26, Y = R29:R28, R31:R30)
8	I/O	I/O Register
9	A	I/O Space Address
10	q	Shift for Relative Indirect Addressing (6-bit value)
11	.	Register Name (Address) & Bit Number Separator
12	[XX]	Content of Memory Cell with Address XX
13	{XX}	Content of Memory Cell with Address XX (memory of programs)
		Operations
1	•	Inversion
2	•	Logical AND
3	∨	Logical OR
4	⊕	Exclusive OR
		Systems
1	PC	Programm counter
2	STACK	Current Stack Level
3	SP	Stack Pointer
		Flags
1	⇔	Instruction Effect on Flag
2	0	Reset Flag to "0"
3	1	Set flag to "1"
4	—	Instruction don't Effect on Flag

Waveform diagram

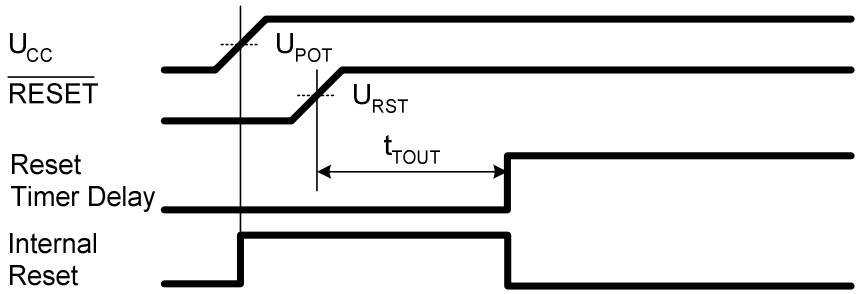
Reset for Power up ($\overline{\text{RESET}}$ pin is connected to U_{cc})



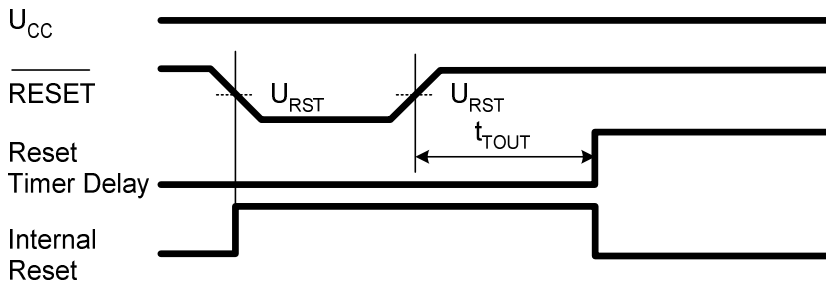
Reset for Power up ($\overline{\text{RESET}}$ pin is connected to U_{cc} , U_{cc} rise time is long)



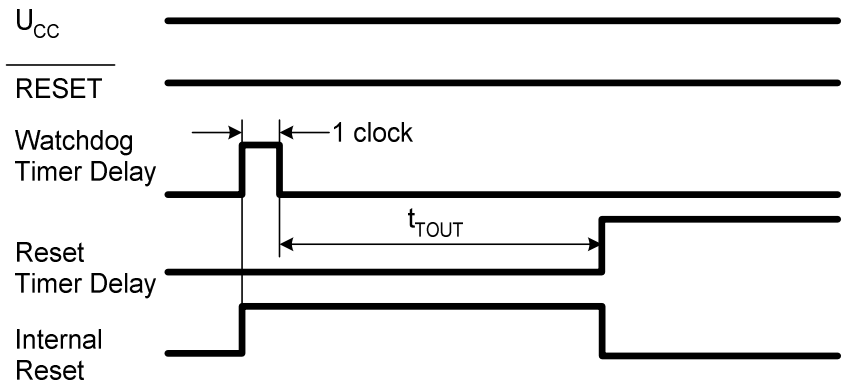
Reset for Power up ($\overline{\text{RESET}}$ pin is externally controlled)



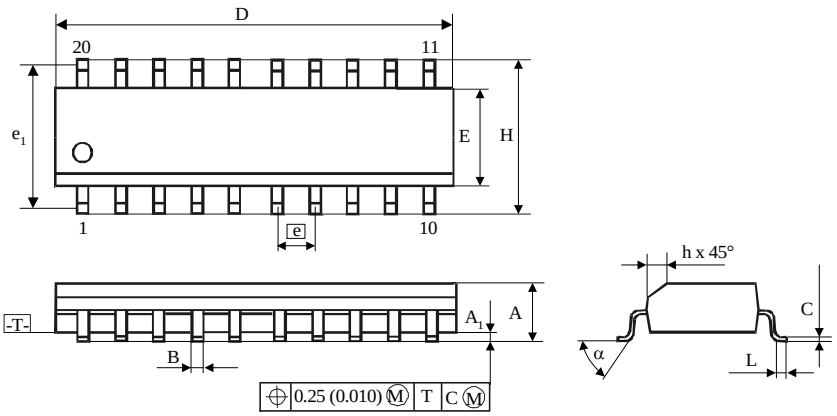
Hardware Reset



Watchdog timer Reset



MS-013AC Package dimensions



	A	A_1	B	C	D	E	e	e_1	H	h	L	α
mm												°
min	2.35	0.10	0.33	0.23	12.60	7.40	1.27	9.53	10.00	0.25	0.40	0
max	2.65	0.30	0.51	0.32	13.00	7.60	(nom)	(nom)	10.65	0.75	1.27	8