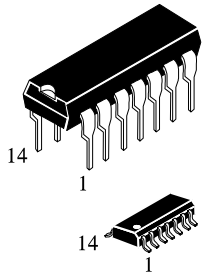
IN74HC21A

Dual 4-Input AND Gate



ORDERING INFORMATION

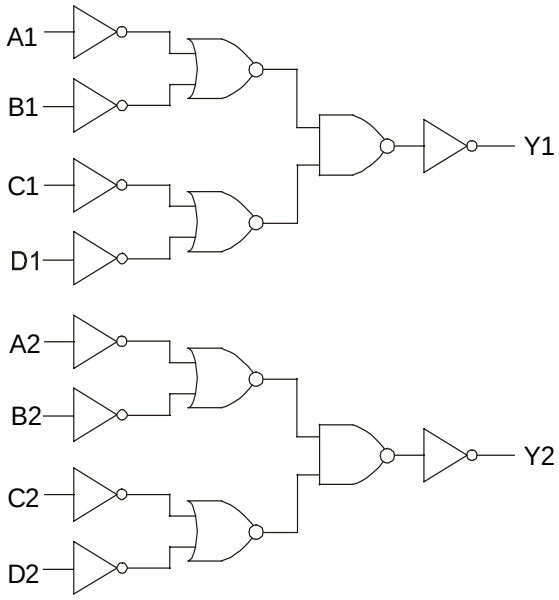
IN74HC21AN	Plastic
IN74HC21AD	SOIC

T_A = -55° to 125° C for all packages

The IN74HC21A is high-speed Si-gate CMOS device and is pin compatible with pullup resistors with low power Schottky TTL (LSTTL). The device provide the Dual 4-input AND function.

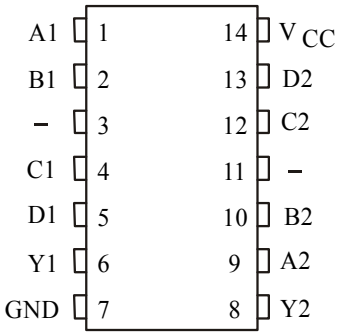
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

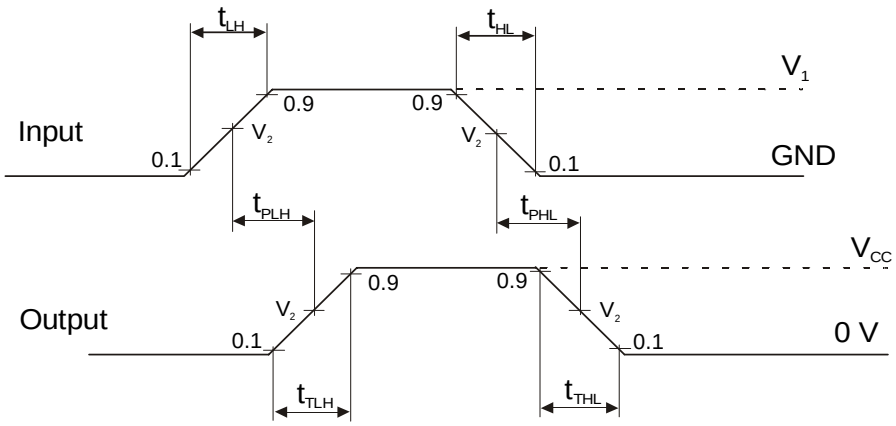
DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage		2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = -50 μA	2.0 3.0 4.5 6.0	1.92 2.92 4.42 5.92	1.9 2.9 4.4 5.9	1.9 2.9 4.4 5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = -2.4 mA	3.0	2.48	2.34	2.2	
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = -4 mA	4.5	3.98	3.84	3.7	
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = -5.2 mA	6.0	5.48	5.34	5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN}= V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = 50 μA	2.0 3.0 4.5 6.0	0.09 0.09 0.09 0.09	0.1 0.1 0.1 0.1	0.1 0.1 0.1 0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = 2.4 mA	3.0	0.26	0.33	0.4	
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = 4 mA	4.5	0.26	0.33	0.4	
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert$ = 5.2 mA	6.0	0.26	0.33	0.4	
I_{IL}	Maximum Low-Level Input Leakage Current	V_{IN}= 0 V	6.0	-0.1	-1.0	-1.0	μA
I_{IH}	Maximum High-Level Input Leakage Current	$V_{IN}= V_{CC}$	6.0	0.1	1.0	1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or 0 V	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

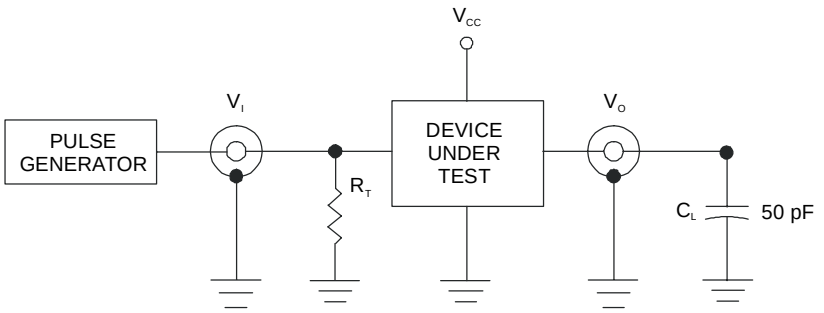
Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PHL}, t_{PLH}	Maximum Propagation Delay (Figure 1)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time (Figure 1)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	5.0	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	T_A=25°C,V_{CC}=5.0 V 50	pF



V_1 = 0.5 V_{CC}

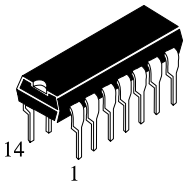
Figure 1. Switching Waveforms

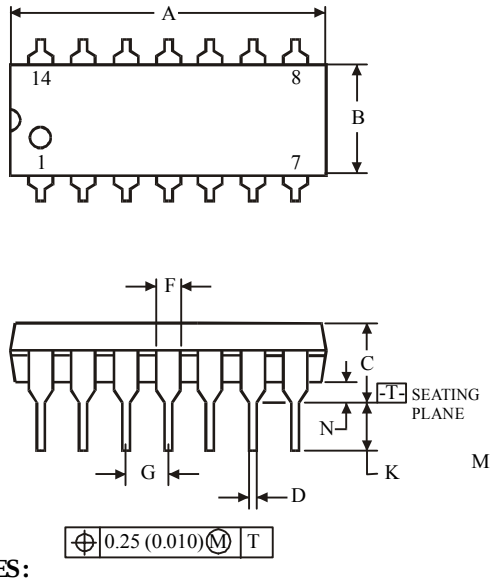


Termination resistance R_T – should be equal to Z_{OUT} of pulse generators

Figure 2. Test Circuit

N SUFFIX PLASTIC DIP
(MS - 001AA)



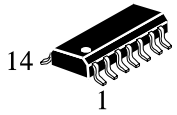


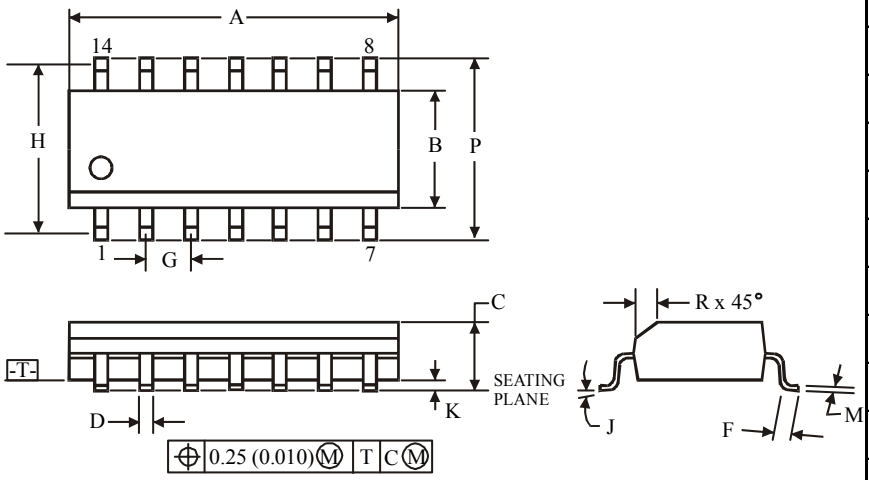
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AB)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.