

2K 1.8V CMOS Serial EEPROMs

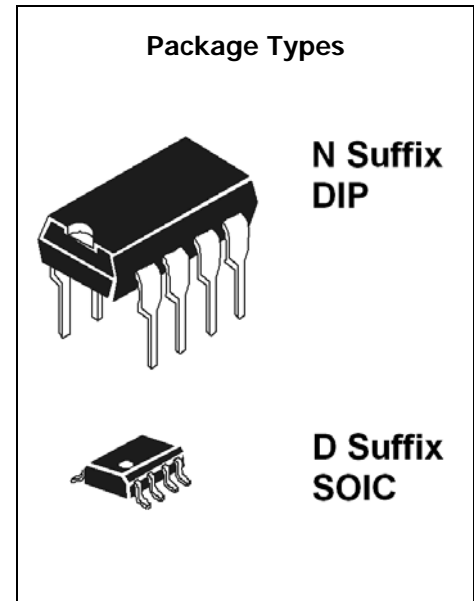
IN24AA02

DESCRIPTION

IN24AA02 is a 2K-bit Electrically Erasable PROM. The device is organized as a single block of 256x8 bit memory with a two-wire serial interface. Low voltage design permits operation down to 1.8V with standby and active currents of only 1 μ A and 3mA respectively. The IN24AA02 also has a page-write capability for up to 8 bytes of data.

FEATURES

- Single supply with operation down to 1.8V
- Two version:
 - Version A – pins A0, A1, A2 are using for the addressing on a single bus system (up to eight ICs),
 - Version B – pins A0, A1, A2 are not using. Only one IC may be using on a bus.
- Low power CMOS technology
- Organized as a single block of 256 bytes (256x8)
- Two wire serial interface bus, IIC compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (2.5-5.5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 6 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 2,000V
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-pin SOP
- Temperature range -40°C to +85°C (industrial)



PIN ASSIGNMENT

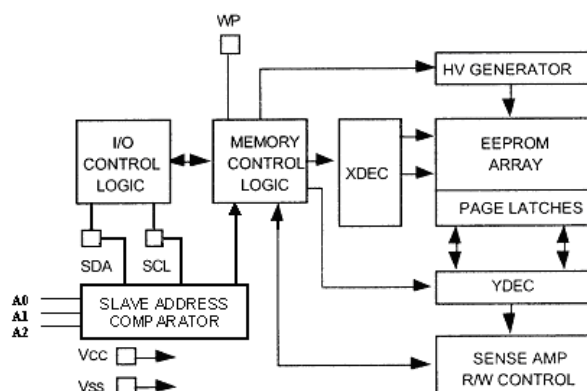
A0	1	8	V _{CC}
A1	2	7	WP
A2	3	6	SCL
V _{SS}	4	5	SDA

PINNING

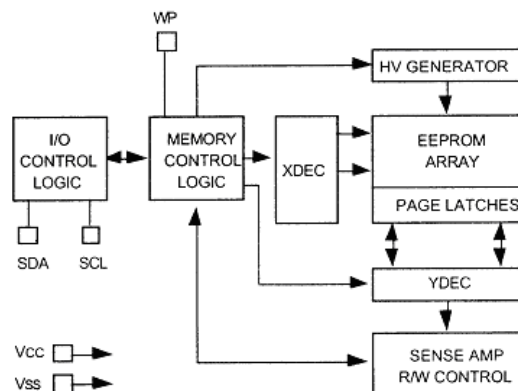
Name	Function
V _{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
V _{CC}	+1.8V to 5.5V Power Supply
A0, A1, A2	Pins for device address selection

Note: Pins A0, A1 & A2 are not used for IN24AA02B (No internal connections)

Figure 1. Representative Block Diagram



24AA02A Block Diagram



24AA02B Block Diagram

ELECTRICAL CHARACTERISTICS

Maximum Ratings

Parameter	Value
V_{CC}	7.0 V
All inputs and outputs w.r.t. V_{SS}	-0.3V to $V_{CC}+1.0V$
Storage temperature	-65°C to +150°C
Ambient temp. with power applied	-40°C to +85°C

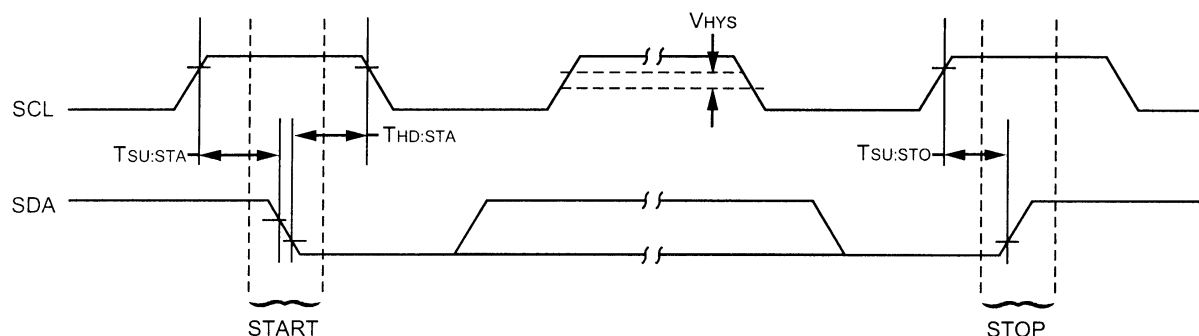
DC CHARACTERISTICS

$V_{CC} = +1.8V$ to $+5.5V$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$

Parameter	Symbol	Min	Max	Units	Mode
WP, SCL and SDA pins:					
High level input voltage	V_{IH}	$0.7V_{CC}$	-	V	(Note) $I_{OL}=3.0mA$, $V_{CC}=2.5V$
Low level input voltage	V_{IL}	-	$0.3V_{CC}$	V	
Hysteresis of Schmitt trigger inputs	V_{HYS}	$0.05V_{CC}$	-	V	
Low level output voltage	V_{OL}	-	0.40	V	
Input leakage current	I_{LI}	-	± 1	μA	$V_{IN}=V_{SS}$ to V_{CC}
Output leakage current	I_{LO}	-	± 1	μA	$V_{OUT}=V_{SS}$ to V_{CC}
Pin capacitance (all inputs/outputs)	C_{IN} C_{OUT}	-	10	pF	$V_{CC}=5.0V$ (Note) $T_{amb}=25^{\circ}C$, $F_{CLK}=1MHz$
Operating current	I_{CC} WRITE I_{CC} READ	-	3 1	mA mA	$V_{CC}=5.5V$, $SCL=400kHz$ -
Standby current	I_{CCS}	-	1	μA	$SDA=SCL=V_{CC}$, $WP=V_{SS}$

Note: This parameter is periodically sampled and not 100% tested.

Figure 2. Bus timing Start/Stop

**AC CHARACTERISTICS**

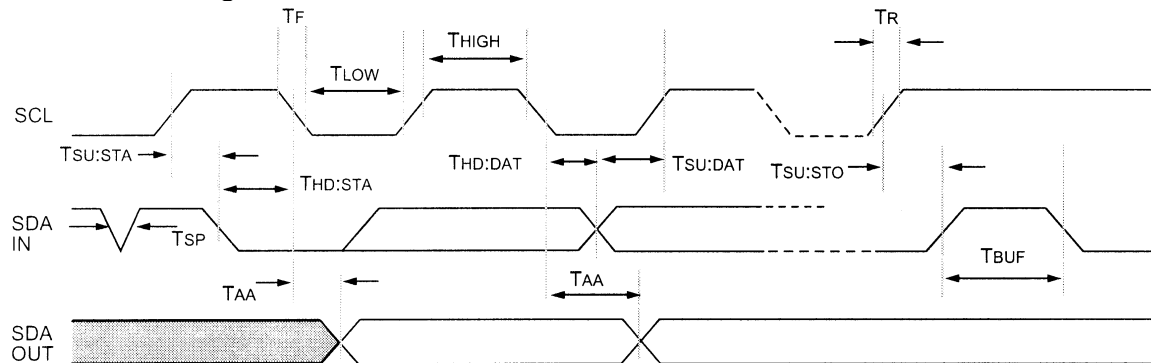
Parameter	Symbol	1.8≤V _{CC} <2.5V		2.5≤V _{CC} ≤5.5V		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	F _{CLK}	-	100	-	400	kHz	
Clock high time	T _{HIGH}	4000	-	600	-	ns	
Clock low time	T _{LOW}	4700	-	1300	-	ns	
SDA and SCL rise time	T _R	-	1000	-	300	ns	Note 2
SDA and SCL fall time	T _F	-	300	-	300	ns	Note 2
START condition hold time	T _{HD:STA}	4000	-	600	-	ns	After this period the first clock pulse is generated
START condition setup time	T _{SU:STA}	4700	-	600	-	ns	Only relevant for repeated START condition
Data input hold time	T _{HD:DAT}	0	-	0	-	ns	Note 1
Data input setup time	T _{SU:DAT}	250	-	100	-	ns	
STOP condition setup time	T _{SU:STO}	4000	-	600	-	ns	
Output valid from clock	T _{AA}	-	3500	-	900	ns	Note 1
Bus free time	T _{BUF}	4700	-	1300	-	ns	Time the bus must be free before a new transmission can start
Output fall time from V _{IH} min to V _{IL} max	T _{OF}	-	250	20+0.1C _B	250	ns	C _B ≤100pF (Note2)
Input filter spike suppression (SDA & SCL pins)	T _{SP}	-	50	-	50	ns	Note 3
Write cycle time	T _{WR}	-	5	-	5	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. C_B = total capacitance of one bus line in pF.

Note 3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt trigger inputs that provide improved noise and spike suppression. This eliminates the need for a T_i specification for standard operation.

Figure 3. Bus timing Data



FUNCTIONAL DESCRIPTION

The IN24AA02 supports a bi-directional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the IN24AA02 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 4).

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although

only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

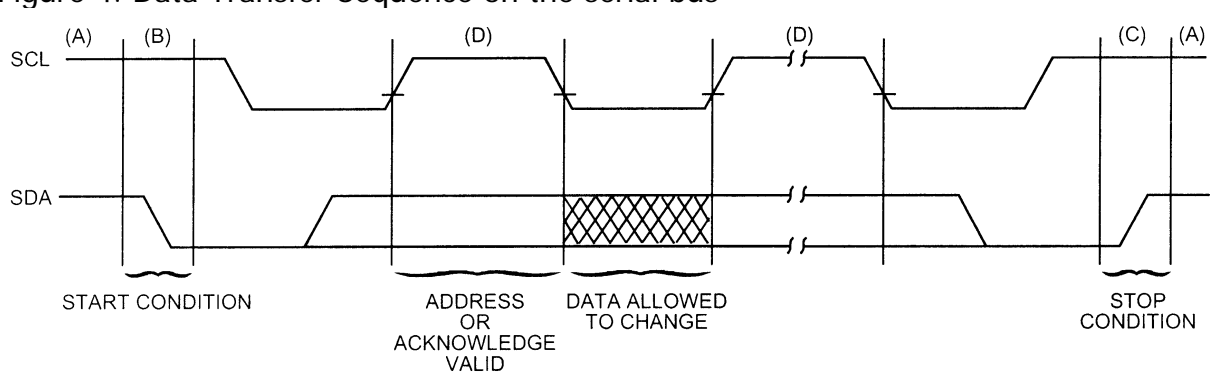
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The IN24AA02 does not generate any acknowledge bits if an internal programming cycle is in progress

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 4. Data Transfer Sequence on the serial bus



BUS CHARACTERISTICS

Slave Address

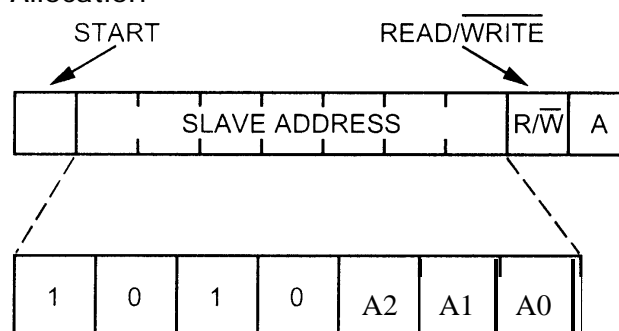
The IN24AA02 are software-compatible with devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24AA02 can be used in place of two 24AA01's, for example, without any modifications to software. The "chip select" portion of the control byte becomes don't care.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the IN24AA02, followed by three bits address selection (In a case of IN24AA02B these three bits can be anyone). The eighth bit of slave address determines if the master device wants to read or write to the IN24AA02 (see Figure 5).

The IN24AA02 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/W
For IN24AA02A			
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0
For IN24AA02B			
Read	1010	X X X	1
Write	1010	X X X	0

Figure 5. Control Byte Allocation



WRITE OPERATION

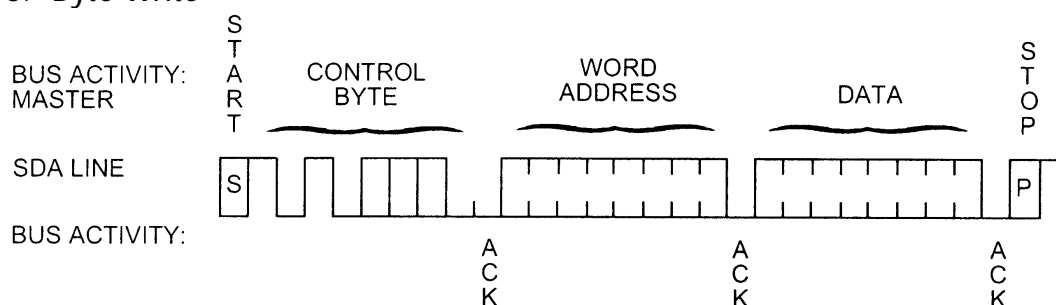
Byte Write

Following the start condition from the master, the device code (4 bits), the device address selection (3 bits), and the R/W bit, which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the IN24AA02. After receiving another acknowledge signal from the IN24AA02 the master device will transmit the data word to be written into the addressed memory location. The IN24AA02 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the IN24AA02 will not generate acknowledge signals (see Figure 6).

Page Write

The write control byte, word address and the first data byte are transmitted to the IN24AA02 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the IN24AA02, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8).

Figure 6. Byte Write

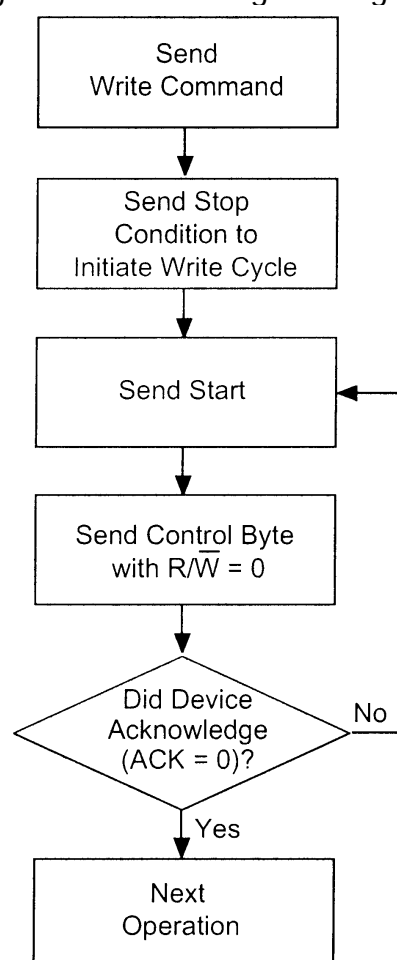


ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput).

Once the stop conditions for a write command has been issued from the master, the device initiates the internally timed write cycle, ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\bar{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7 for flow diagram.

Figure 7. Acknowledge Polling Flow



WRITE PROTECTION

The IN24AA02 can be used as a serial ROM when the WP pin is connected to V_{CC} . Programming will be inhibited and the entire memory will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

CURRENT ADDRESS READ

The IN24AA02 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n , the next current address read operation would access data from address $n+1$. Upon receipt of the slave address with R/W bit set to one, the IN24AA02 issues an acknowledge and transmits the eight bit data word. The

master will not acknowledge the transfer but does generate a stop condition and the IN24AA02 discontinues transmission (see Figure 9).

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. Sending the word address to the IN24AA02 as part of a write operation does this. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The IN24AA02 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the IN24AA02 discontinues transmission (see Figure 10).

Figure 8. Page Write

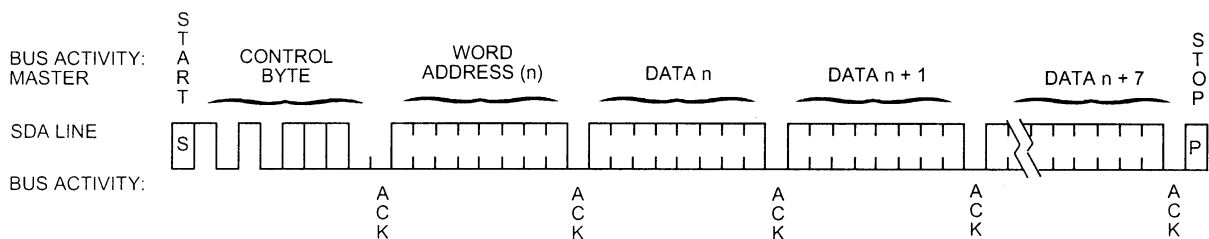


Figure 9. Current Address Read

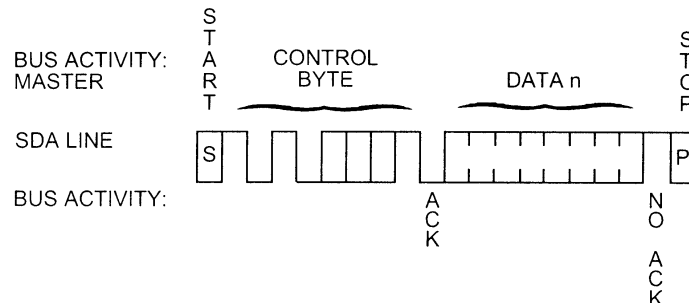
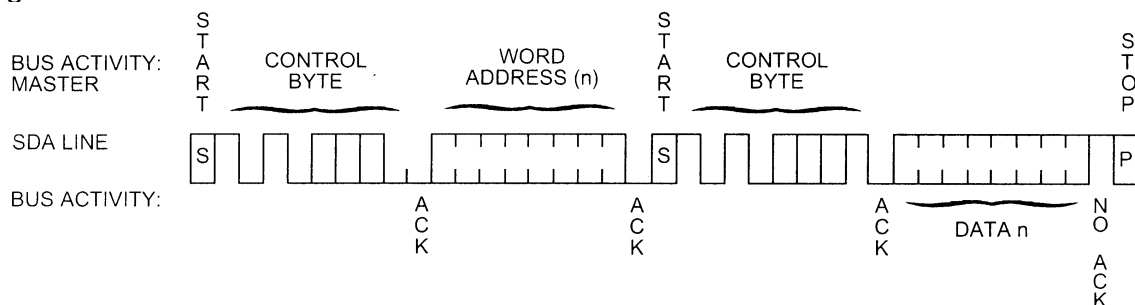


Figure 10. Random Read



SEQUENTIAL READ

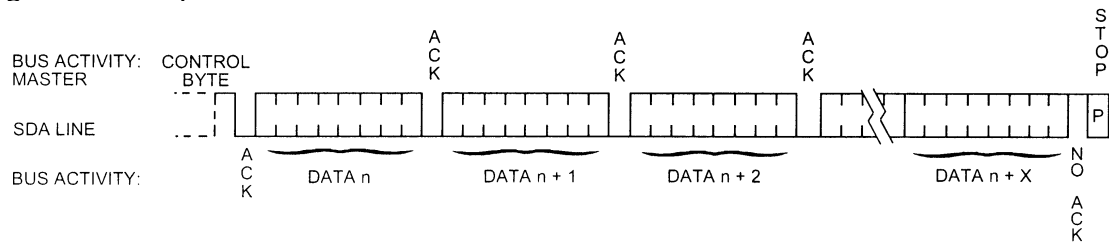
Sequential reads are initiated in the same way as a random read except that after the IN24AA02 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the IN24AA02 to transmit the next sequentially addressed 8 bit word (see Figure 11).

To provide sequential reads the IN24AA02 contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

NOISE PROTECTION

The SCL and SDA inputs have Schmitt trigger and filter circuits, which suppress noise spikes to assure proper device operation even on a noisy bus.

Figure 11. Sequential read



PIN DESCRIPTIONS

SDA Serial Address/Data Input/Output

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to V_{CC} (typical 4.7K Ω for 100kHz, 1K Ω for 400kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP

This pin must be connected to either V_{SS} or V_{CC} .

If tied to V_{SS} , normal memory operation is enabled (read/write the entire memory).

If tied to V_{CC} , WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the IN24AA02 as a serial ROM when WP is enabled (tied to V_{CC}). This pin is internally pulled down to V_{SS} .

A0, A1, A2

For IN24AA02A these inputs are used to device address selection. These pins are internally pulled down to V_{SS} .

For IN24AA02B these inputs are not used. They may be left floating or tied to either V_{SS} or V_{CC} .

TYPICAL CONFIGURATION

Using the A0, A1, and A2 input pins (IN24AA02A), up to eight devices can be connected to the same two-wire bus as slaves (see figure 12). On the contrary only one IN24AA02B can be connected to the two-wire bus as the slave (see figure 13).

Figure 12. Typical Configuration for IN24AA02A

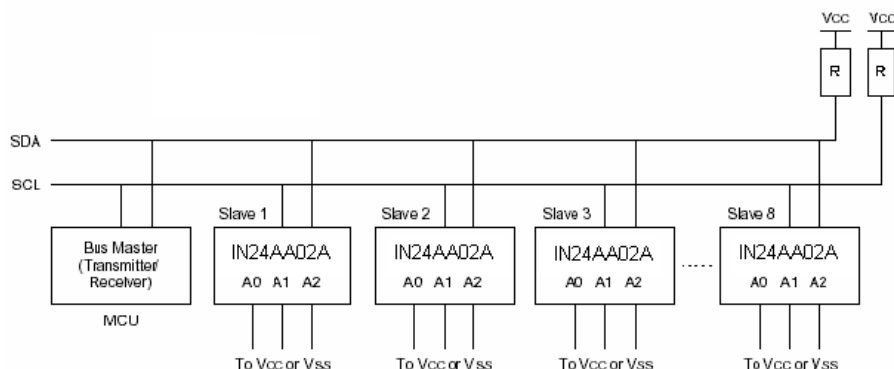
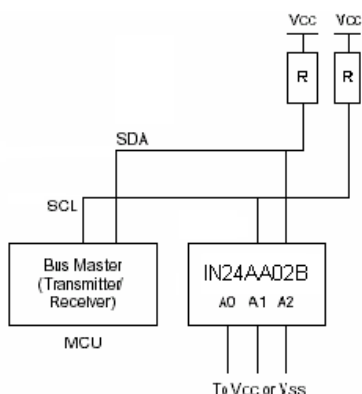


Figure 13. Typical Configuration for IN24AA02B

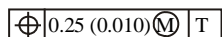
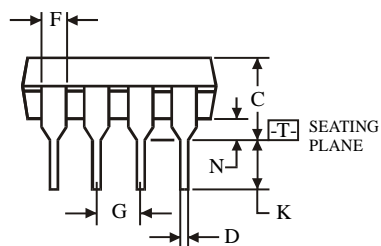
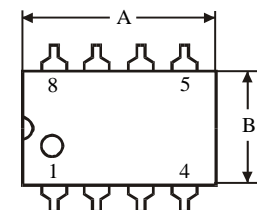


Ordering information

Ordering information

Type	Description	Ordering code	Package	Packing	Standard of packing
IN24AA02A	2K Bits, 1.8-5.5V, -40°C to +85°C, Address pins are used	IN24AA02AN	DIP-8	Tube	49
		IN24AA02AD	SOIC-8		97
		IN24AA02ADR1	SOIC-8	Tape & Reel	2500
		IN24AA02ADR2	SOIC-8		4000
		IN24AA02A	Chip on wafer (6'')		
IN24AA02B	2K Bits, 1.8-5.5V, -40°C to +85°C, Address pins are not used	IN24AA02BN	DIP-8	Tube	49
		IN24AA02BD	SOIC-8		97
		IN24AA02BDR1	SOIC-8	Tape & Reel	2500
		IN24AA02BDR2	SOIC-8		4000
		IN24AA02B	Chip on wafer (6'')		

N SUFFIX PLASTIC DIP
(MS – 001BA)



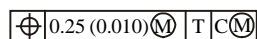
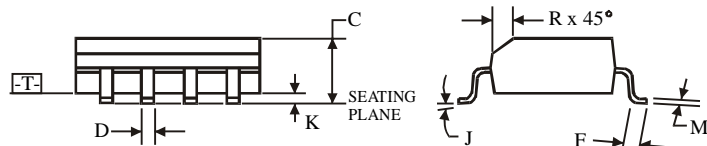
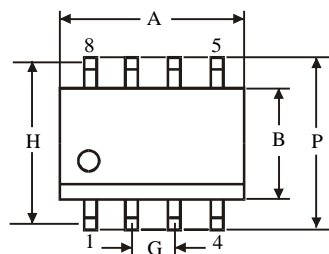
clude mold flash or protrusions.
0.25 mm (0.010) per side.

NOTES:
1. Dimensions "A", "B" do not include mold flash or protrusions.

Symbol	Dimension, mm	
	min	max
A	8.51	10.16
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

Maximum mold flash or protrusions

D SUFFIX SOIC
(MS - 012AA)

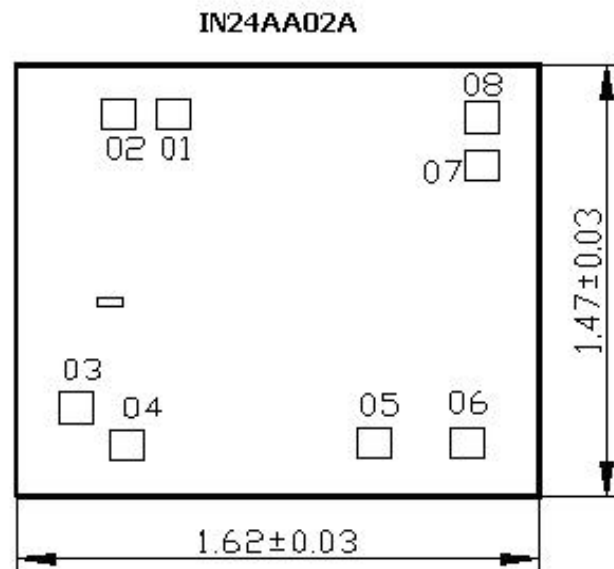


NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	min	max
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

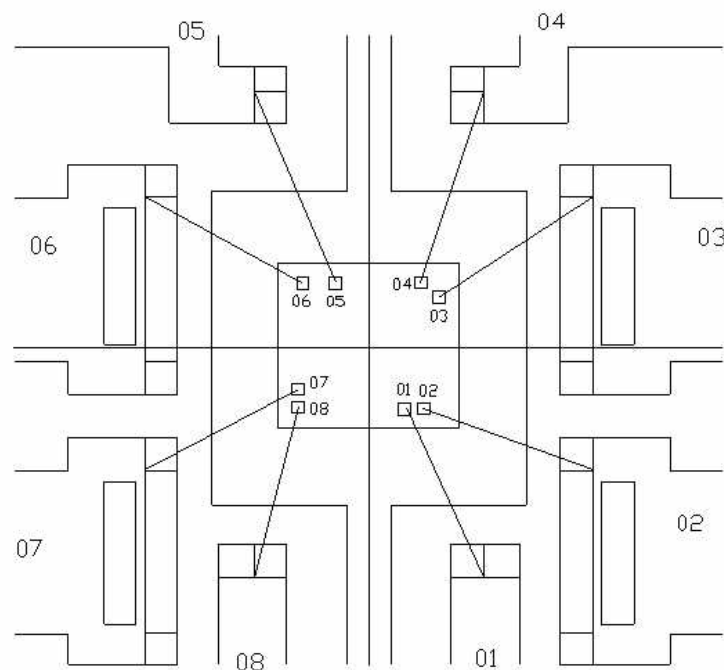
IN24AA02A Chip Diagram



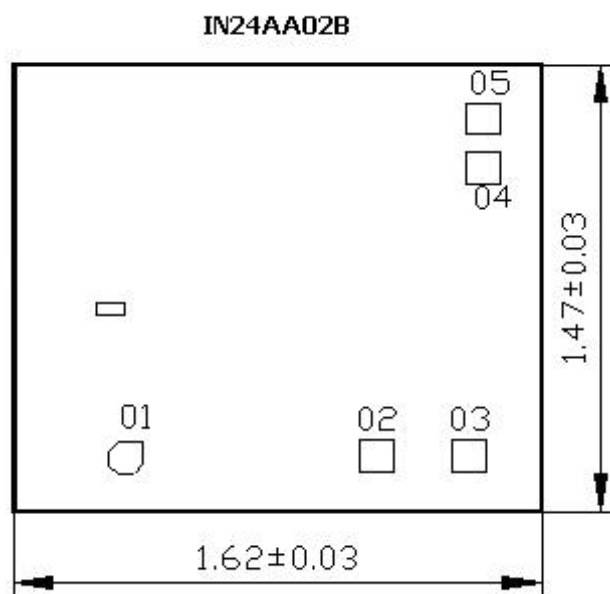
Pad location

Pad No	X, mkm	Y, mkm	Pad No	X, mkm	Y, mkm
1	423	1274	5	1068	105
2	245	1272	6	1366	105
3	106	232	7	1411	1092
4	272	101	8	1411	1260

IN24AA02A Bonding Diagram



IN24AA02B Chip Diagram

**Pad location**

Pad No	X, mkm	Y, mkm	Pad No	X, mkm	Y, mkm
01	272	101	04	1411	1.092
02	1068	105	05	1411	1260
03	1.366	0.105			

IN24AA02B Bonding Diagram

