SONY

Diagonal 6.46 mm (Type 1/2.8) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

Tentative

IMX327LQR-C

STARVIS

Description

The IMX327LQR-C is a diagonal 6.46 mm (Type 1/2.8) CMOS active pixel type solid-state image sensor with a square pixel array and 2.13 M effective pixels. This chip operates with analog 2.9 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- CMOS active pixel type dots
- Built-in timing adjustment circuit, H/V driver and serial communication circuit
- Input frequency: 74.25 MHz / 37.125 MHz
- Number of recommended recording pixels: 1920 (H) × 1080 (V) approx. 2.07M pixel
- Readout mode
  All-pixel scan mode
  720p-HD readout mode
  Window cropping mode
  Vertical / Horizontal direction-normal / inverted readout mode
- Readout rate
  Maximum frame rate in Full HD 1080p mode: 60 frame / s
- Wide dynamic range (WDR) function
  Multiple exposure WDR
  Digital overlap WDR
- Variable-speed shutter function (resolution 1H units)
- 10-bit / 12-bit A/D converter
- Conversion gain switching (HCG Mode / LCG Mode)
- CDS / PGA function
  0 dB to 27 dB: Analog Gain 27 dB (step pitch 0.3 dB)
  27.3 dB to 69 dB: Analog Gain 27 dB + Digital Gain 0.3 to 42 dB (step pitch 0.3 dB)
- Supports I/O switching
  Low voltage LVDS (150 m Vp-p) serial (2 ch / 4 ch switching) DDR output
  CSI-2 serial data output (2 Lane / 4 Lane, RAW10 / RAW12 output)
- Recommended exit pupil distance: –30 mm to –∞

Exmor R

Device Structure

- CMOS image sensor
- Image size
  Type 1/2.8
- Total number of pixels
  1945 (H) × 1109 (V) approx. 2.16 M pixels
- Number of effective pixels
  1945 (H) × 1097 (V) approx. 2.13 M pixels
- Number of active pixels
  1937 (H) × 1097 (V) approx. 2.12 M pixels
- Number of recommended recording pixels
  1920 (H) × 1080 (V) approx. 2.07 M pixels
- Unit cell size
  2.9 µm (H) × 2.9 µm (V)
- Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 10 pixels, rear 0 pixels
- Dummy
  Horizontal (H) direction: Front 0 pixels, rear 3 pixels
  Vertical (V) direction: Front 0 pixels, rear 0 pixels
- Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 2.9 V)	AV_{DD}	-0.3	3.3	V	
Supply voltage (interface 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital 1.2 V)	DV_{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V

Application Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 2.9 V)	AV_{DD}	2.80	2.90	3.00	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V
Performance guarantee temperature	Tspec	-10	—	60	˚C
Operating guarantee temperature	Topr	-30	—	85	˚C
Storage guarantee temperature	Tstg	-40	—	85	˚C

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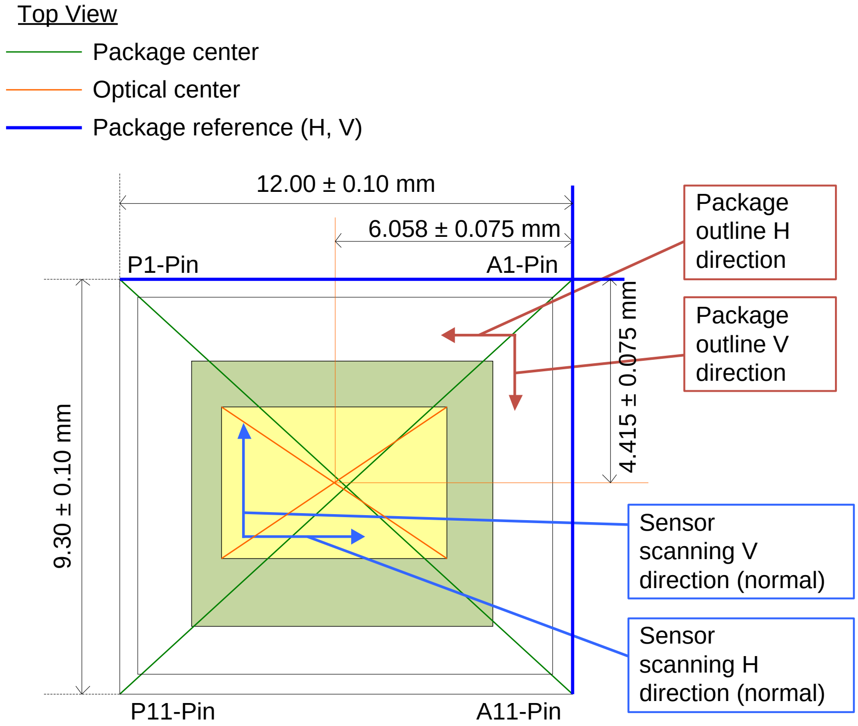
General-0.0.9

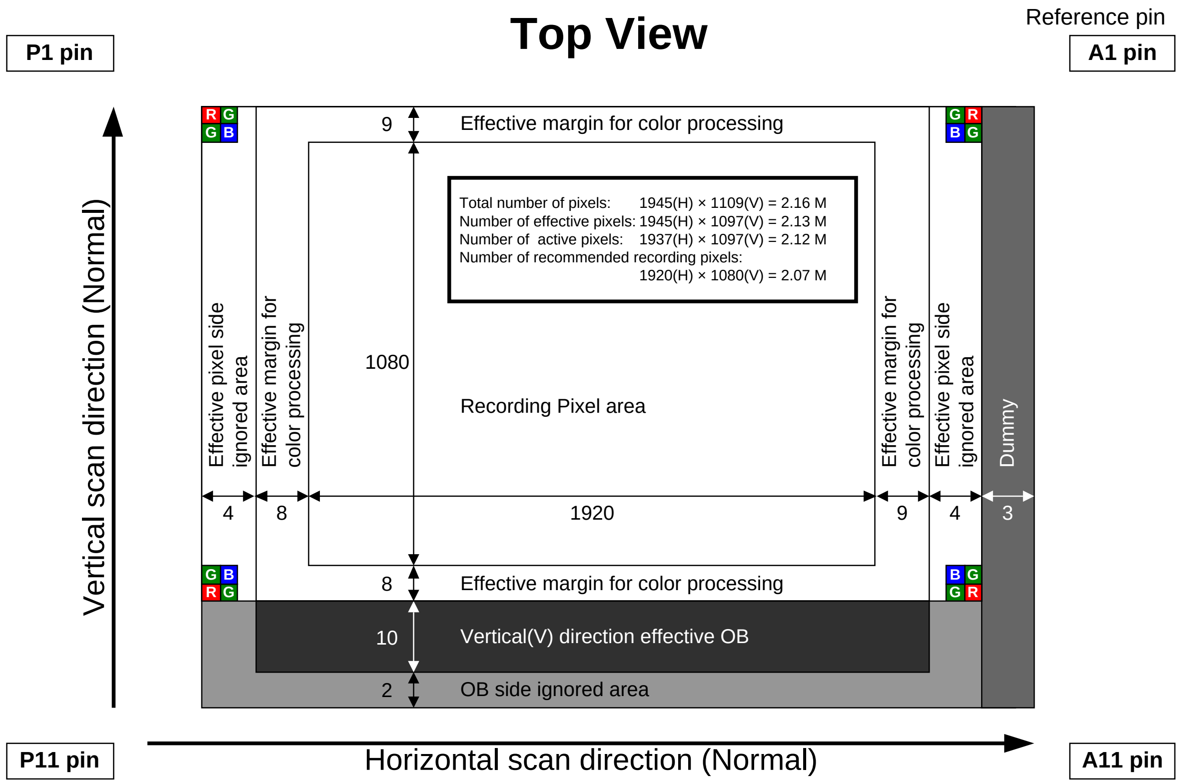
Contents

Optical Center



Optical Center

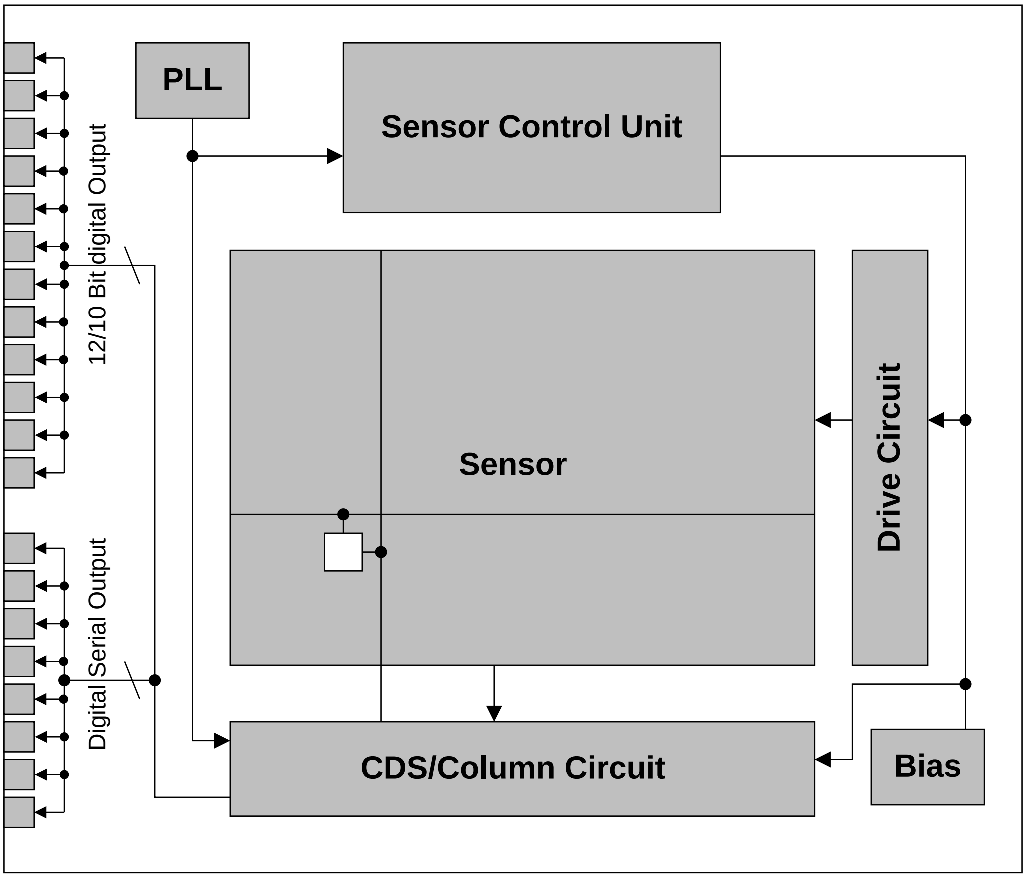
Pixel Arrangement



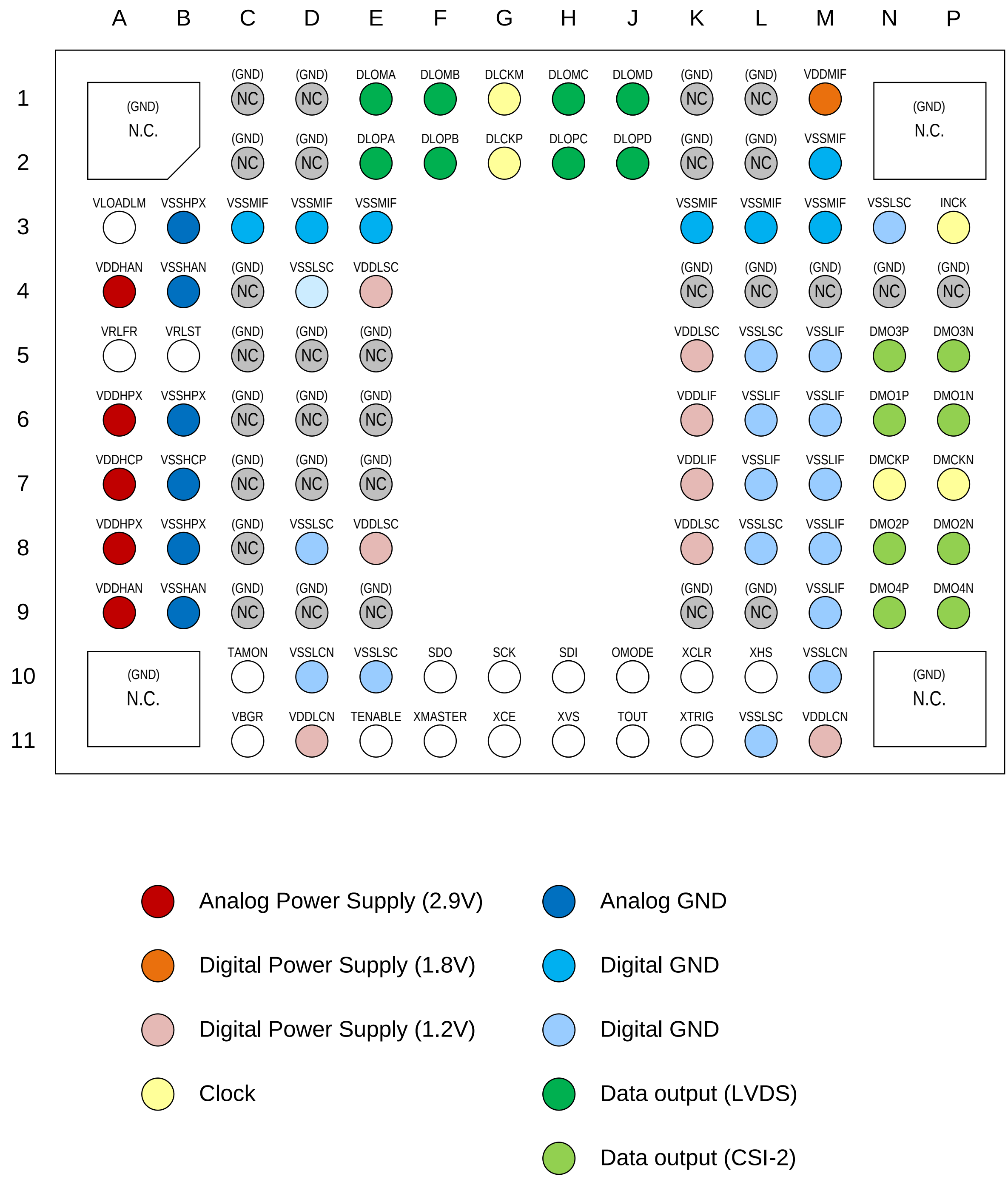
* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.

Pixel Arrangement (Top View)

Block Diagram and Pin Configuration



Block Diagram



*The N.C. pin can be connected to GND.

Pin Configuration (Bottom View)

Pin Description

No.	Pin No	I/O	Analog /Digital	Symbol	Description	Remarks
1	A1	—	—	N.C.	—	GND connectable
2	A3	O	A	VLOADLM	Reference pin	
3	A4	Power	A	VDDHAN	2.9 V power supply	
4	A5	O	A	VRLFR	Reference pin	
5	A6	Power	A	VDDHPX	2.9 V power supply	
6	A7	Power	A	VDDHCP	2.9 V power supply	
7	A8	Power	A	VDDHPX	2.9 V power supply	
8	A9	Power	A	VDDHAN	2.9 V power supply	
9	A11	—	—	N.C.	—	GND connectable
10	B3	GND	A	VSSHPX	2.9 V GND	
11	B4	GND	A	VSSHAN	2.9 V GND	
12	B5	O	A	VRLST	Reference pin	
13	B6	GND	A	VSSHPX	2.9 V GND	
14	B7	GND	A	VSSHCP	2.9 V GND	
15	B8	GND	A	VSSHPX	2.9 V GND	
16	B9	GND	A	VSSHAN	2.9 V GND	
17	C1	—	—	N.C.	—	GND connectable
18	C2	—	—	N.C.	—	GND connectable
19	C3	GND	D	VSSMIF	1.8 V GND	
20	C4	—	—	N.C.	—	GND connectable
21	C5	—	—	N.C.	—	GND connectable
22	C6	—	—	N.C.	—	GND connectable
23	C7	—	—	N.C.	—	GND connectable
24	C8	—	—	N.C.	—	GND connectable
25	C9	—	—	N.C.	—	GND connectable
26	C10	O	A	TAMON	TEST output pin	OPEN
27	C11	O	A	VBGR	Reference pin	
28	D1	—	—	N.C.	—	GND connectable
29	D2	—	—	N.C.	—	GND connectable
30	D3	GND	D	VSSMIF	1.8 V GND	
31	D4	GND	D	VSSLSC	1.2 V GND	
32	D5	—	—	N.C.	—	GND connectable
33	D6	—	—	N.C.	—	GND connectable
34	D7	—	—	N.C.	—	GND connectable
35	D8	GND	D	VSSLSC	1.2 V GND	
36	D9	—	—	N.C.	—	GND connectable
37	D10	GND	D	VSSLCN	1.2 V GND	
38	D11	Power	D	VDDLCN	1.2 V power supply	

No.	Pin No	I/O	Analog /Digital	Symbol	Description	Remarks
39	E1	O	D	DLOMA	LVDS output	data
40	E2	O	D	DLOPA	LVDS output	data
41	E3	GND	D	VSSMIF	1.8 V GND	
42	E4	Power	D	VDDLSC	1.2 V power supply	
43	E5	—	—	N.C.	—	GND connectable
44	E6	—	—	N.C.	—	GND connectable
45	E7	—	—	N.C.	—	GND connectable
46	E8	Power	D	VDDLSC	1.2 V power supply	
47	E9	—	—	N.C.	—	GND connectable
48	E10	GND	D	VSSLSC	1.2 V GND	
49	E11	I	D	TENABLE	TEST Enable	OPEN
50	F1	O	D	DLOMB	LVDS output	data
51	F2	O	D	DLOPB	LVDS output	data
52	F10	O	D	SDO	Communication output	4-wire: SDO pin I^2C: Open
53	F11	I	D	XMASTER	Master / Slave selection	High: Slave mode / Low: Master mode
54	G1	O	D	DLCKM	LVDS output	clock
55	G2	O	D	DLCKP	LVDS output	clock
56	G10	I	D	SCK	Communication clock	4-wire: SCK pin I^2C: SCL pin
57	G11	I	D	XCE	Communication enable	4-wire: XCE pin I^2C: Fixed to High
58	H1	O	D	DLOMC	LVDS output	data
59	H2	O	D	DLOPC	LVDS output	data
60	H10	I/O	D	SDI	Communication input	4-wire: SDI pin I^2C: SDA pin
61	H11	I/O	D	XVS	Vertical sync signal	
62	J1	O	D	DLOMD	LVDS output	data
63	J2	O	D	DLOPD	LVDS output	data
64	J10	I	D	OMODE	Serial output interface selection	High: LVDS / Low: CSI-2
65	J11	O	D	TOUT	TEST output pin	OPEN
66	K1	—	—	N.C.	—	GND connectable
67	K2	—	—	N.C.	—	GND connectable
68	K3	GND	D	VSSMIF	1.8 V GND	
69	K4	—	—	N.C.	—	GND connectable
70	K5	Power	D	VDDLSC	1.2 V power supply	
71	K6	Power	D	VDDLIF	1.2 V power supply	
72	K7	Power	D	VDDLIF	1.2 V power supply	
73	K8	Power	D	VDDLSC	1.2 V power supply	
74	K9	—	—	N.C.	—	GND connectable
75	K10	I	D	XCLR	System clear	High: Normal / Low: Clear
76	K11	I	D	XTRIG	Trigger mode input	OPEN
77	L1	—	—	N.C.	—	GND connectable
78	L2	—	—	N.C.	—	GND connectable

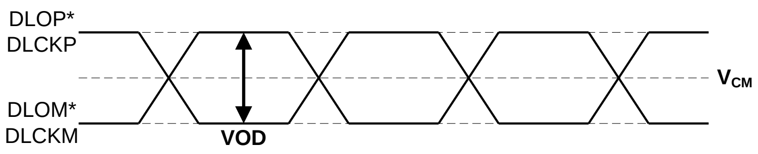
No.	Pin No	I/O	Analog /Digital	Symbol	Description	Remarks
79	L3	GND	D	VSSMIF	1.8 V GND	
80	L4	—	—	N.C.	—	GND connectable
81	L5	GND	D	VSSLSC	1.2 V GND	
82	L6	GND	D	VSSLIF	1.2 V GND	
83	L7	GND	D	VSSLIF	1.2 V GND	
84	L8	GND	D	VSSLSC	1.2 V GND	
85	L9	—	—	N.C.	—	GND connectable
86	L10	I/O	D	XHS	Horizontal sync signal	
87	L11	GND	D	VSSLSC	1.2 V GND	
88	M1	Power	D	VDDMIF	1.8 V power supply	
89	M2	GND	D	VSSMIF	1.8 V GND	
90	M3	GND	D	VSSMIF	1.8 V GND	
91	M4	—	—	N.C.	—	GND connectable
92	M5	GND	D	VSSLIF	1.2 V GND	
93	M6	GND	D	VSSLIF	1.2 V GND	
94	M7	GND	D	VSSLIF	1.2 V GND	
95	M8	GND	D	VSSLIF	1.2 V GND	
96	M9	GND	D	VSSLIF	1.2 V GND	
97	M10	GND	D	VSSLCN	1.2 V GND	
98	M11	Power	D	VDDLCN	1.2 V power supply	
99	N3	GND	D	VSSLSC	1.2 V GND	
100	N4	—	—	N.C.	—	GND connectable
101	N5	O	D	DMO3P	CSI-2 output	data
102	N6	O	D	DMO1P	CSI-2 output	data
103	N7	O	D	DMCKP	CSI-2 output	clock
104	N8	O	D	DMO2P	CSI-2 output	data
105	N9	O	D	DMO4P	CSI-2 output	data
106	P1	—	—	N.C.	—	GND connectable
107	P3	I	D	INCK	Master clock input	
108	P4	—	—	N.C.	—	GND connectable
109	P5	O	D	DMO3N	CSI-2 output	data
110	P6	O	D	DMO1N	CSI-2 output	data
111	P7	O	D	DMCKN	CSI-2 output	clock
112	P8	O	D	DMO2N	CSI-2 output	data
113	P9	O	D	DMO4N	CSI-2 output	data
114	P11	—	—	N.C.	—	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	analog	VDDHx	AV_{DD}		2.80	2.90	3.00	V
	Interface	VDDMx	OV_{DD}		1.70	1.80	1.90	V
	digital	VDDLx	DV_{DD}		1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER OMODE SCK SDI XCE XTRIG	VIH	XVS / XHS Slave Mode	$0.8OV_{DD}$	—	—	V
			VIL		—	—	$0.2OV_{DD}$	V
Digital output voltage		DLOP [A:D] DLOM [A:D] DLCKP DLCKM	VCM	Low voltage LVDS	—	$OV_{DD}/2$	—	V
			VOD	Low voltage LVDS (Termination resistance: 100 Ω)	100	150	220	mV
		XHS XVS SDO TOUT	VOH	XVS / XHS Master Mode	OV_{DD}-0.4	—	—	V
			VOL		—	—	0.4	V

LVDS output



Current Consumption

Item	pin	Symbol	Typ.		Max.		Unit
			Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current MIPI CSI-2 / 4 Lane 12 bit, 60 frame/s Full HD 1080p mode	VDDH	IAV_{DD}	TBD	TBD	TBD	TBD	mA
	VDDM	IOV_{DD}	TBD	TBD	TBD	TBD	mA
	VDDL	IDV_{DD}	TBD	TBD	TBD	TBD	mA
Standby current	VDDH	IAV_{DD}_STB	TBD		TBD		mA
	VDDM	IOV_{DD}_STB	TBD		TBD		mA
	VDDL	IDV_{DD}_STB	TBD		TBD		mA

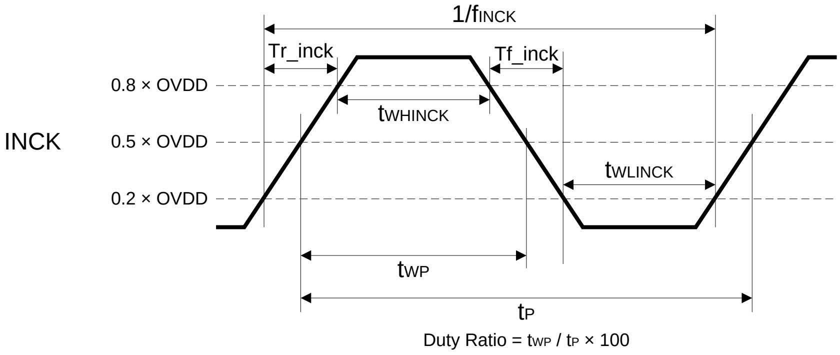
Operating current: (Typ.) Supply voltage 2.90 V / 1.8 V / 1.2 V, Tj = 25 ˚C
(Max.) Supply voltage 3.00 V / 1.9 V / 1.3 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption,

Standby: (Max.) Supply voltage 3.00 V / 1.9 V / 1.3 V, Tj = 60 ˚C, INCK: 0 V, light-obstructed state.

Standard luminous intensity: luminous intensity at 1/3 of the sensor saturated
Saturated luminous intensity: luminous intensity when the sensor is saturated.

AC Characteristics

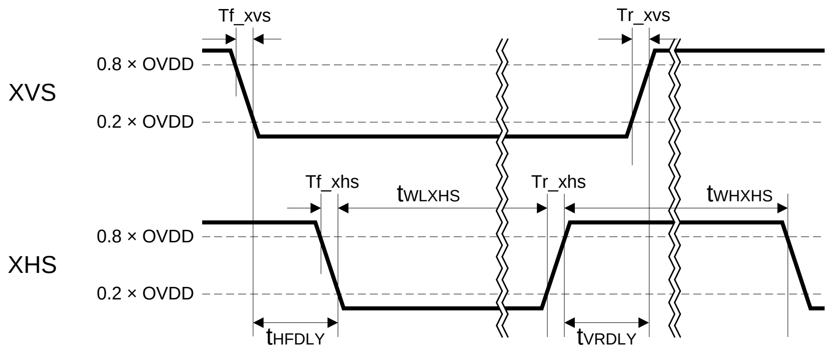
Master Clock Waveform (INCK)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

*The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics In Slave Mode (XMASTER pin = High)



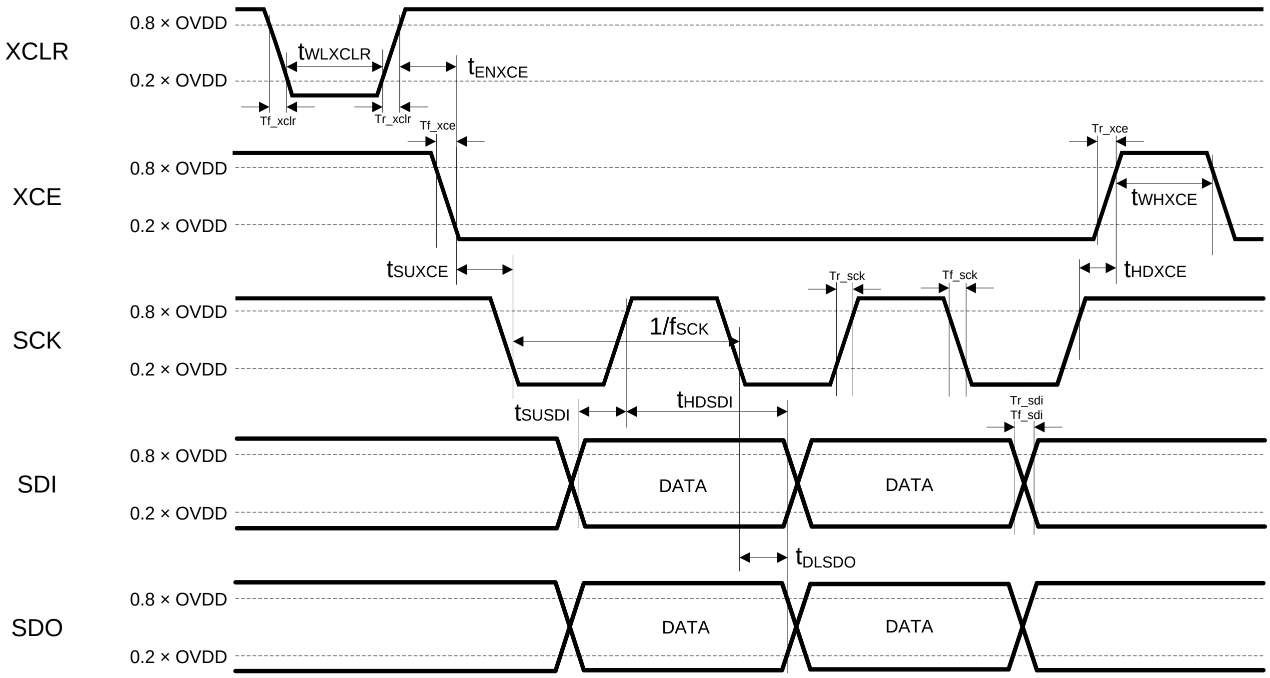
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	1 / f_{INCK}	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics In Master Mode (XMASTER pin = Low)

* XVS and XHS cannot be used for the sync signal to pixels.
Be sure to detect sync code to detect the start of effective pixels in 1 line.
For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

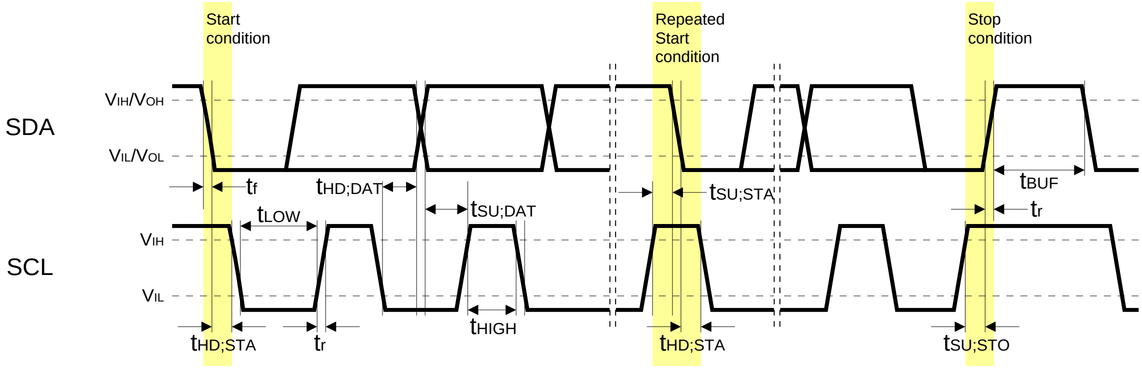
Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level pulse width	t_{WLXCLR}	4 / f_{INCK}	—	—	ns	
XCE effective margin	t_{ENXCE}	20	—	—	μs	
XCE input set-up time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input set-up time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF
XCLR Rise time	Tr_xclr	—	—	5	ns	20 % to 80 %
XCLR Fall time	Tf_xclr	—	—	5	ns	80 % to 20 %
XCE Rise time	Tr_xce	—	—	5	ns	20 % to 80 %
XCE Fall time	Tf_xce	—	—	5	ns	80 % to 20 %
SCK Rise time	Tr_sck	—	—	5	ns	20 % to 80 %
SCK Fall time	Tf_sck	—	—	5	ns	80 % to 20 %
SDI Rise time	Tr_sdi	—	—	5	ns	20 % to 80 %
SDI Fall time	Tf_sdi	—	—	5	ns	80 % to 20 %

I^2C



I^2C Specification

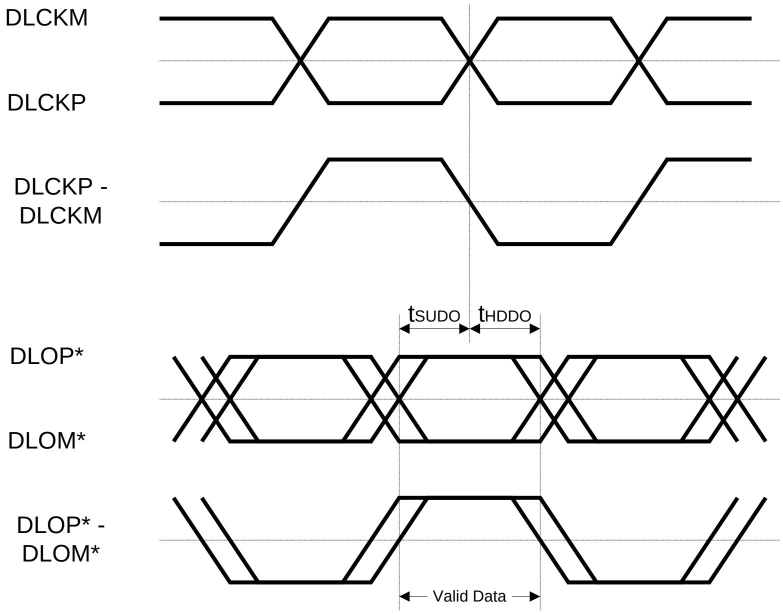
Item	Symbol	Min.	Typ.	Max.	Unit	条件
Low level input voltage	VIL	-0.3	—	$0.3 \times OV_{DD}$	V	
High level input voltage	VIH	$0.7 \times OV_{DD}$	—	1.9	V	
Low level input voltage	VOL	0	—	$0.2 \times OV_{DD}$	V	OVDD < 2 V, Sink 3 mA
High level input voltage	VOH	$0.8 \times OV_{DD}$	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, $0.7 \times OV_{DD}$ – $0.3 \times OV_{DD}$
Input current	Ii	-10	—	10	µA	$0.1 \times OV_{DD}$ – $0.9 \times OV_{DD}$
Capacitance for SCK (SCL) /SDI (SDA)	Ci	—	—	10	pF	

I^2C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	µs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	µs

DLCKP / DLCKM, DLOP / DLOM

Low Voltage LVDS DDR Output

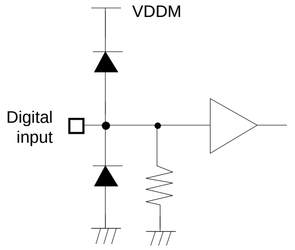
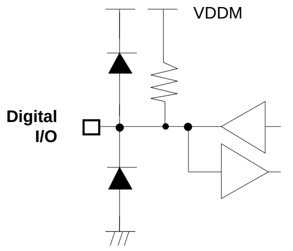
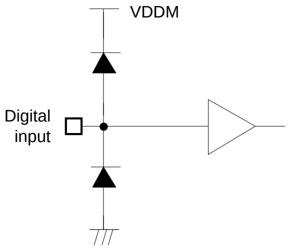
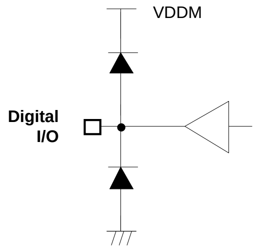
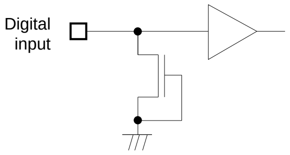
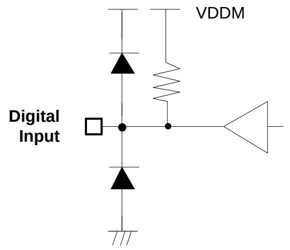
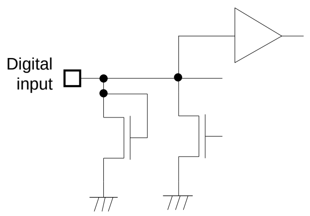
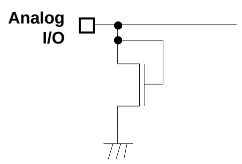
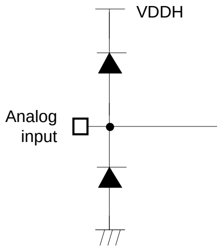
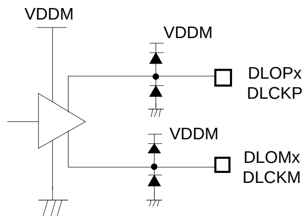
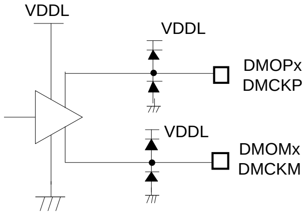


(Output load capacitance: 8 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DLCKP/DLCKM clock duty	—	40	50	60	%	DLCK = 297 MHz (Max.)
DLO set-up time	t_{SUDO}	400	—	—	ps	Data Rate 297 MHz DDR
DLO hold time	t_{HDDO}	400	—	—	ps	Data Rate 297 MHz DDR

I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
OMODE TENABLE		XVS XHS	
XMASTER XCE		SDO TOUT	
XCLR INCK		XTRIG	
SDI SCK		VRLFR VRLST	
VLOADLM VBGR TAMON		DLOPx DLONx DLCKP DLCKM	
DMOPx DMOMx DMCKP DMCKM			

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

TBD

Image Sensor Characteristics

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, All-pixel scan mode, 12 bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	TBD	TBD	—	Digit (mV)	1	1/30 s storage 12 bit converted value HCG mode
			TBD	TBD	—	Digit (mV)		1/30 s storage 12 bit converted value LCG mode
Sensitivity ratio	R / G	RG	TBD	—	TBD	—	2	—
	B / G	BG	TBD	—	TBD	—		—
Saturation signal		Vsat	TBD	—	—	Digit (mV)	3	12 bit converted value LCG mode
Video signal shading		SH	—	—	TBD	%	4	—
Vertical line		VL			TBD	µV	5	12 bit converted value LCG mode
Dark signal		Vdt	—	—	TBD	Digit (mV)	6	1/30 s storage 12 bit converted value LCG mode
Dark signal shading		ΔVdt	—	—	TBD	Digit (mV)	7	1/30 s storage 12 bit converted value LCG mode
Conversion efficiency ratio		Rcg	TBD	TBD	TBD	—	8	HCG mode / LCG mode

Note)

1. Converted value into mV using 1Digit = TBD mV for 12-bit output and 1Digit = TBD mV for 10-bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.
3. The characteristics above apply to effective pixel area that is shown below.

Zone Definition

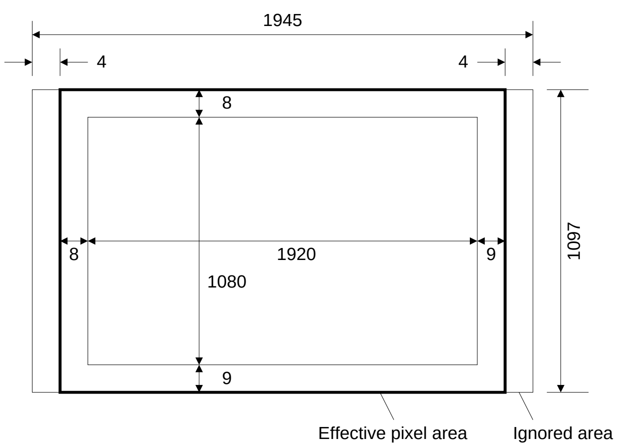


Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr / Gb channel signal output or the R / B channel signal output of the measurement system.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance - 30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   Sg = (VGr + VGb) / 2 × 100/30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 650 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signa l
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 650 mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 650 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 650 × 100 [%]

5. Vertical Line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculates eachaverage output of Gr, Gb, R and B on respective columns. Calculates maximum value of difference with adjacent column on the same color (VL [µV]).

6. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

7. Dark signal shading
   After the measurement item 5, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [mV]

8. Conversion efficiency ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 420 mV at the LCG mode, measure the average values of Gr and Gb signal output and calculate the ratio between HCG mode and LCG mode

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^2C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^2C communication is shared, so the external pin XCE must be fixed to power supply side when using I^2C communication.

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

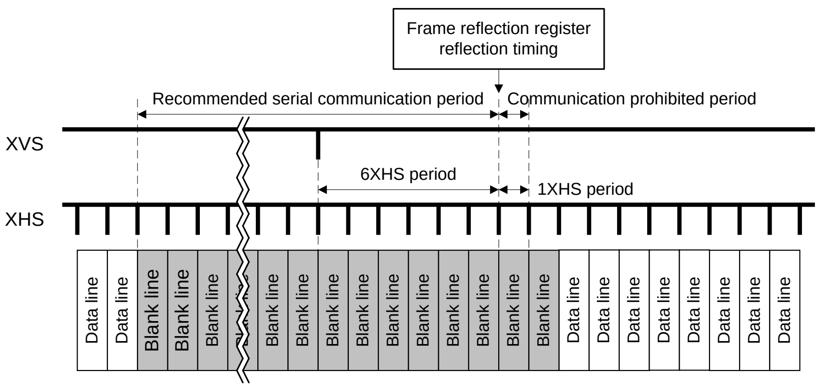
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	02h: Write to the Chip ID = 02h register 03h: Write to the Chip ID = 03h register 04h: Write to the Chip ID = 04h register 05h: Write to the Chip ID = 05h register 06h: Write to the Chip ID = 06h register 82h: Read from the Chip ID = 02h register 83h: Read from the Chip ID = 03h register 84h: Read from the Chip ID = 04h register 85h: Read from the Chip ID = 05h register 86h: Read from the Chip ID = 06h register
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within in the 6XHS period after the falling edge of XVS from the blanking line output start time after valid line of one frame is finished. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.)



Register Write and Read (4-wire)

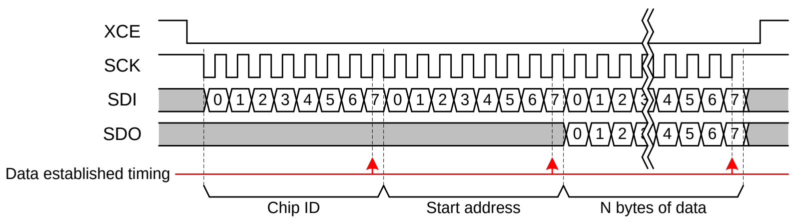
Follow the communication procedure below when writing registers.

1. Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
2. Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
3. Input Chip ID (CID = 02h or 03h or 04h or 05h or 06h) to the first byte. If the Chip ID differs, subsequent data is ignored.
4. Input the start address to the second byte. The address is automatically incremented.
5. Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
6. The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
7. Set XCE High to end communication.

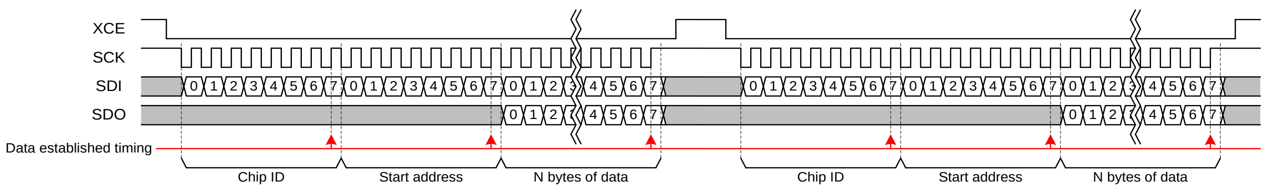
Follow the communication procedure below when reading registers.

1. Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
2. Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
3. Input Chip ID (CID = 82h or 83h or 84h or 85h or 86h) to the first byte. If the Chip ID differs, subsequent data is ignored.
4. Input the start address to the second byte. The address is automatically incremented.
5. Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
6. The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
7. Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



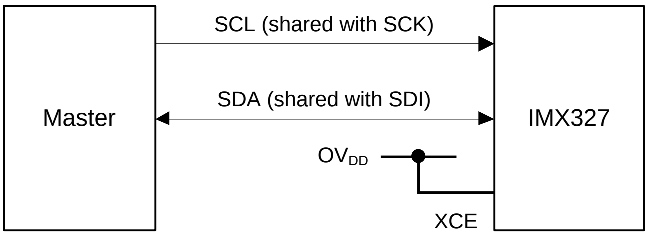
Serial Communication (Continuous Address)



Serial Communication (Discontinuous Address)

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

SLAVE Address

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R / W

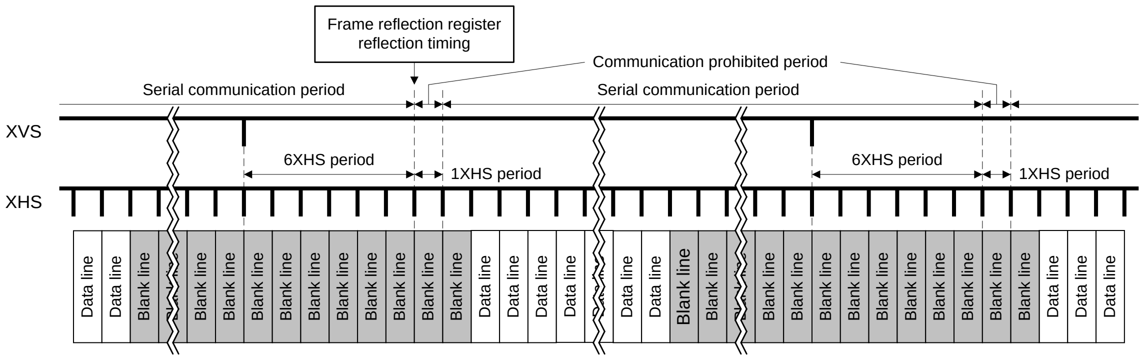
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Remarks
SCL (Common to SCK)	G2	Serial clock input
SDA (Common to SDI)	E2	Serial data communication

Register Communication Timing (I^2C)

In I^2C communication system, communication can be performed excluding during the period when communication is prohibited from the falling edge of XVS to 6H after (1H period). For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.) Using REG_HOLD function is recommended for register setting using I^2C communication. For REG_HOLD function, see “Register Transmission Setting” in “Description of Functions”.



Communication Protocol

I^2C serial communication supports a 16-bit register address and 8-bit data message type.

S	Slave Address [7:1]	R / W	A	Register Address [15:8]	A	Register Address [7:0]	A	DATA [7:0]	A / $\bar{A}$	P

From Master to Slave

From Slave to Master

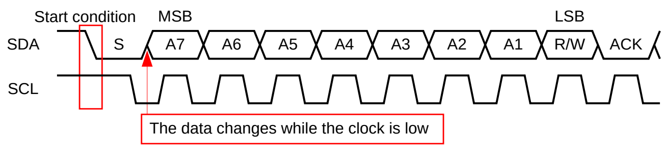
Direction depend on operation

S : Start Condition
Sr : Repeated Start Condition
P : Stop Condition
A : Acknowledge
$\bar{A}$: Negative Acknowledge

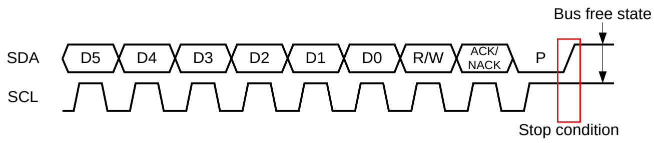
R/W=
0: Write (Master → Sensor)
1: Read (Sensor → Master)

Communication Protocol

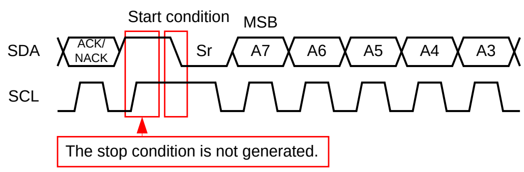
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\bar{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

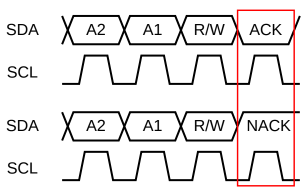


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



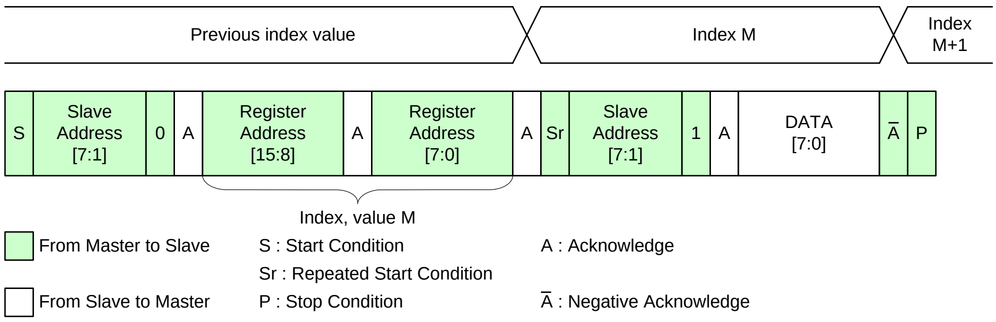
Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

This sensor corresponds to four reed modes and the two write modes.

Single Read from Random Location

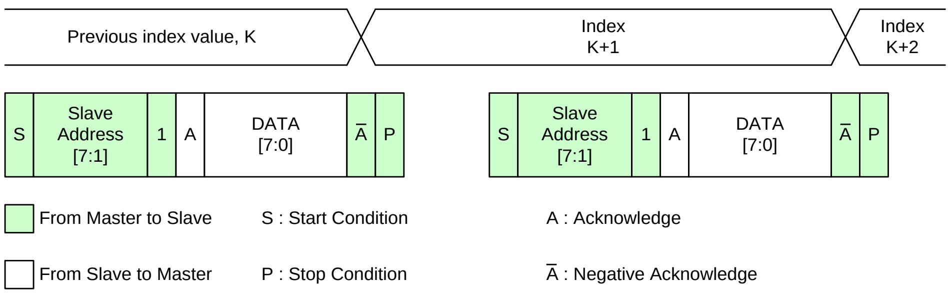
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

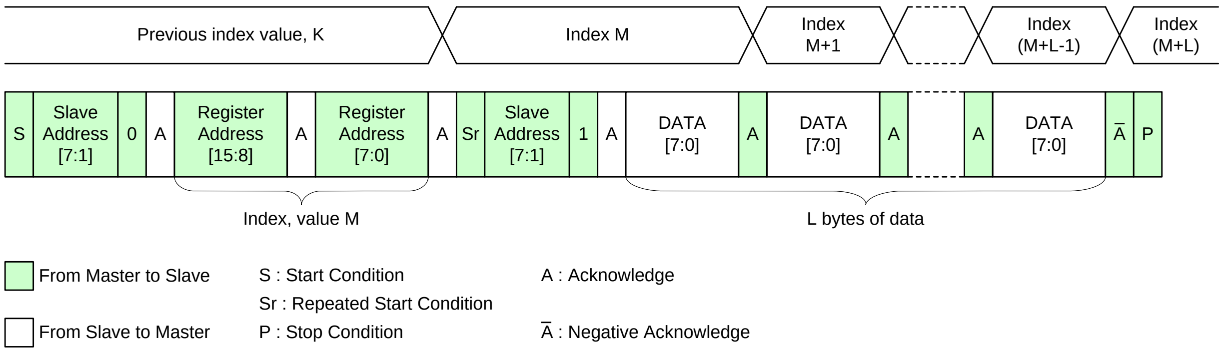
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

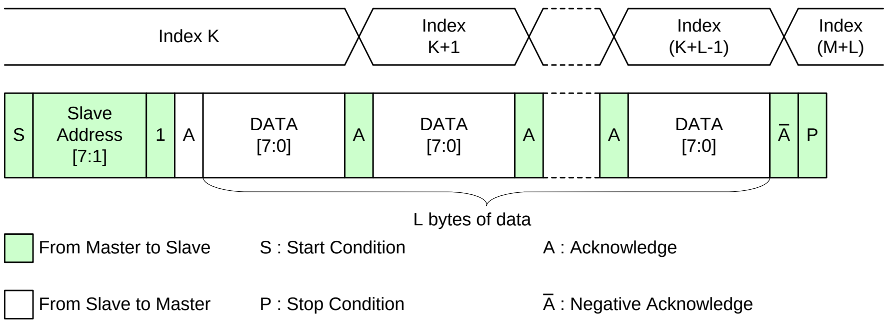
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

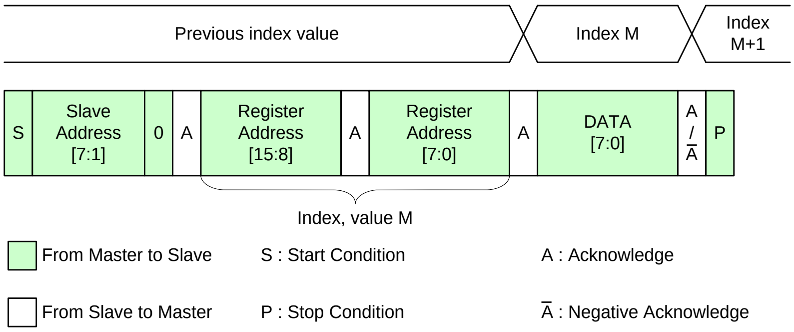
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

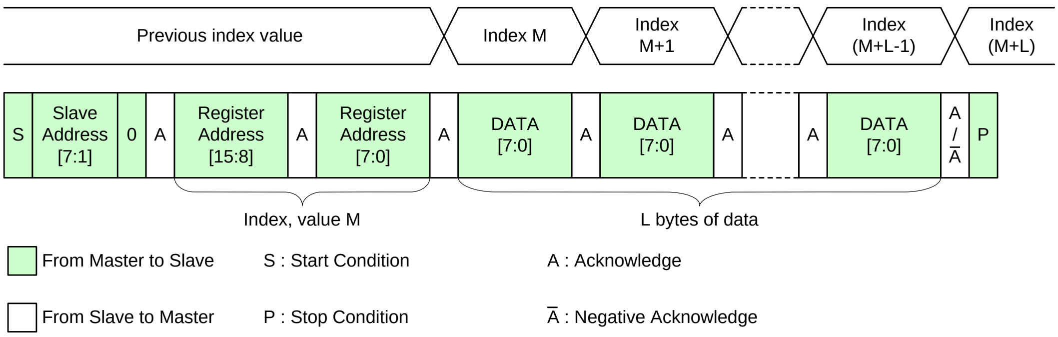
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 1280 bytes (256 × 5) of registers, composed of registers with addresses 00h to FFh that correspond to Chip ID = 02h (write mode) / 82h (read mode), Chip ID = 03h (write mode) / 83h (read mode), Chip ID = 04h (write mode) / 84h (read mode), Chip ID = 05h (write mode) / 85h (read mode), and Chip ID = 06h (write mode) / 86h (read mode). Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 1280 bytes.

The values must be changed from the default value, so initial setting after reset is required after power-on. There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than belows, set them in sensor standby state.

STANDBY
REGHOLD
XMSTA
SW_RESET
XVSOUTSEL [1:0]
XHSOUTSEL [1:0]

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h, 04h, 05h and 06h. (In I^2C communication, address; 3000h to 30FFh, 3100h to 31FFh, 3200h to 32FFh, 3300h to 33FFh, 3400h to 34FFh)

For the register that is writing " * " to the setting value in description (Indicated by red letter), change the value from the default value after the reset.

(1) Registers corresponding to Chip ID = 02h in Write mode. (Read: Chip ID = 82h)

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
00h	3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	Immediately
		1		Fixed to “0h”	0h		—
		2		Fixed to “0h”	0h		—
		3		Fixed to “0h”	0h		—
		4		Fixed to “0h”	0h		—
		5		Fixed to “0h”	0h		—
		6		Fixed to “0h”	0h		—
		7		Fixed to “0h”	0h		—
01h	3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	Immediately
		1		Fixed to “0h”	0h		—
		2		Fixed to “0h”	0h		—
		3		Fixed to “0h”	0h		—
		4		Fixed to “0h”	0h		—
		5		Fixed to “0h”	0h		—
		6		Fixed to “0h”	0h		—
		7		Fixed to “0h”	0h		—
02h	3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	Immediately
		1		Fixed to “0h”	0h		—
		2		Fixed to “0h”	0h		—
		3		Fixed to “0h”	0h		—
		4		Fixed to “0h”	0h		—
		5		Fixed to “0h”	0h		—
		6		Fixed to “0h”	0h		—
		7		Fixed to “0h”	0h		—
03h	3003h	0	SW_RESET	Software reset 0: Operating 1: Reset	0h	00h	Immediately
		1		Fixed to “0h”	0h		—
		2		Fixed to “0h”	0h		—
		3		Fixed to “0h”	0h		—
		4		Fixed to “0h”	0h		—
		5		Fixed to “0h”	0h		—
		6		Fixed to “0h”	0h		—
		7		Fixed to “0h”	0h		—
04h	3004h	[7:0]		Fixed to “10h”	10h	10h	—

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
05h	3005h	0	ADBIT	AD conversion bits setting 0: 10 bit, 1: 12 bit	1h	01h	V
		1	—	Fixed to “0h”	0h		—
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
06h	3006h	[7:0]	—	Fixed to “00h”	00h	00h	V
07h	3007h	0	VREVERSE	Vertical (V) direction readout inversion control 0: Normal, 1: Inverted	0h	00h	V
		1	HREVERSE	Horizontal (H) direction readout inversion control 0: Normal, 1: Inverted	0h		V
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4 5 6	WINMODE [2:0]	Window mode setting 0: Full HD1080p 1: HD720p 4: Window cropping from Full HD 1080p Others: Setting prohibited	0h		V
		7	—	Fixed to “0h”	0h		—
08h	3008h	[7:0]	—	Fixed to “A0h”	A0h	A0h	—
09h	3009h	0 1	FRSEL [1:0]	Frame rate (Data rate) setting For details, see the register setting list in each operation mode.	1h	01h	V
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	FDG_SEL	Conversion gain switching 0: LCG Mode 1: HCG Mode	0h		V
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—

<table>
<tr><th colspan="2">Address</th><th rowspan="2">bit</th><th rowspan="2">Register name</th><th rowspan="2">Description</th><th colspan="2">Default value after reset</th><th rowspan="2">Reflection timing</th></tr>
<tr><th>4-wire</th><th>I²C</th><th>By register</th><th>By address</th></tr>
<tr><td rowspan="8">0Ah</td><td rowspan="8">300Ah</td><td>0</td><td rowspan="9">BLKLEVEL [8:0]</td><td>LSB</td><td rowspan="9">0F0h</td><td rowspan="8">F0h</td><td rowspan="9">V</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>3</td><td></td></tr>
<tr><td>4</td><td>Black level offset value setting</td></tr>
<tr><td>5</td><td></td></tr>
<tr><td>6</td><td></td></tr>
<tr><td>7</td><td></td></tr>
<tr><td rowspan="8">0Bh</td><td rowspan="8">300Bh</td><td>0</td><td>MSB</td><td rowspan="8">00h</td></tr>
<tr><td>1</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>2</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>3</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>4</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>5</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>6</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>7</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>0Ch ～ 10h</td><td>300Ch ～ 3010h</td><td>[7:0]</td><td>—</td><td>Reserved</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>11h</td><td>3011h</td><td>[7:0]</td><td>—</td><td>Set to "0Ah"</td><td>00h</td><td>00h</td><td>Immediately</td></tr>
<tr><td>12h ～ 13h</td><td>3012h ～ 3013h</td><td>[7:0]</td><td>—</td><td>Reserved</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td rowspan="8">14h</td><td rowspan="8">3014h</td><td>0</td><td rowspan="8">GAIN [7:0]</td><td>LSB</td><td rowspan="8">00h</td><td rowspan="8">00h</td><td rowspan="8">V</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>3</td><td>Gain setting</td></tr>
<tr><td>4</td><td>(0.0 dB to 69.0 dB / 0.3 dB step)</td></tr>
<tr><td>5</td><td></td></tr>
<tr><td>6</td><td></td></tr>
<tr><td>7</td><td>MSB</td></tr>
<tr><td>15h ～ 17h</td><td>3015h ～ 3017h</td><td>[7:0]</td><td>—</td><td>Reserved</td><td>—</td><td>—</td><td>—</td></tr>
</table>

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
18h	3018h	0	VMAX [17:0]	LSB When sensor master mode vertical span setting. (Number of operation lines count from 1) For details, see the item of "Slave Mode and Master Mode" in the section of "Description of Various Functions" MSB	0465h	65h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
19h	3019h	0				04h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Ah	301Ah	0				00h	
		1					
		2	—	Fixed to "0h"	0h		—
		3	—	Fixed to "0h"	0h		—
		4	—	Fixed to "0h"	0h		—
		5	—	Fixed to "0h"	0h		—
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—
1Bh	301Bh	[7:0]	—	Fixed to "00h"	00h	00h	—
1Ch	301Ch	0	HMAX [15:0]	LSB When sensor master mode horizontal span setting. (Number of operation clocks count from 1) For details, see the item of "Slave Mode and Master Mode " in the section of "Description of Various Functions" MSB	0898h	98h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Dh	301Dh	0				08h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Eh	301Eh	[7:0]	—	Fixed to "B2h"	B2h	B2h	—
1Fh	301Fh	[7:0]	—	Fixed to "01h"	01h	01h	—

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
20h	3020h	0	SHS1 [17:0]	LSB	00000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
21h	3021h	0		Storage time adjustment Designated in line units.		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
22h	3022h	0				00h	
		1		MSB			
		2	—	Fixed to “0h”	0h		—
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
23h to 39h	3023h to 3039h	[7:0] to [7:0]		Reserved	—	—	—
3Ah	303Ah	0	WINWV_OB [3:0]	LSB In window cropping mode Cropping size designation (Vertical direction effective OB)	Ch	0Ch	V
		1					
		2					
		3		MSB			
		4	—	Fixed to “0h”	0h		
		5	—	Fixed to “0h”	0h		
		6	—	Fixed to “0h”	0h		
		7	—	Fixed to “0h”	0h		
3Bh	303Bh	[7:0]	—	Fixed to “00h”	00h	00h	—
3Ch	303Ch	0	WINPV [10:0]	LSB	000h	00h	V
		1					
		2					
		3					
		4		In window cropping mode Designation of upper left coordinate for cropping position (Vertical position)			
		5					
		6					
		7					
3Dh	303Dh	0				00h	
		1					
		2		MSB			
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
3Eh	303Eh	0	WINWV [10:0]	LSB In window cropping mode Cropping size designation (Vertical direction MSB	449h	49h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Fh	303Fh	0				04h	
		1					
		2					
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
40h	3040h	0	WINPH [10:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (horizontal position) Set to become the multiple of four MSB	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
41h	3041h	0				00h	
		1					
		2					
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
42h	3042h	0	WINWH [10:0]	LSB In window cropping mode Cropping size designation (horizontal direction) Set to become the multiple of four MSB	79Ch	9Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
43h	3043h	0				07h	
		1					
		2					
		3	—	Fixed to “0h”	0h		—
		4	—	Fixed to “0h”	0h		—
		5	—	Fixed to “0h”	0h		—
		6	—	Fixed to “0h”	0h		—
		7	—	Fixed to “0h”	0h		—
44h to 45h	3044h to 3045h	[7:0] to [7:0]	—	Reserved	—	—	—

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
46h	3046h	0	ODBIT	Number of output bit setting 0: 10 bit, 1: 12 bit * In CSI-2 mode (OMODE = Low), Fixed to "1h".	1h	E1h	Immediately
		1	—	Fixed to "0h"	0h		—
		2	—	Fixed to "0h"	0h		—
		3	—	Fixed to "0h"	0h		—
		4 5 6 7	OPORTSEL [3:0]	Output interface selection (In CSI-2, don't care. CSI-2 Interface will be selected by Chip ID: 06h register.) Dh: LVDS 2 ch Eh: LVDS 4 ch Others: Setting prohibited	Eh		Immediately
47h	3047h	[7:0]	—	Fixed to "01h"	01h	01h	—
48h	3048h	0	—	Fixed to "0h"	0h	00h	—
		1	—	Fixed to "0h"	0h		—
		2	—	Fixed to "0h"	0h		—
		3	—	Fixed to "0h"	0h		—
		4 5	XVSLNG [1:0]	XVS pulse width setting in master mode. (In slave mode, setting is invalid.) 0: 1H, 1: 2H, 2: 4H, 3: 8H	0h		Immediately
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—
49h	3049h	0	—	Fixed to "0h"	0h	08h	—
		1	—	Fixed to "0h"	0h		—
		2	—	Fixed to "0h"	0h		—
		3	—	Fixed to "1h"	1h		—
		4 5	XHSLNG [1:0]	XHS pulse width setting in master mode. (In slave mode, setting is invalid.) 0: Min. to 3: Max.	0h		Immediately
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—
4Ah	304Ah	[7:0]	—	Fixed to "00h"	00h	00h	—
4Bh	304Bh	0 1	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Fixed to High 2: VSYNC output Others: Setting prohibited	0h	00h	Immediately
		2 3	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Fixed to High 2: HSYNC output Others: Setting prohibited	0h		Immediately
		4	—	Fixed to "0h"	0h		—
		5	—	Fixed to "0h"	0h		—
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
4Ch to 5Bh	304Ch to 305Bh	[7:0] to [7:0]	—	Reserved	—	—	—
5Ch	305Ch	[7:0]	INCKSEL1	The value is set according to INCK.	0Ch	0Ch	Immediately
5Dh	305Dh	[7:0]	INCKSEL2	The value is set according to INCK.	00h	00h	Immediately
5Eh	305Eh	[7:0]	INCKSEL3	The value is set according to INCK.	10h	10h	Immediately
5Fh	305Fh	[7:0]	INCKSEL4	The value is set according to INCK.	01h	01h	Immediately
60h to 9Dh	3060h to 309Dh	[7:0] to [7:0]	—	Reserved	—	—	—
9Eh	309Eh	[7:0]	—	Set to "4Ah"	5Ah	5Ah	Immediately
9Fh	309Fh	[7:0]	—	Set to "4Ah"	5Ah	5Ah	Immediately
A0h to FFh	30A0h to 30FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(2) Registers corresponding to Chip ID = 03h in Write mode. (Read: Chip ID = 83h)

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
00h to 27h	3100h to 3127h	[7:0] to [7:0]	—	Reserved	—	—	—
28h	3128h	[7:0]	—	Set to "04h"	05h	05h	—
29h	3129h	[7:0]	ADBIT1	The value is set according to AD conversion bits 10 bit: 1Dh 12 bit: 00h	1Dh	1Dh	—
2Ah to 3Ah	312Ah to 313Ah	[7:0] to [7:0]	—	Reserved	—	—	—
3Bh	313Bh	[7:0]	—	Set to "41h"	51h	51h	—
3Ch to 5Dh	313Ch to 315Dh	[7:0] to [7:0]	—	Reserved	—	—	—
5Eh	315Eh	[7:0]	INCKSEL5	The value is set according to INCK. INCK = 74.25 MHz: 1Bh INCK = 37.125 MHz: 1Ah	1Bh	1Bh	Immediately
5Fh to 63h	315Fh to 3163h	[7:0] to [7:0]	—	Reserved	—	—	—
64h	3164h	[7:0]	INCKSEL6	The value is set according to INCK. INCK = 74.25 MHz: 1Bh INCK = 37.125 MHz: 1Ah	1Bh	1Bh	Immediately
65h to 7Bh	3165h to 317Bh	[7:0] to [7:0]	—	Reserved	—	—	—
7Ch	317Ch	[7:0]	ADBIT2	The value is set according to AD conversion bits 10 bit: 12h 12 bit: 00h	12h	12h	—
7Dh to EBh	317Dh to 31EBh	[7:0] to [7:0]	—	Reserved	—	—	—
ECh	31ECh	[7:0]	ADBIT3	The value is set according to AD conversion bits 10 bit: 37h 12 bit: 0Eh	37h	37h	—
EDh to FFh	31EDh to 31FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(3) Registers corresponding to Chip ID = 04h in Write mode. (Read: Chip ID = 84h)

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h to FFh	3200h to 32FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(4) Registers corresponding to Chip ID = 05h in Write mode. (Read: Chip ID = 85h)

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h to FFh	3300h to 33FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(5) Registers corresponding to Chip ID = 06h in Write mode. (Read: Chip ID = 86h)
* These registers are set in CSI-2 interface only.

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
00h to 04h	3400h to 3404h	[7:0] to [7:0]	—	Reserved	—	—	—
05h	3405h	0	—	Fixed to "0h"	0h	20h	—
		1	—	Fixed to "0h"	0h		—
		2	—	Fixed to "0h"	0h		—
		3	—	Fixed to "0h"	0h		—
		4	REPETITION [1:0]	* Refer to "Output signal Interface Control" section.	2h		Immediately
		5					
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—
06h	3406h	[7:0]	—	Fixed to "00h"	00h	00h	—
07h	3407h	0	PHYSICAL_LANE_NUM [1:0]	Physically connect the Lane number	3h	03h	Immediately
		1					
		2	—	Fixed to "0h"	0h		—
		3	—	Fixed to "0h"	0h		—
		4	—	Fixed to "0h"	0h		—
		5	—	Fixed to "0h"	0h		—
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—
08h to 13h	3408h to 3413h	[7:0] to [7:0]	—	Reserved	—	—	—
14h	3414h	0	OPB_SIZE_V [5:0]	LSB Vertical (V) direction OB width setting. * Refer to each operating setting. MSB	0Ah	0Ah	Immediately
		1					
		2					
		3					
		4					
		5					
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—
15h to 17h	3415h to 3417h	[7:0] to [7:0]	—	Reserved	—	—	—
18h	3418h	0	Y_OUT_SIZE [12:0]	LSB Vertical (V) direction effective pixel width setting. * Refer to each operating setting. MSB	0449h	49h	Immediately
		1					
		2					
		3					
		4					
		5					
		6					
		7					
19h	3419h	0				04h	
		1					
		2					
		3					
		4					
		5	—	Fixed to "0h"	0h		—
		6	—	Fixed to "0h"	0h		—
		7	—	Fixed to "0h"	0h		—

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
1Ah to 40h	341Ah to 3440h	[7:0] to [7:0]	—	Reserved	—	—	—
41h	3441h	[7:0]	CSI_DT_FMT [15:0]	LSB RAW10: 0A0Ah / RAW12: 0C0Ch MSB	0C0Ch	0Ch	Immediately
42h	3442h	[7:0]				0Ch	
43h	3443h	[1:0]	CSI_LANE_ MODE [1:0]	Lane number setting 0: Setting prohibited, 1: 2Lane, 3: 4Lane 2: Setting prohibited	3h	03h	Immediately
		[7:2]	—	Fixed to “00h”	00h		
44h	3444h	[7:0]	EXTCK_FREQ [15:0]	LSB Master clock frequency 2520h: INCK = 37.125 MHz 4A40h: INCK = 74.25 MHz MSB	4A40h	40h	Immediately
45h	3445h	[7:0]				4Ah	
46h	3446h	[7:0]	TCLKPOST[8:0]	Global timing setting	047h	47h	Immediately
47h	3447h	0				00h	
		[7:1]	—	Fixed to “00h”	00h		
48h	3448h	[7:0]	THSZERO[8:0]	Global timing setting	01Fh	1Fh	Immediately
49h	3449h	0				00h	
		[7:1]	—	Fixed to “00h”	00h		
4Ah	344Ah	[7:0]	THSPREPARE [8:0]	Global timing setting	017h	17h	Immediately
4Bh	344Bh	0				00h	
		[7:1]	—	Fixed to “00h”	00h		
4Ch	344Ch	[7:0]	TCLKTRAIL[8:0]	Global timing setting	00Fh	0Fh	Immediately
4Dh	344Dh	0				00h	
		[7:1]	—	Fixed to “00h”	00h		
4Eh	344Eh	[7:0]	THSTRAIL[8:0]	Global timing setting	017h	17h	Immediately
4Fh	344Fh	0				00h	
		[7:1]	—	Fixed to “00h”	00h		
50h	3450h	[7:0]	TCLKZERO[8:0]	Global timing setting	047h	47h	Immediately
51h	3451h	0				00h	
		[7:1]	—	Fixed to “00h”	00h		
52h	3452h	[7:0]	TCLKPREPARE [8:0]	Global timing setting	00Fh	0Fh	Immediately
53h	3453h	0				00h	
		[7:1]	—	Fixed to “00h”	00h		

<table>
<tr><th colspan="2">Address</th><th rowspan="2">bit</th><th rowspan="2">Register name</th><th rowspan="2">Description</th><th colspan="2">Default value after reset</th><th rowspan="2">Reflection timing</th></tr>
<tr><th>4-wire</th><th>I2C</th><th>By register</th><th>By address</th></tr>
<tr><td>54h</td><td>3454h</td><td>[7:0]</td><td rowspan="2">TLPX[8:0]</td><td rowspan="2">Global timing setting</td><td rowspan="2">00Fh</td><td>0Fh</td><td rowspan="3">Immediately</td></tr>
<tr><td rowspan="2">55h</td><td rowspan="2">3455h</td><td>0</td><td rowspan="2">00h</td></tr>
<tr><td>[7:1]</td><td>—</td><td>Fixed to “00h”</td><td>00h</td></tr>
<tr><td>56h to 71h</td><td>3456h to 3471h</td><td>[7:0] to [7:0]</td><td>—</td><td>Reserved</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td rowspan="8">72h</td><td rowspan="8">3472h</td><td>0</td><td rowspan="13">X_OUT_SIZE [12:0]</td><td rowspan="13">LSB
Horizontal (H) direction effective pixel width setting.
* Refer to each operating setting.
MSB</td><td rowspan="13">079Ch</td><td rowspan="8">9Ch</td><td rowspan="13">Immediately</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td></tr>
<tr><td>6</td></tr>
<tr><td>7</td></tr>
<tr><td rowspan="8">73h</td><td rowspan="8">3473h</td><td>0</td><td rowspan="8">07h</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>6</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>7</td><td>—</td><td>Fixed to “0h”</td><td>0h</td><td>—</td></tr>
<tr><td>74h to 7Fh</td><td>3474h to 347Fh</td><td>[7:0] to [7:0]</td><td>—</td><td>Reserved</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>80h</td><td>3480h</td><td>[7:0]</td><td>INCKSEL7</td><td>The value is set according to INCK.
INCK = 74.25 MHz: 92h
INCK = 37.125 MHz: 49h</td><td>92h</td><td>92h</td><td>Immediately</td></tr>
<tr><td>81h to FFh</td><td>3481h to 34FFh</td><td>[7:0] to [7:0]</td><td>—</td><td>Reserved</td><td>—</td><td>—</td><td>—</td></tr>
</table>

Readout Drive mode

The table below lists the operating modes available with this sensor. (N/A: Not supported mode)

<table>
<tr><th rowspan="3">Window</th><th rowspan="3">Mode</th><th rowspan="3">INCK [MHz]</th><th rowspan="3">AD conversion [bit]</th><th rowspan="3">Output bit width [bit]</th><th rowspan="3">Frame rate [frame/s]</th><th colspan="4">Data rate</th></tr>
<tr><th colspan="2">Serial LVDS [Mbps/ch]</th><th colspan="2">CSI-2 [Mbps/Lane]</th></tr>
<tr><th>2 ch</th><th>4 ch</th><th>2 Lane</th><th>4 Lane</th></tr>
<tr><td rowspan="4">Full HD 1080p</td><td rowspan="2">All pixel</td><td rowspan="2">37.125
74.25</td><td>10/12</td><td>10/12</td><td>30 / 25</td><td>445.5</td><td>222.75</td><td>445.5</td><td>222.75</td></tr>
<tr><td>10/12</td><td>10/12</td><td>60 / 50</td><td>N/A</td><td>445.5</td><td>891</td><td>445.5</td></tr>
<tr><td rowspan="2">Window cropping</td><td rowspan="2">37.125
74.25</td><td>10/12</td><td>10/12</td><td>*1</td><td>445.5</td><td>222.75</td><td>445.5</td><td>222.75</td></tr>
<tr><td>10/12</td><td>10/12</td><td>*2</td><td>N/A</td><td>445.5</td><td>891</td><td>445.5</td></tr>
<tr><td rowspan="2">HD720p</td><td rowspan="2">All-pixel</td><td rowspan="2">37.125
74.25</td><td>10/12</td><td>10/12</td><td>30</td><td>297</td><td>148.5</td><td>297</td><td>148.5</td></tr>
<tr><td>10/12</td><td>10/12</td><td>60</td><td>594</td><td>297</td><td>594</td><td>297</td></tr>
</table>

*1: FRSEL = 2h

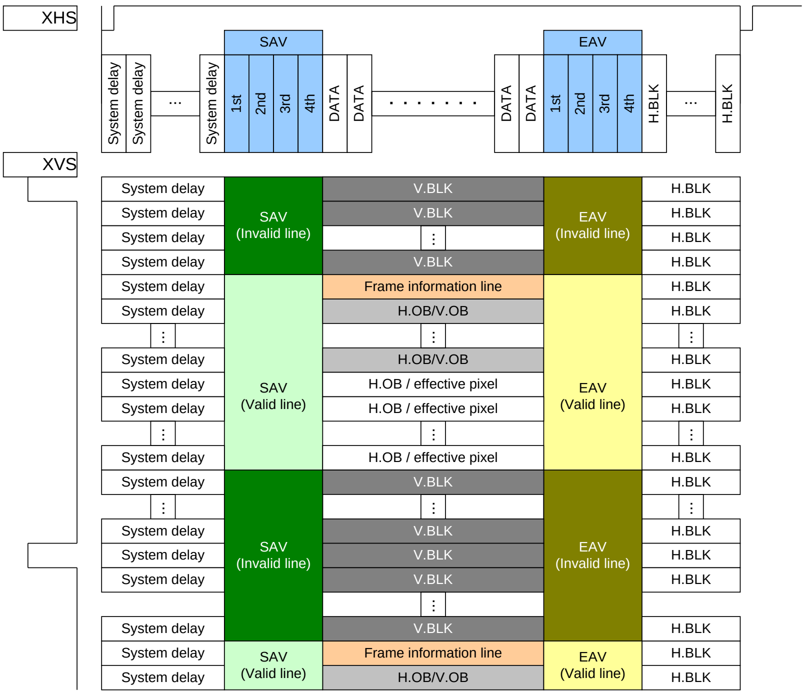
*2: FRSEL = 1h

Window	Mode	INCK [MHz]	Frame rate [frame/s]	Recording pixels		Total number of pixels			1H period [µs]
				H [pixels]	V [lines]	H [pixels] LVDS CSI-2 (10 bit)	H [pixels] LVDS CSI-2 (12 bit)	V [lines]	
Full HD 1080p	All-pixel	37.125 74.25	25	1920	1080	3168	2640	1125	35.6
			30			2640	2200		29.6
			50			3168	2640		17.8
			60			2640	2200		14.8
	Window cropping	37.125 74.25	*1	*3	*3	2640	2200	*4	29.6
			*2						14.8
HD720p	All-pixel	37.125 74.25	25	1280	720	3168	2640	750	53.3
			30			2640	2200		44.4
			50			3168	2640		26.7
			60			2640	2200		22.2

*1: FRSEL = 2h
*2: FRSEL = 1h
*3: Arbitrary value that was designated to cropping area
*4: Please refer to description of window cropping mode

Sync code (Serial LVDS output)

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd.
(BLK: Blanking period)



Sync Code Output Timing

List of Sync Code

Sync code	1st code		2nd code		3rd code		4th code	
	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit
SAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2D8h	B60h

(Note 1) They are output to each channel seriously in MSB first when low-voltage LVDS serial.
For details, see the item of "Signal output" and "Output pin setting".

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.

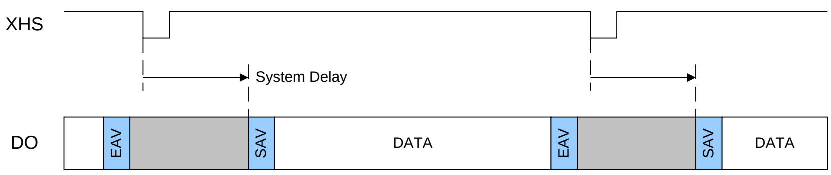


Image Data Output Format (CSI-2 output)

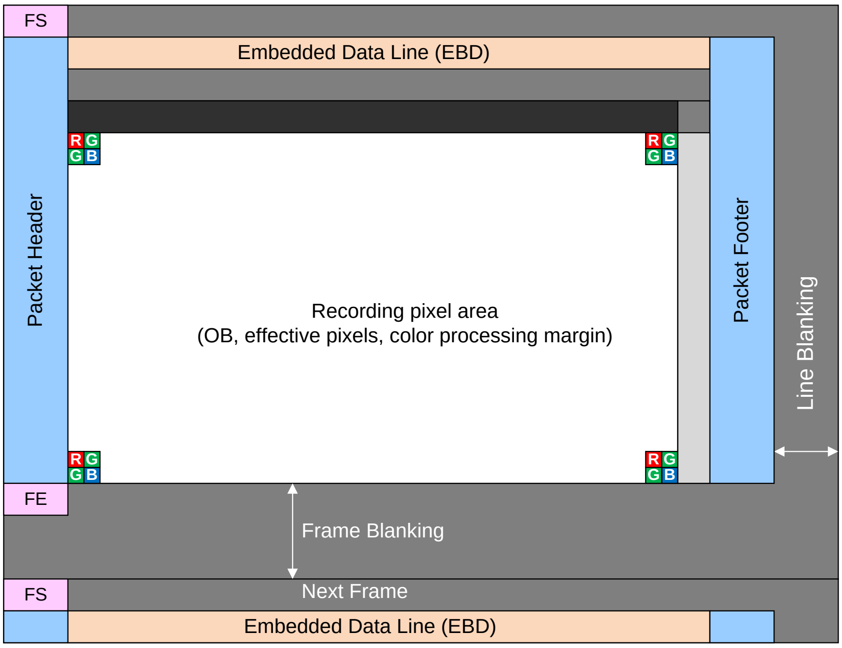
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
10h	NULL	N/A	Invalid data
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 41h, 42h (3441h, 3442h) CSI_DT_FMT [15:0]	0A0Ah
2Ch	RAW12		0C0Ch
37h	OB Data	N/A	Vertical OB line data

Frame Structure



Frame Structure of CSI-2 output

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.

Embedded Data Format

Packet Header	0Ah	Tag	Data	Tag	Data	Tag	Data	Tag	Data	Tag	Data	07h	07h	Packet Footer	

RAW10 (CSI_DT_FMT = 0A0Ah)

Packet Header	0Ah	Tag	Data	Tag	55h	Data	Tag	Data	Tag	55h	Data	Tag	Data	07h	55h	Packet Footer

RAW12 (CSI_DT_FMT = 0C0Ch)

Packet Header	0Ah	Tag	55h	Data	Tag	55h	Data	Tag	55h	Data	Tag	55h	Data	07h	55h	Packet Footer

The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data.
07h	End of Data.
AAh	CCI Register Index MSB [15:8]
A5h	CCI Register Index LSB [7:0]
5Ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
FFh	Illegal Tag. If found treat as end of Data.

Specific output examples are shown below. (4-wire: Chip ID = 05h)

TBD

Image Data Output Format

All-pixel scan mode (Full HD 1080p)

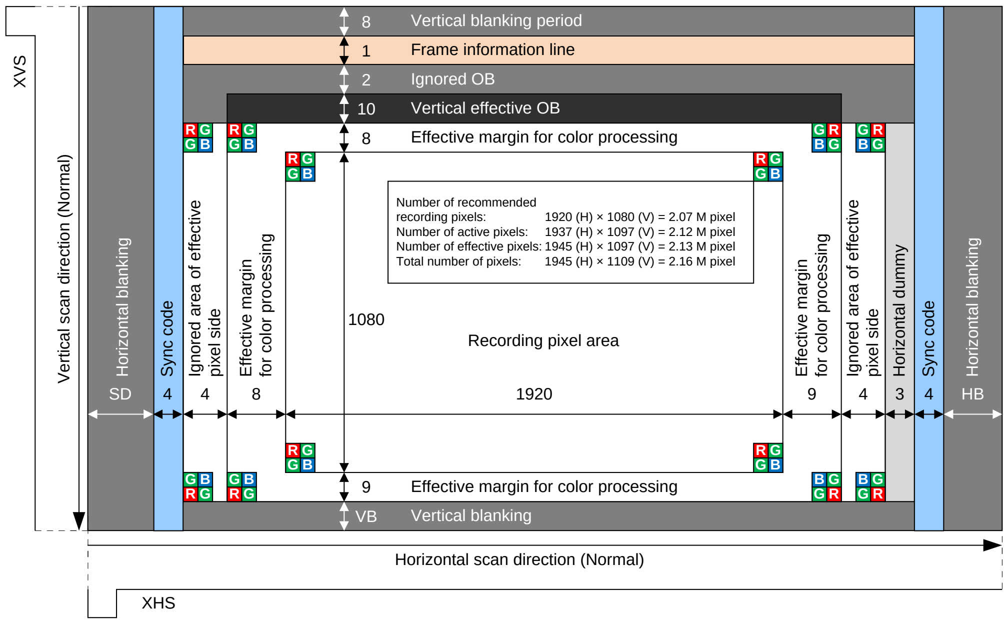
List of Setting Register for LVDS serial output

Address		bit	Register Name	Initial Value	LVDS serial		備考
4-wire	I^{2}C				2 ch	4 ch	
Chip ID: 02h							
05h	3005h	[0]	ADBIT	1h	0h / 1h		0: 10 bit, 1: 12 bit
07h	3007h	[0]	VREVERSE	0h	0h / 1h		0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h		0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	0h		Full HD 1080p
09h	3009h	[1:0]	FRSEL	1h	2h		30 / 25 [frame/s]
					N/A	1h	60 / 50 [frame/s]
		[4]	FDG_SEL	0h	0h / 1h		0: LCG mode, 1: HCG mode
12h	3012h	[7:0]	—	F0h	64h		Initial setting
13h	3013h	[7:0]	—	00h	00h		Initial setting
18h	3018h	[7:0]	VMAX	465h	465h		25 /30 / 50 / 60 [frame/s]
19h	3019h	[7:0]					
1Ah	301Ah	[1:0]					
1Ch	301Ch	[7:0]	HMAX	0898h	1130h / 14A0h		1130h: 30[frame/s] / 14A0h: 25[frame/s]
1Dh	301Dh	[7:0]			N/A	0898h / 0A50h	0898h: 60[frame/s] / 0A50h: 50[frame/s]
46h	3046h	[1:0]	ODBIT	1h	0h / 1h		0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	Eh	Dh	Eh	I/F selection
5Ch	305Ch	[7:0]	INCKSEL1	0Ch	0Ch /18h		Set according to INCK 74.25 / 37.125 MHz
5Dh	305Dh	[7:0]	INCKSEL2	00h	00h / 00h		
5Eh	305Eh	[7:0]	INCKSEL3	10h	10h / 20h		
5Fh	305Fh	[7:0]	INCKSEL4	01h	01h / 01h		
Chip ID = 03h							
29h	3129h	[7:0]	ADBIT1	1Dh	1Dh / 00h		10 bit: 1Dh 12 bit: 00h
5Eh	315Eh	[7:0]	INCKSEL5	1Bh	1Bh / 1Ah		INCK: 74.25 / 37.125 MHz
64h	3164h	[7:0]	INCKSEL6	1Bh	1Bh / 1Ah		INCK: 74.25 / 37.125 MHz
7Ch	317Ch	[7:0]	ADBIT2	12h	12h / 00h		10 bit: 12h 12 bit: 00h
ECh	31ECh	[7:0]	ADBIT3	37h	37h / 0Eh		10 bit: 37h 12 bit: 0Eh
Chip ID = 04h							
00h ~ FFh	3200h ~ 32FFh	[7:0] ~ [7:0]	Set register value that described on item "Register map".				
Chip ID = 05h							
00h ~ FFh	3300h ~ 33FFh	[7:0] ~ [7:0]	Set register value that described on item "Register map".				
Chip ID = 06h							
00h ~ 7Fh	3400h ~ 347Fh	[7:0] ~ [7:0]	Changing the value is not necessary.				
80h	3480h	[7:0]	INCKSEL7	92h	92h / 49h		INCK: 74.25 / 37.125 MHz
81h ~ FFh	3481h ~ 34FFh	[7:0] ~ [7:0]	Changing the value is not necessary.。				

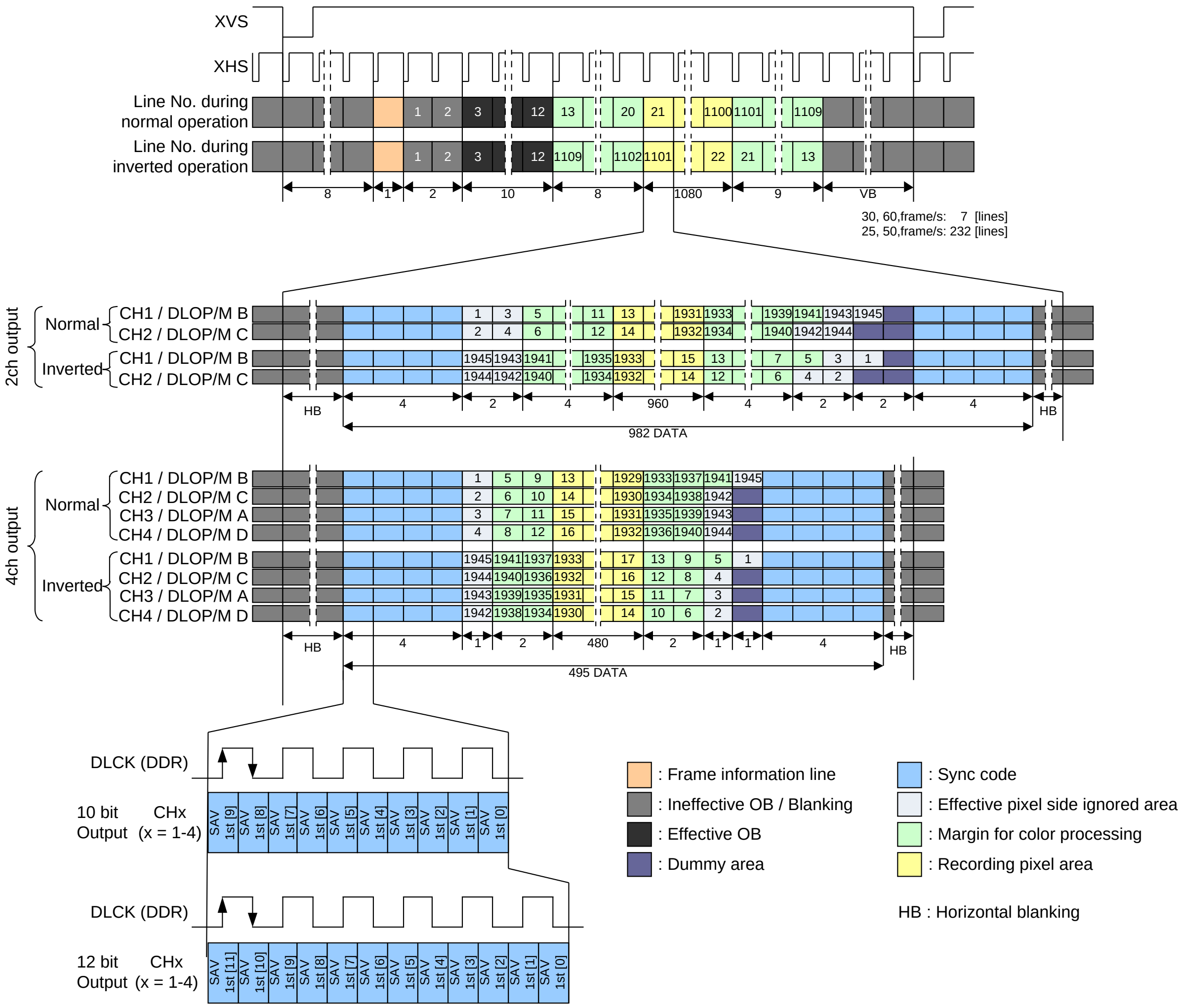
List of Setting Register for CSI-2 serial output

Address 4-wire	Address I²C	bit	Register Name	Initial Value	CSI-2 serial 2 lane 30 / 25 [frame /s]	CSI-2 serial 2 lane 60 / 50 [frame /s]	CSI-2 serial 4 lane 30 / 25 [frame /s]	CSI-2 serial 4 lane 60 / 50 [frame /s]	Remarks
Chip ID: 02h									
05h	3005h	[0]	ADBIT	1h	0h / 1h				0: 10 bit, 1: 12 bit
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	0h				Full HD 1080p
09h	3009h	[1:0]	FRSEL	1h	2h	1h	2h	1h	
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
12h	3012h	[7:0]	—	F0h	64h				Initial setting
13h	3013h	[7:0]	—	00h	00h				Initial setting
18h	3018h	[7:0]	VMAX	465h	465h				25 /30 / 50 / 60 [frame/s]
19h	3019h	[7:0]							
1Ah	301Ah	[1:0]							
1Ch	301Ch	[7:0]	HMAX	0898h	1130h / 14A0h	0898h / 0A50h	1130h / 14A0h	0898h / 0A50h	30 / 60[frame / s] / 25 / 50[frame / s]
1Dh	301Dh	[7:0]							
46h	3046h	[1:0]	ODBIT	1h	1h				In CSI-2, fixed to “1h”.
		[7:4]	OPORTSEL	Eh	0h				In CSI-2, fixed to “0h”.
5Ch	305Ch	[7:0]	INCKSEL1	0Ch	0Ch / 18h				Set according to INCK 74.25 / 37.125 MHz
5Dh	305Dh	[7:0]	INCKSEL2	00h	03h / 03h				
5Eh	305Eh	[7:0]	INCKSEL3	10h	10h / 20h				
5Fh	305Fh	[7:0]	INCKSEL4	01h	01h / 01h				
Chip ID: 03h									
29h	3129h	[7:0]	ADBIT1	1Dh	1Dh / 00h				10 bit: 1Dh 12 bit: 00h
5Eh	315Eh	[7:0]	INCKSEL5	1Bh	1Bh / 1Ah				Set according to INCK 74.25 / 37.125 MHz
64h	3164h	[7:0]	INCKSEL6	1Bh	1Bh / 1Ah				Set according to INCK 74.25 / 37.125 MHz
7Ch	317Ch	[7:0]	ADBIT2	12h	12h / 00h				10 bit: 12h 12 bit: 00h
ECh	31ECh	[7:0]	ADBIT3	37h	37h / 0Eh				10 bit: 37h 12 bit: 0Eh
Chip ID: 04h									
00h ~ FFh	3200h ~ 32FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.						
Chip ID: 05h									
00h ~ FFh	3300h ~ 33FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.						

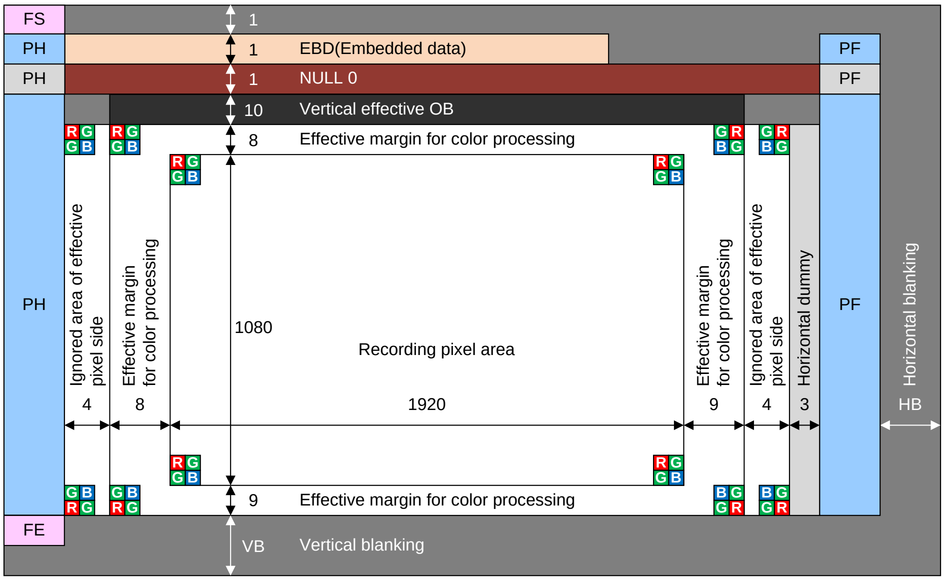
Address		bit	Register Name	Initial Value	CSI-2 serial				Remarks
					2 lane		4 lane		
4-wire	I^{2}C				30 / 25 [frame /s]	60 / 50 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	
Chip ID = 06h									
				Data rate	445.5	891	222.75	445.5	[Mbps / Lane]
05h	3405h	[5:4]	REPETITION	2h	1h	0h	2h	1h	
07h	3407h	[1:0]	PHYSICAL_ LANE_NUM	3h	1h		3h		
14h	3414h	[5:0]	OPB_SIZE_V	Ah	Ah				
18h	3418h	[7:0]	Y_OUT_SIZE	0449h	0449h				
19h	3419h	[4:0]							
41h	3441h	[7:0]	CSI_DT_FMT	0C0Ch	0A0Ah / 0C0Ch				0A0Ah: RAW10 / 0C0Ch: RAW12
42h	3442h	[7:0]							
43h	3443h	[1:0]	CSI_LANE_ MODE	3h	1h		3h		
44h	3444h	[7:0]	EXTCK_FREQ	4A40h	37.125 MHz :2520h 74.25 MHz :4A40h				Set according to INCK
45h	3445h	[7:0]							
46h	3446h	[7:0]	TCLKPOST	047h	057h	077h	047h	057h	Global timing
47h	3447h	[0]							
48h	3448h	[7:0]	THSZERO	01Fh	037h	067h	01Fh	037h	Global timing
49h	3449h	[0]							
4Ah	344Ah	[7:0]	THSPREPARE	017h	01Fh	047h	017h	01Fh	Global timing
4Bh	344Bh	[0]							
4Ch	344Ch	[7:0]	TCLKTRAIL	00Fh	01Fh	037h	00Fh	01Fh	Global timing
4Dh	344Dh	[0]							
4Eh	344Eh	[7:0]	THSTRAIL	017h	01Fh	03Fh	017h	01Fh	Global timing
4Fh	344Fh	[0]							
50h	3450h	[7:0]	TCLKZERO	047h	077h	0FFh	047h	077h	Global timing
51h	3451h	[0]							
52h	3452h	[7:0]	TCLKPREPARE	00Fh	01Fh	03Fh	00Fh	01Fh	Global timing
53h	3453h	[0]							
54h	3454h	[7:0]	TLPX	00Fh	017h	037h	00Fh	017h	Global timing
55h	3455h	[0]							
72h	3472h	[7:0]	X_OUT_SIZE	079Ch	079Ch				
73h	3473h	[4:0]							
80h	3480h	[7:0]	INCKSEL7	92h	37.125 MHz :49h 74.25 MHz :92h				Set according to INCK



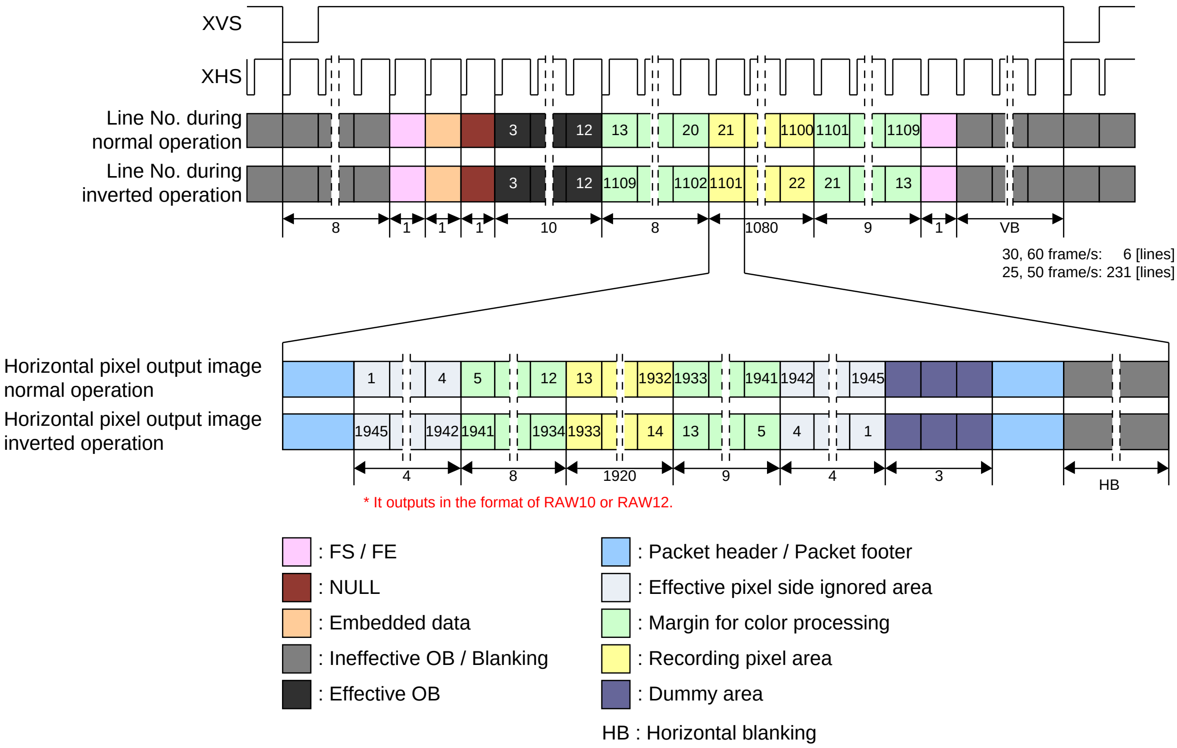
Pixel Array Image Drawing in Full HD 1080p mode (Serial LVDS output)



Drive Timing Chart for Full HD 1080p mode (Serial LVDS output)



Pixel Array Image Drawing in Full HD 1080p mode (CSI-2 serial output)



Drive Timing Chart for Full HD 1080p mode (CSI-2 serial output)

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
Cropping position is set, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from all-pixel scan mode and vertical, horizontal period and frame rate are fixed to the value for this mode. Pixels cropped by horizontal cropping setting are output with left justified and that extends the horizontal blanking period.
Window cropping image is shown in the figure below.
Cropping position is set, regarding effective pixel start position as origin (0, 0) in all pixel scan mode.
Only vertical width can be set for OB (horizontal width is the same as the Window cropping width).

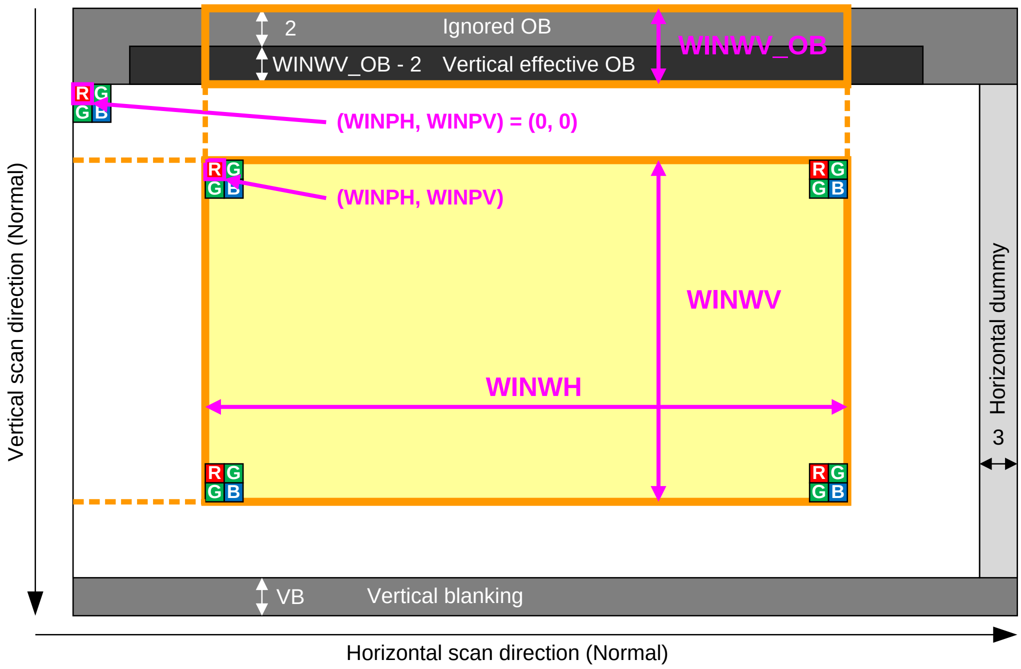


Image Drawing of Window Cropping Mode

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

WINPH + WINWH ≤ 1944
368 ≤ WINWH
Set WINPH and WINWH to a multiple of 4.

V_{TTL} (Number of lines per frame or VMAX) ≥ WINWV_OB + WINWV + 13

However,
6 ≤ WINWV_OB ≤ 12
WINPV + WINWV ≤ 1096
304 ≤ WINWV
OB_SIZE_V = WINWV_OB - 2 (In CSI-2 output)
Y_OUT_SIZE = WINWV (In CSI-2 output)

Frame rate on Window cropping mode
Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))

1H period (unit: [µs]) : Fix 1H time in a mode before cropping and calculate it by the value of "Number of INCK in 1H" in the table of "Operating Mode" and "List of Operation Modes and Output Rates".

List of Setting Register for LVDS serial output

Address 4-wire	Address I²C	bit	Register Name	Initial Value	LVDS serial 2 ch	LVDS serial 4 ch	備考
Chip ID: 02h							
05h	3005h	[0]	ADBIT	1h	0h / 1h		0: 10 bit, 1: 12 bit
07h	3007h	[0]	VREVERSE	0h	0h / 1h		0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h		0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	4h		Window cropping
09h	3009h	[1:0]	FRSEL	1h	2h		
					N/A	1h	
		[4]	FDG_SEL	0h	0h / 1h		0: LCG mode, 1: HCG mode
12h	3012h	[7:0]	—	F0h	64h		Initial setting
13h	3013h	[7:0]	—	00h	00h		Initial setting
18h	3018h	[7:0]	VMAX	465h	V_{TTL}		See previous page.
19h	3019h	[7:0]					
1Ah	301Ah	[1:0]					
1Ch	301Ch	[7:0]	HMAX	0898h	1130h / 14A0h		1130h: 30[frame/s] / 14A0h: 25[frame/s]
1Dh	301Dh	[7:0]			N/A	0898h / 0A50h	0898h: 60[frame/s] / 0A50h: 50[frame/s]
46h	3046h	[1:0]	ODBIT	1h	0h / 1h		0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	Eh	Dh	Eh	I/F selection
5Ch	305Ch	[7:0]	INCKSEL1	0Ch	0Ch / 18h		Set according to INCK 74.25/37.125 MHz
5Dh	305Dh	[7:0]	INCKSEL2	00h	00h / 00h		
5Eh	305Eh	[7:0]	INCKSEL3	10h	10h / 20h		
5Fh	305Fh	[7:0]	INCKSEL4	01h	01h / 01h		
Chip ID = 03h							
29h	3129h	[7:0]	ADBIT1	1Dh	1Dh / 00h		10 bit: 1Dh 12 bit: 00h
5Eh	315Eh	[7:0]	INCKSEL5	1Bh	1Bh / 1Ah		INCK : 74.25 / 37.125 MHz
64h	3164h	[7:0]	INCKSEL6	1Bh	1Bh / 1Ah		INCK : 74.25 / 37.125 MHz
7Ch	317Ch	[7:0]	ADBIT2	12h	12h / 00h		10 bit: 12h 12 bit: 00h
ECh	31ECh	[7:0]	ADBIT3	37h	37h / 0Eh		10 bit: 37h 12 bit: 0Eh
Chip ID = 04h							
00h ~ FFh	3200h ~ 32FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.				
Chip ID = 05h							
00h ~ FFh	3300h ~ 33FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.。				
Chip ID = 06h							
00h ~ 7Fh	3400h ~ 347Fh	[7:0] ~ [7:0]	Changing the value is not necessary.				
80h	3480h	[7:0]	INCKSEL7	92h	92h / 49h		INCK: 74.25 / 37.125 MHz
81h ~ FFh	3481h ~ 34FFh	[7:0] ~ [7:0]	Changing the value is not necessary.				

List of Setting Register for CSI-2 serial output

Address 4-wire	Address I²C	bit	Register Name	Initial Value	CSI-2 serial 2 lane *1 [frame /s]	CSI-2 serial 2 lane *2 [frame /s]	CSI-2 serial 4 lane *1 [frame /s]	CSI-2 serial 4 lane *2 [frame /s]	Remarks
Chip ID: 02h									
05h	3005h	[0]	ADBIT	1h	0h / 1h				0: 10 bit, 1: 12 bit
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	4h				Window cropping
09h	3009h	[1:0]	FRSEL	1h	2h	1h	2h	1h	
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
12h	3012h	[7:0]	—	F0h	64h				Initial setting
13h	3013h	[7:0]	—	00h	00h				Initial setting
18h	3018h	[7:0]	VMAX	465h	V_{TTL}				See previous page.
19h	3019h	[7:0]							
1Ah	301Ah	[1:0]							
1Ch	301Bh	[7:0]	HMAX	0898h	1130h / 14A0h	0898h / 0A50h	1130h / 14A0h	0898h / 0A50h	465h: 30 / 60[frame / s] / 546h: 25 / 50[frame / s]
1Dh	301Ch	[7:0]							
46h	3046h	[1:0]	ODBIT	1h	1h				In CSI-2, fixed to "1h".
		[7:4]	OPORTSEL	Eh	0h				In CSI-2, fixed to "0h".
5Ch	305Ch	[7:0]	INCKSEL1	0Ch	0Ch / 18h				Set according to INCK 74.25/37.125 MHz
5Dh	305Dh	[7:0]	INCKSEL2	00h	03h / 03h				
5Eh	305Eh	[7:0]	INCKSEL3	10h	10h / 20h				
5Fh	305Fh	[7:0]	INCKSEL4	01h	01h / 01h				
Chip ID = 03h									
29h	3129h	[7:0]	ADBIT1	1Dh	1Dh / 00h				10 bit: 1Dh 12 bit: 00h
5Eh	315Eh	[7:0]	INCKSEL5	1Bh	1Bh / 1Ah				Set according to INCK 74.25 / 37.125 MHz
64h	3164h	[7:0]	INCKSEL6	1Bh	1Bh / 1Ah				Set according to INCK 74.25 / 37.125 MHz
7Ch	317Ch	[7:0]	ADBIT2	12h	12h / 00h				10 bit: 12h 12 bit: 00h
ECh	31ECh	[7:0]	ADBIT3	37h	37h / 0Eh				10 bit: 37h 12 bit: 0Eh
Chip ID = 04h									
00h ~ FFh	3200h ~ 32FFh	[7:0] ~ [7:0]	Set register value that described on item "Register map".						
Chip ID = 05h									
00h ~ FFh	3300h ~ 33FFh	[7:0] ~ [7:0]	Set register value that described on item "Register map".						

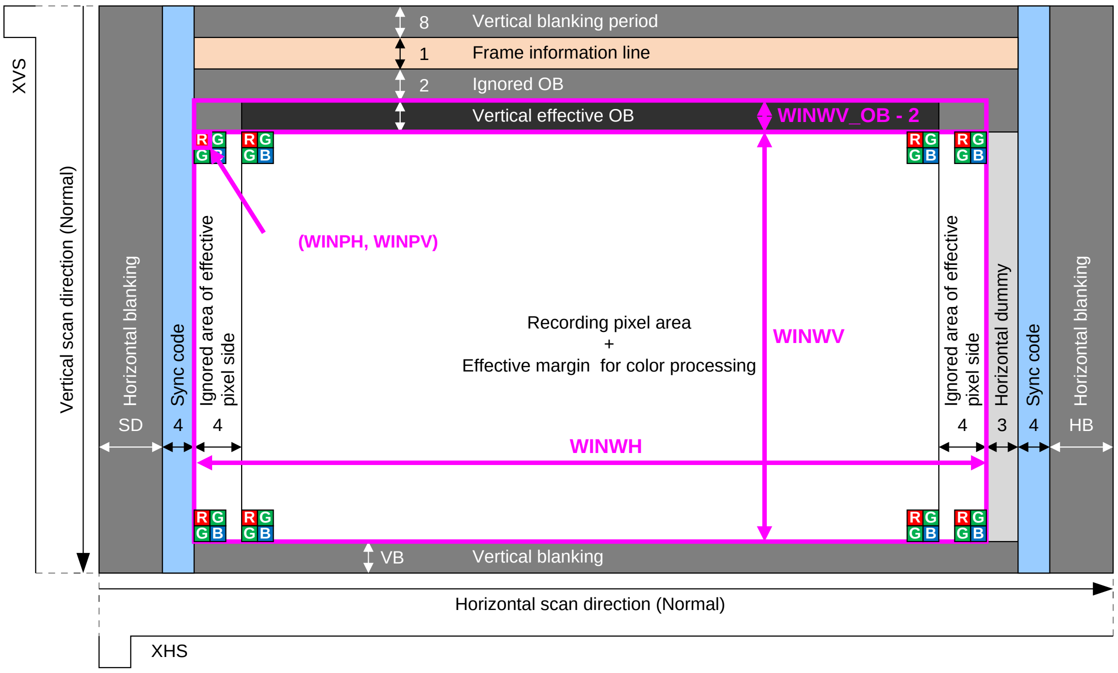
Address 4-wire	Address I²C	bit	Register Name	Initial Value	CSI-2 serial 2 lane *1 [frame /s]	CSI-2 serial 2 lane *2 [frame /s]	CSI-2 serial 4 lane *1 [frame /s]	CSI-2 serial 4 lane *2 [frame /s]	Remarks
Chip ID = 06h									
				Data rate	445.5	891	222.75	445.5	[Mbps / Lane]
05h	3405h	[5:4]	REPETITION	2h	1h	0h	2h	1h	
07h	3407h	[1:0]	PHYSICAL_ LANE_NUM	3h	1h		3h		
14h	3414h	[5:0]	OPB_SIZE_V	Ah	Ah				
18h	3418h	[7:0]	Y_OUT_SIZE	0449h	0449h				
19h	3419h	[4:0]							
41h	3441h	[7:0]	CSI_DT_FMT	0C0Ch	0A0Ah / 0C0Ch				0A0Ah: RAW10 / 0C0Ch: RAW12
42h	3442h	[7:0]							
43h	3443h	[1:0]	CSI_LANE_ MODE	3h	1h		3h		
44h	3444h	[7:0]	EXTCK_FREQ	4A40h	37.125 MHz : 2520h 74.25 MHz: 4A40h				Set according to INCK
45h	3445h	[7:0]							
46h	3446h	[7:0]	TCLKPOST	047h	057h	077h	047h	057h	Global timing
47h	3447h	[0]							
48h	3448h	[7:0]	THSZERO	01Fh	037h	067h	01Fh	037h	Global timing
49h	3449h	[0]							
4Ah	344Ah	[7:0]	THSPREPARE	017h	01Fh	047h	017h	01Fh	Global timing
4Bh	344Bh	[0]							
4Ch	344Ch	[7:0]	TCLKTRAIL	00Fh	01Fh	037h	00Fh	01Fh	Global timing
4Dh	344Dh	[0]							
4Eh	344Eh	[7:0]	THSTRAIL	017h	01Fh	03Fh	017h	01Fh	Global timing
4Fh	344Fh	[0]							
50h	3450h	[7:0]	TCLKZERO	047h	077h	0FFh	047h	077h	Global timing
51h	3451h	[0]							
52h	3452h	[7:0]	TCLKPREPARE	00Fh	01Fh	03Fh	00Fh	01Fh	Global timing
53h	3453h	[0]							
54h	3454h	[7:0]	TLPX	00Fh	017h	037h	00Fh	017h	Global timing
55h	3455h	[0]							
72h	3472h	[7:0]	X_OUT_SIZE	079Ch	079Ch				
73h	3473h	[4:0]							
80h	3480h	[7:0]	INCKSEL7	92h	37.125 MHz : 49h 74.25 MHz : 92h				Set according to INCK

The example of window cropping setting is shown below.
The frame rate is maximum setting as each image format. For adjust the frame rate, please extend the VMAX or the number of lines per frame.

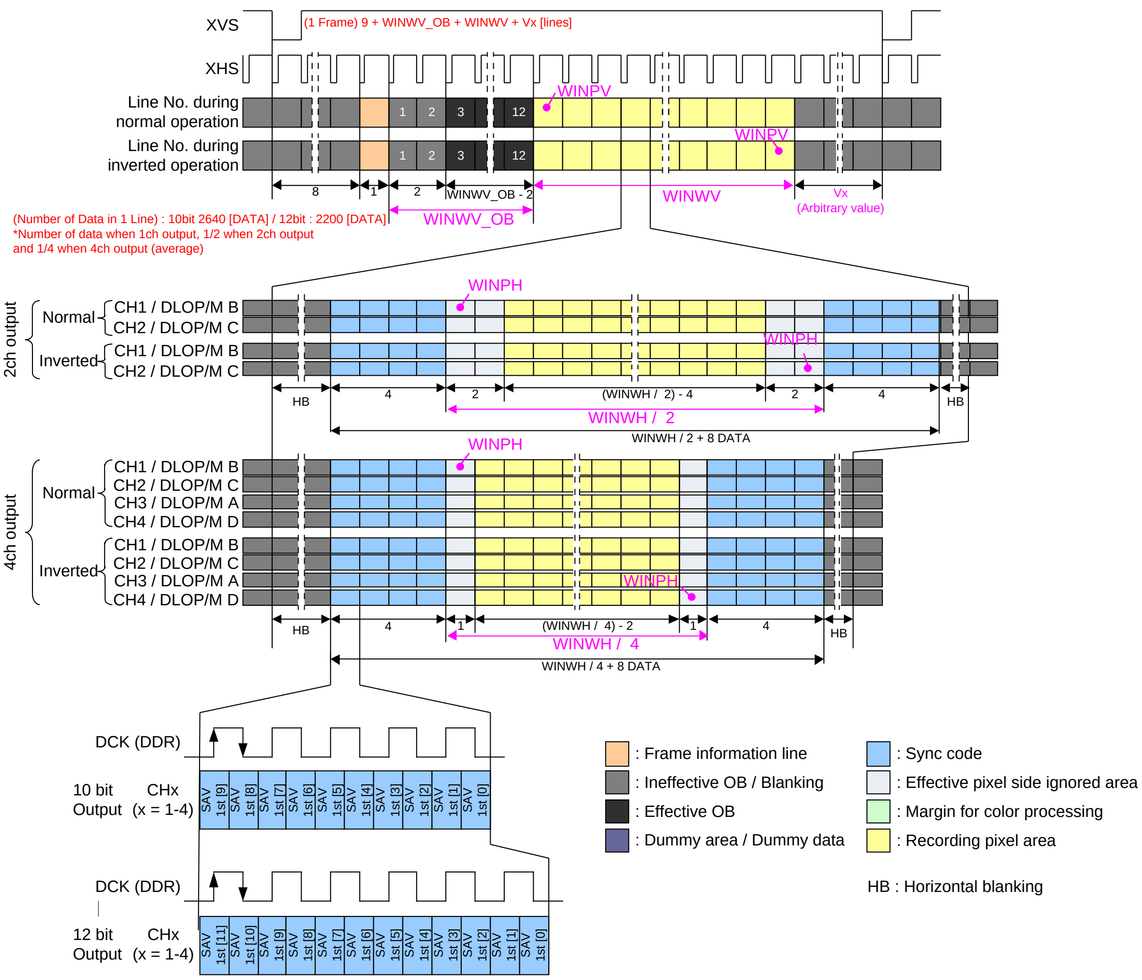
Example of Window cropping Mode Setting

Image size	INCK [MHz]	Output Resolution [bit]	Frame rate [frame/s]	Number of recording pixels		Register setting [DEC] (HEX)						
				Horizontal	Vertical	FRSEL	HMAX	VMAX	WINPH	WINPV	WINWH	WINWV
VGA	37.125 74.25	10/12	64.9	640	480	2	4400d (0898h)	520d (208h)	640d (280h)	300d (12Ch)	656d (290h)	496d (1F0h)
		10/12	129.8			1	2200d (898h)					
CIF	37.125 74.25	10/12	102.9	352	288	2	4400d (0898h)	328d (148h)	784d (310h)	396d (18Ch)	368d (170h)	304d (130h)
		10/12	205.8			1	2200d (898h)					

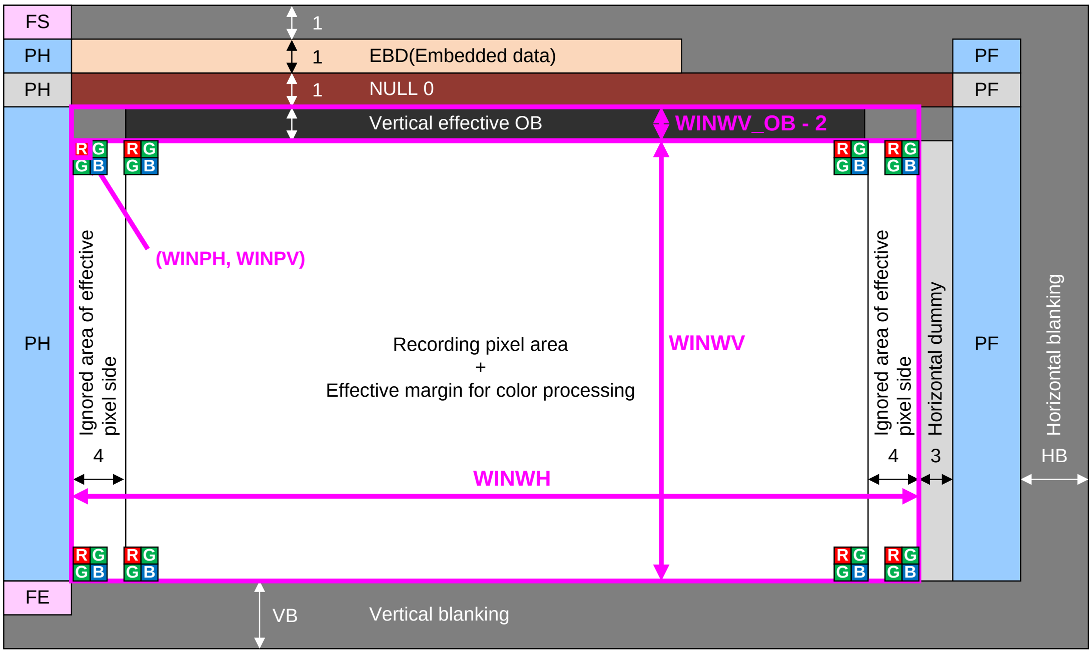
* These settings are when the ignored OB line is 2 lines and effective OB line is 10 lines.
* When the CSI-2 output, set the value that is set to register WINWV_OB to register Y_OUT_SIZE.



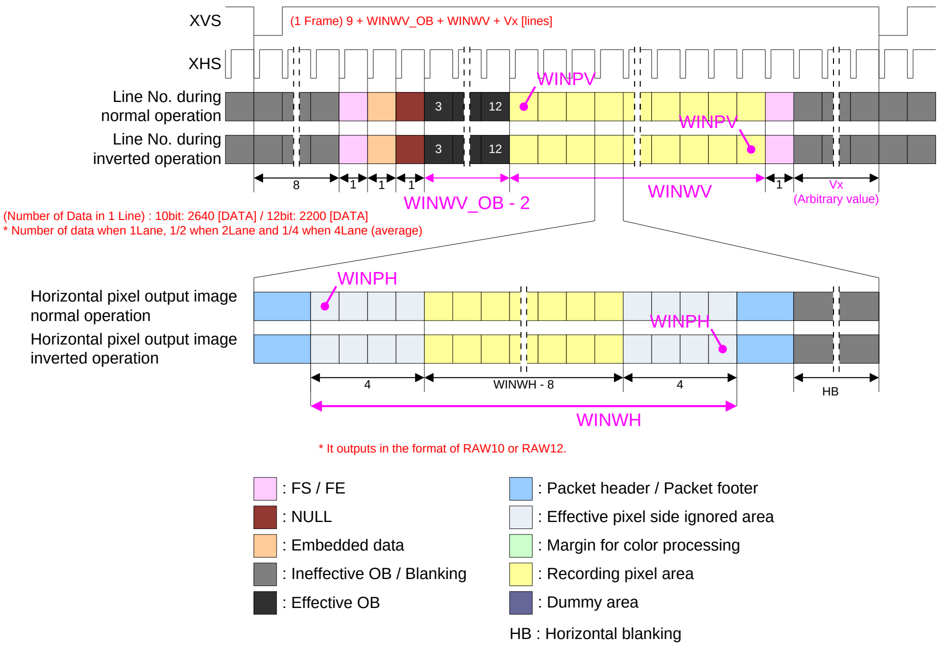
Pixel Array Image Drawing in Window Cropping mode (Serial LVDS output)



Drive Timing Chart for Window Cropping mode (Serial LVDS output)



Pixel Array Image Drawing in Window Cropping mode (CSI-2 serial output)



Drive Timing Chart for Window Cropping mode (CSI-2 serial output)

HD720p mode

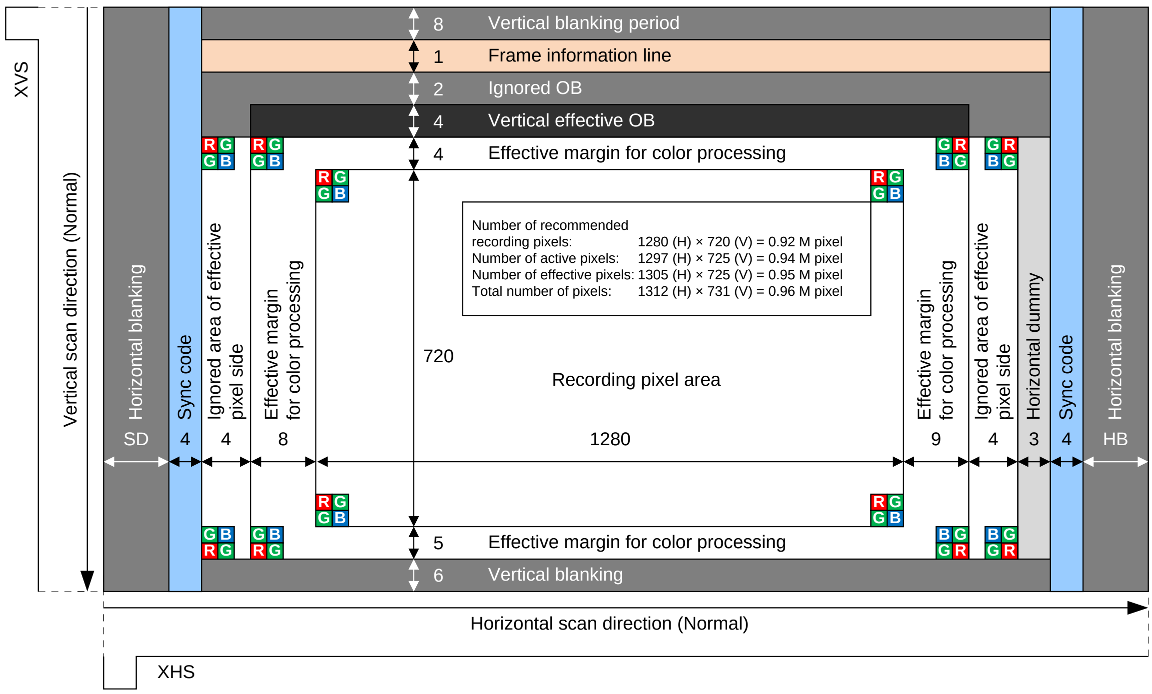
List of Setting Register for LVDS serial output

Address 4-wire	Address I²C	bit	Register Name	Initial Value	LVDS serial 2 ch	LVDS serial 4 ch	Remarks
Chip ID: 02h							
05h	3005h	[0]	ADBIT	1h	0h / 1h		0: 10 bit, 1: 12 bit
07h	3007h	[0]	VREVERSE	0h	0h / 1h		0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h		0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	1h		HD 720p
09h	3009h	[1:0]	FRSEL	1h	2h		30 [frame/s]
					1h		60 [frame/s]
		[4]	FDG_SEL	0h	0h / 1h		0: LCG mode, 1: HCG mode
12h	3012h	[7:0]	—	F0h	64h		Initial setting
13h	3013h	[7:0]	—	00h	00h		Initial setting
18h	3018h	[7:0]	VMAX	465h	2EEh		25 /30 / 50 / 60 [frame/s]
19h	3019h	[7:0]					
1Ah	301Ah	[1:0]					
1Ch	301Ch	[7:0]	HMAX	0898h	19C8h / 1EF0h		19C8h: 30[frame/s] / 1EF0h: 25[frame/s]
1Dh	301Dh	[7:0]			0CE4h / 0F78h		0CE4h: 60[frame/s] / 0F78h: 50[frame/s]
46h	3046h	[1:0]	ODBIT	1h	0h / 1h		0: 10 bit, 1: 12 bit
		[7:4]	OPORTSEL	Eh	Dh	Eh	I/F selection
5Ch	305Ch	[7:0]	INCKSEL1	0Ch	10h / 20h		Set according to INCK 74.25/37.125 MHz
5Dh	305Dh	[7:0]	INCKSEL2	00h	00h / 00h		
5Eh	305Eh	[7:0]	INCKSEL3	10h	10h / 20h		
5Fh	305Fh	[7:0]	INCKSEL4	01h	01h / 01h		
Chip ID = 03h							
29h	3129h	[7:0]	ADBIT1	1Dh	1Dh / 00h		10 bit: 1Dh 12 bit: 00h
5Eh	315Eh	[7:0]	INCKSEL5	1Bh	1Bh / 1Ah		INCK: 74.25 / 37.125 MHz
64h	3164h	[7:0]	INCKSEL6	1Bh	1Bh / 1Ah		INCK: 74.25 / 37.125 MHz
7Ch	317Ch	[7:0]	ADBIT2	12h	12h / 00h		10 bit: 12h 12 bit: 00h
ECh	31ECh	[7:0]	ADBIT3	37h	37h / 0Eh		10 bit: 37h 12 bit: 0Eh
Chip ID = 04h							
00h ~ FFh	3200h ~ 32FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.				
Chip ID = 05h							
00h ~ FFh	3300h ~ 33FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.				
Chip ID = 06h							
00h ~ 7Fh	3400h ~ 347Fh	[7:0] ~ [7:0]	Changing the value is not necessary.				
80h	3480h	[7:0]	INCKSEL7	92h	92h / 49h		INCK: 74.25 / 37.125 MHz
81h ~ FFh	3481h ~ 34FFh	[7:0] ~ [7:0]	Changing the value is not necessary.				

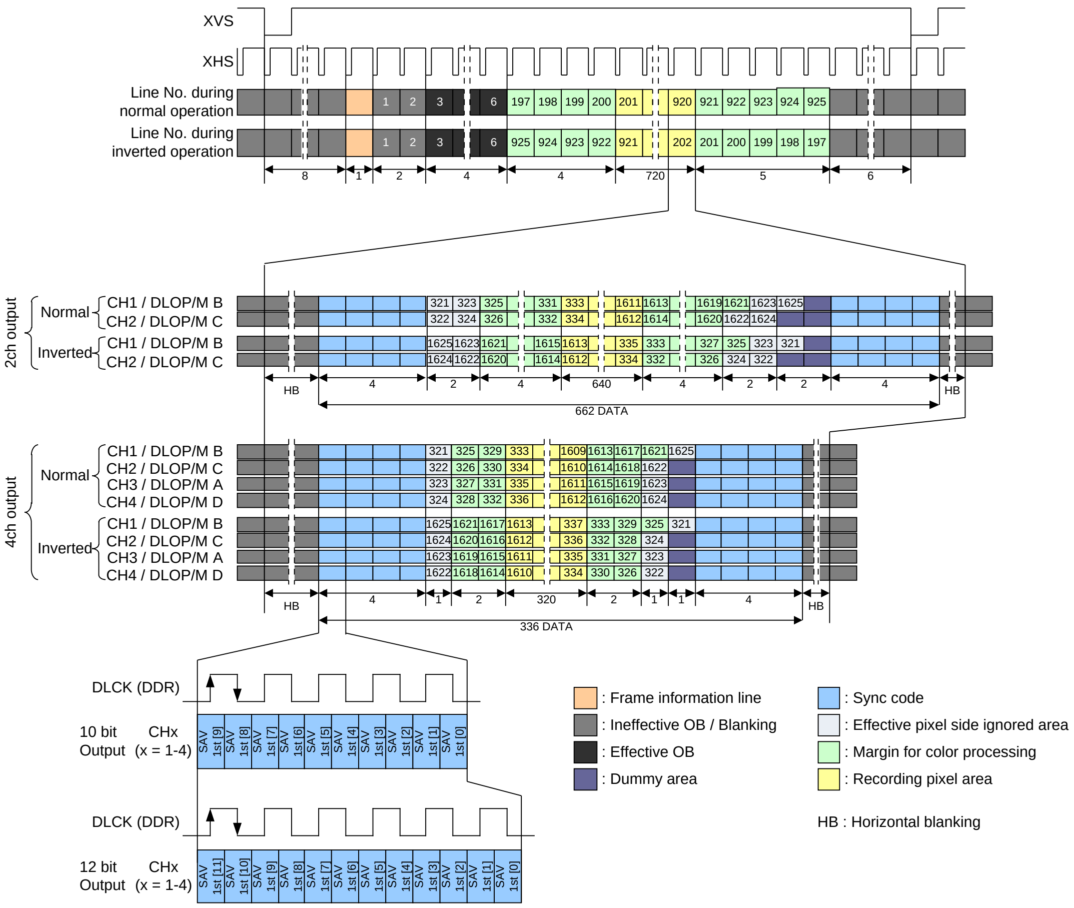
List of Setting Register for CSI-2 serial output

Address		bit	Register Name	Initial Value	CSI-2 serial				Remarks
					2 lane		4 lane		
4-wire	I²C				30 [frame /s]	60 [frame /s]	30 [frame /s]	60 [frame /s]	
Chip ID: 02h									
05h	3005h	[0]	ADBIT	1h	0h / 1h				0: 10 bit, 1: 12 bit
07h	3007h	[0]	VREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[1]	HREVERSE	0h	0h / 1h				0: Normal, 1: Inverted
		[6:4]	WINMODE	0h	1h				HD 720p
09h	3009h	[1:0]	FRSEL	1h	2h	1h	2h	1h	
		[4]	FDG_SEL	0h	0h / 1h				0: LCG mode, 1: HCG mode
12h	3012h	[7:0]	—	F0h	64h				Initial setting
13h	3013h	[7:0]	—	00h	00h				Initial setting
18h	3018h	[7:0]	VMAX	465h	2EEh				25 /30 / 50 / 60 [frame/s]
19h	3019h	[7:0]							
1Ah	301Ah	[1:0]							
1Ch	301Ch	[7:0]	HMAX	0898h	19C8h / 1EF0h	0CE4h / 0F78h	19C8h / 1EF0h	0CE4h / 0F78h	30 / 60[frame / s] / 25 / 50 [frame / s]
1Dh	301Dh	[7:0]							
44h	3044h	[1:0]	ODBIT	1h	1h				In CSI-2, fixed to “1h”.
		[7:4]	OPORTSEL	Eh	0h				In CSI-2, fixed to “0h”.
5Ch	305Ch	[7:0]	INCKSEL1	0Ch	10h / 20h				Set according to INCK 74.25/37.125 MHz
5Dh	305Dh	[7:0]	INCKSEL2	00h	00h / 00h				
5Eh	305Eh	[7:0]	INCKSEL3	10h	10h / 20h				
5Fh	305Fh	[7:0]	INCKSEL4	01h	01h / 01h				
Chip ID = 03h									
29h	3129h	[7:0]	ADBIT1	1Dh	1Dh / 00h				10 bit: 1Dh 12 bit: 00h
5Eh	315Eh	[7:0]	INCKSEL5	1Bh	1Bh / 1Ah				Set according to INCK 74.25 / 37.125 MHz
64h	3164h	[7:0]	INCKSEL6	1Bh	1Bh / 1Ah				Set according to INCK 74.25 / 37.125 MHz
7Ch	317Ch	[7:0]	ADBIT2	12h	12h / 00h				10 bit: 12h 12 bit: 00h
ECh	31ECh	[7:0]	ADBIT3	37h	37h / 0Eh				10 bit: 37h 12 bit: 0Eh
Chip ID = 04h									
00h ~ FFh	3200h ~ 32FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.						
Chip ID = 05h									
00h ~ FFh	3300h ~ 33FFh	[7:0] ~ [7:0]	Set register value that described on item “Register map”.						

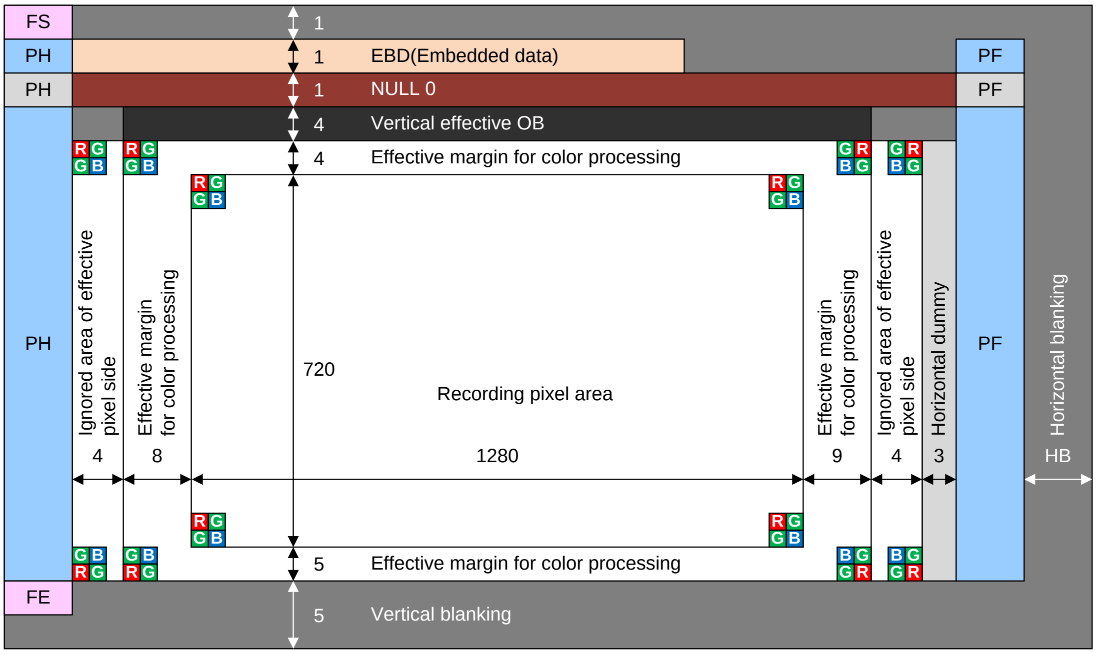
Address 4-wire	Address I²C	bit	Register Name	Initial Value	CSI-2 serial 2 lane 30 [frame /s]	CSI-2 serial 2 lane 60 [frame /s]	CSI-2 serial 4 lane 30 [frame /s]	CSI-2 serial 4 lane 60 [frame /s]	Remarks
Chip ID = 06h									
				Data rate	297	594	148.5	297	[Mbps / Lane]
05h	3405h	[5:4]	REPETITION	2h	1h	0h	2h	1h	
07h	3407h	[1:0]	PHYSICAL_ LANE_NUM	3h	1h		3h		
14h	3414h	[5:0]	OPB_SIZE_V	Ah	4h				
18h	3418h	[7:0]	Y_OUT_SIZE	0449h	2D9h				
19h	3419h	[4:0]							
41h	3441h	[7:0]	CSI_DT_FMT	0C0Ch	0A0Ah / 0C0Ch				0A0Ah: RAW10 0C0Ch: RAW12
42h	3442h	[7:0]							
43h	3443h	[1:0]	CSI_LANE_ MODE	3h	1h		3h		
44h	3444h	[7:0]	EXTCK_FREQ	4A40h	37.125 MHz : 2520h 74.25 MHz : 4A40h				Set according to INCK
45h	3445h	[7:0]							
46h	3446h	[7:0]	TCLKPOST	047h	04Fh	067h	047h	04Fh	Global timing
47h	3447h	[0]							
48h	3448h	[7:0]	THSZERO	01Fh	02Fh	057h	017h	02Fh	Global timing
49h	3449h	[0]							
4Ah	344Ah	[7:0]	THSPREPARE	017h	017h	02Fh	00Fh	017h	Global timing
4Bh	344Bh	[0]							
4Ch	344Ch	[7:0]	TCLKTRAIL	00Fh	017h	027h	00Fh	017h	Global timing
4Dh	344Dh	[0]							
4Eh	344Eh	[7:0]	THSTRAIL	017h	017h	02Fh	00Fh	017h	Global timing
4Fh	344Fh	[0]							
50h	3450h	[7:0]	TCLKZERO	047h	057h	0BFh	02Bh	057h	Global timing
51h	3451h	[0]							
52h	3452h	[7:0]	TCLKPREPARE	00Fh	017h	02Fh	00Bh	017h	Global timing
53h	3453h	[0]							
54h	3454h	[7:0]	TLPX	00Fh	017h	027h	00Fh	017h	Global timing
55h	3455h	[0]							
72h	3472h	[7:0]	X_OUT_SIZE	079Ch	51Ch				
73h	3473h	[4:0]							
80h	3480h	[7:0]	INCKSEL7	92h	37.125 MHz : 49h 74.25 MHz : 92h				Set according to INCK



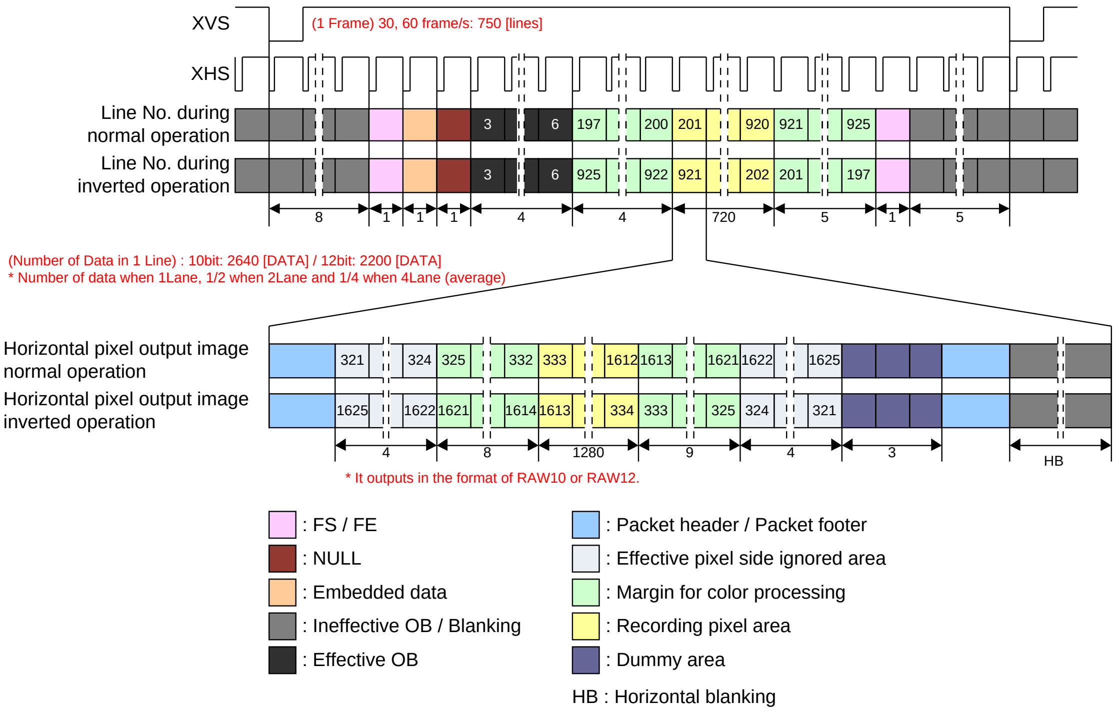
Pixel Array Image Drawing in HD720p mode (Serial LVDS output)



Drive Timing Chart for HD720p mode (Serial LVDS output)



Pixel Array Image Drawing in HD720p mode (CSI-2 serial output)



Drive Timing Chart for HD720p mode (CSI-2 serial output)

Description of Various Function

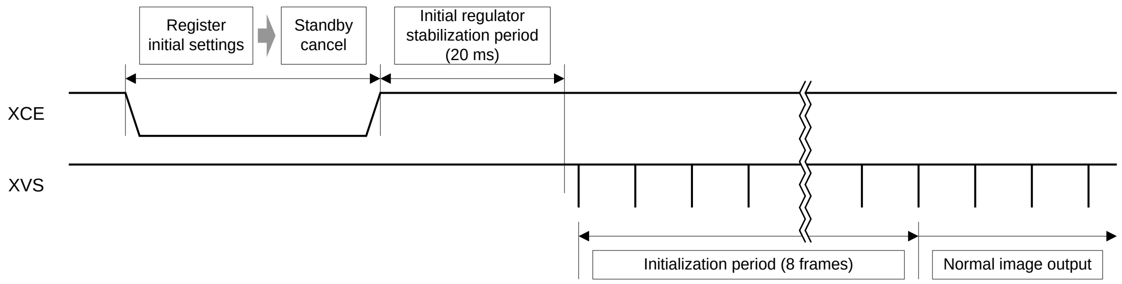
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register name	Register details				Initial value	Setting value	Status	Remarks
	Register	Chip ID	Address ( ) : I^2C	bit				
STANDBY	—	02h	00h (3000h)	[0]	1	1	Standby	Register communication is executed in standby mode.
						0	Operating	

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (20 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)

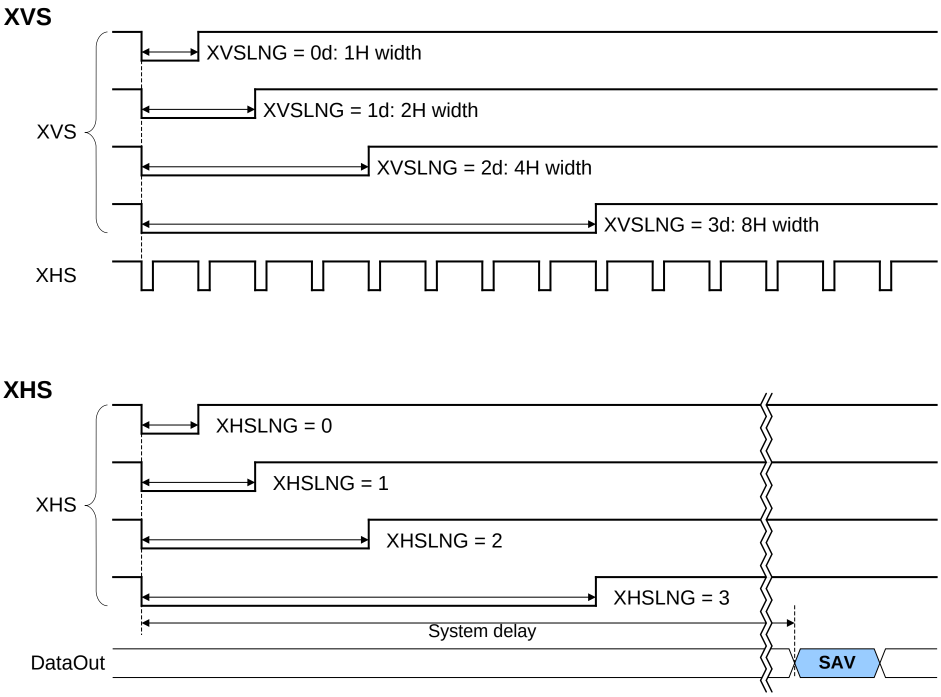
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Operating mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [17:0] register and the clock number in horizontal direction by the HMAX [13:0] register. See the description of Operation Mode for details of the section of “Operating Modes”.

List of Slave and Master Mode Setting

Pin name	Pin processing	Operating mode	Remarks
XMASTER pin	Fixed to Low	Master mode	High: OV_{DD} Low: GND
	Fixed to High	Slave mode	

List of Register in Master Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ) : I²C	bit			
XMSTA	—	02h (3002h)	[0]	1	1: Master operation ready 0: Master operation start	The master operation starts by setting 0.
VMAX [17:0]	VMAX [7:0]	18h (3018h)	[7:0]	00465h	See the item of each drive mode.	Line number per frame designated
	VMAX [15:8]	19h (3019h)	[7:0]			
	VMAX [17:16]	1Ah (301Ah)	[1:0]			
HMAX [13:0]	HMAX [7:0]	1Ch (301Ch)	[7:0]	0898h	See the item of each drive mode.	Clock number per line designated
	HMAX [15:8]	1Dh (301Dh)	[7:0]			
XVSLNG [1:0]	—	48h (3048h)	[5:4]	0h	0: 1H, 1: 2H, 2: 4H, 3: 8H	XVS low level pulse width designated
XHSLNG [1:0]	—	49h (3049h)	[5:4]	0h	0: Min. to 3: Max. See the next	XHS low level pulse width designated
XVSOUTSEL [1:0]	—	4Bh (304Bh)	[1:0]	0h	0: Fixed to High 2: VSYNC output Others: Setting prohibited	
XHSOUTSEL [1:0]	—		[3:2]	0h	0: Fixed to High 2: HSYNC output Others: Setting prohibited	



XVS/XHS output waveform in sensor master mode

List of XHSLNG Register

	LVDS serial output					
DCK	594 [Mbps / ch]	297 [Mbps / ch]	148.5 [Mbps / ch]	445.5 [Mbps / ch]	222.75 [Mbps / ch]	111.375 [Mbps / ch]
XHSLNG = 0	64 bit	32 bit	16 bit	48 bit	24 bit	12 bit
XHSLNG = 1	128 bit	64 bit	32 bit	96 bit	48 bit	24 bit
XHSLNG = 2	256 bit	128 bit	64 bit	192 bit	96 bit	48 bit
XHSLNG = 3	512 bit	256 bit	128 bit	384 bit	192 bit	96 bit

The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output just after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with a undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

Gain Adjustment Function

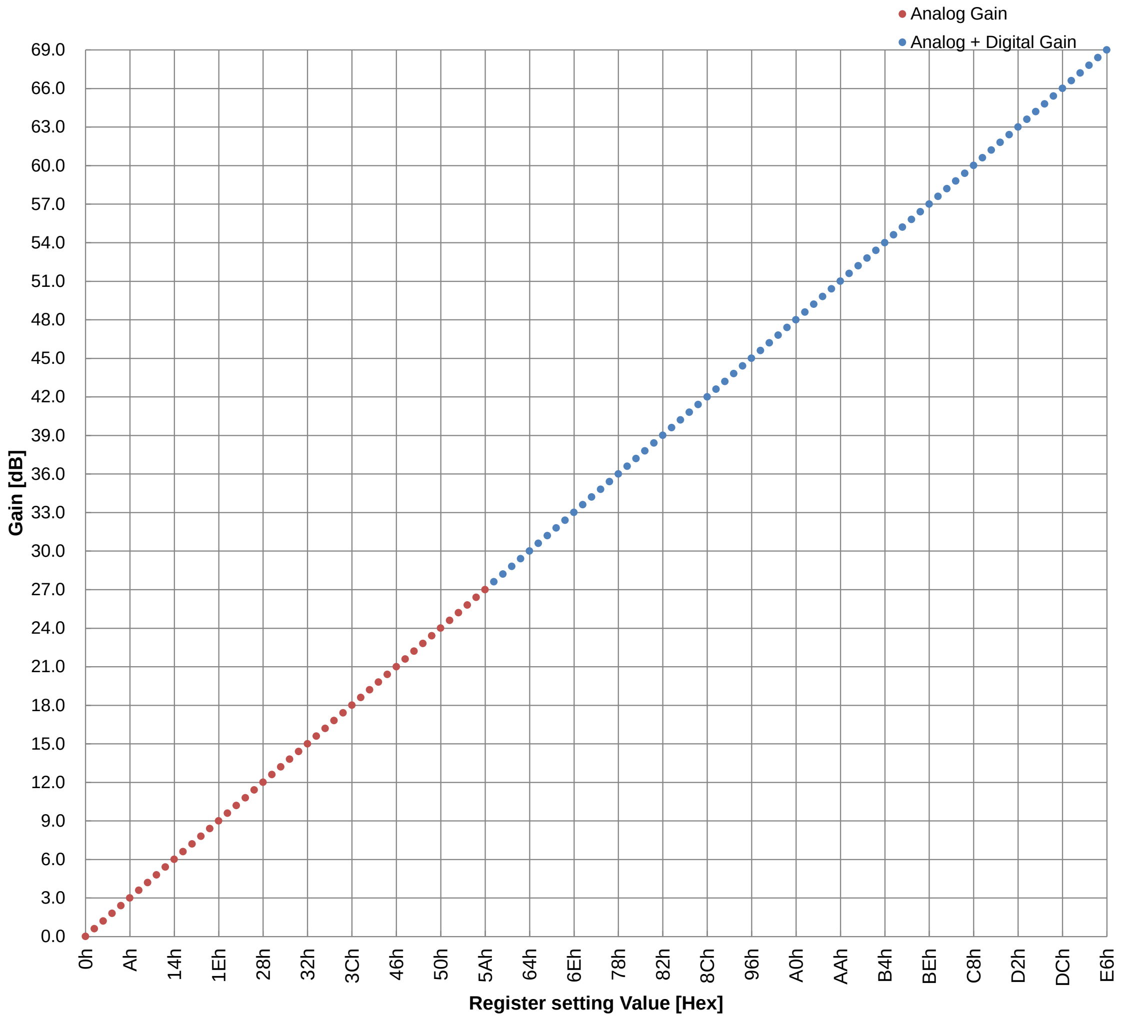
The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to 69 dB by the GAIN [7:0] register setting. The same setting is applied in all colors.

The value which is 10/3 times the gain is set to register. (0.3 dB step)

Example)

When set to 6 dB: 6 × 10/3 = 20d; GAIN [7:0] = 14h

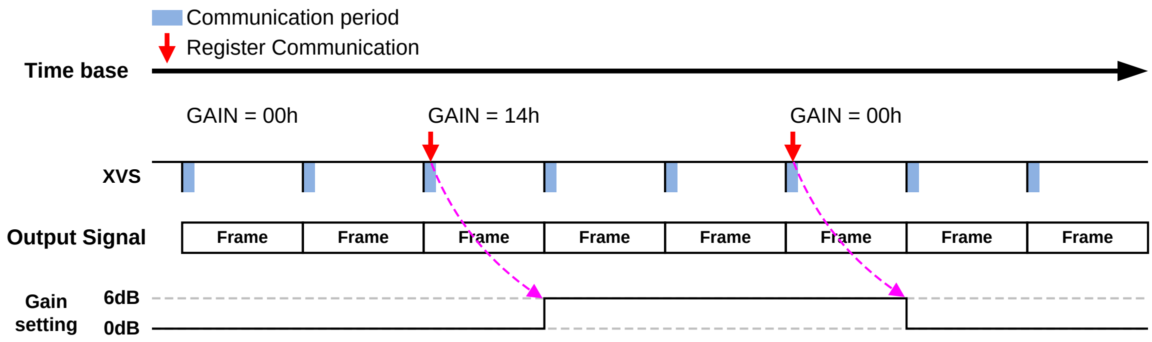
When set to 12.6 dB: 12.6 × 10/3 = 42d; GAIN [7:0] = 2Ah



List of PGC Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ) : I²C	bit		Setting range	
GAIN [7:0]	GAIN [7:0]	14h (3014h)	[7:0]	00h	00h-E6h (0d-230d)	Setting value: Gain [dB] × 10/3 (0.3 dB step)

The gain setting is reflected at the next frame that the communication is performed as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [8:0] register. When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB.

Use with values shown below is recommended.
10-bit output: 03Ch (60d)
12-bit output: 0F0h (240d)

List of Black Level Adjustment Register

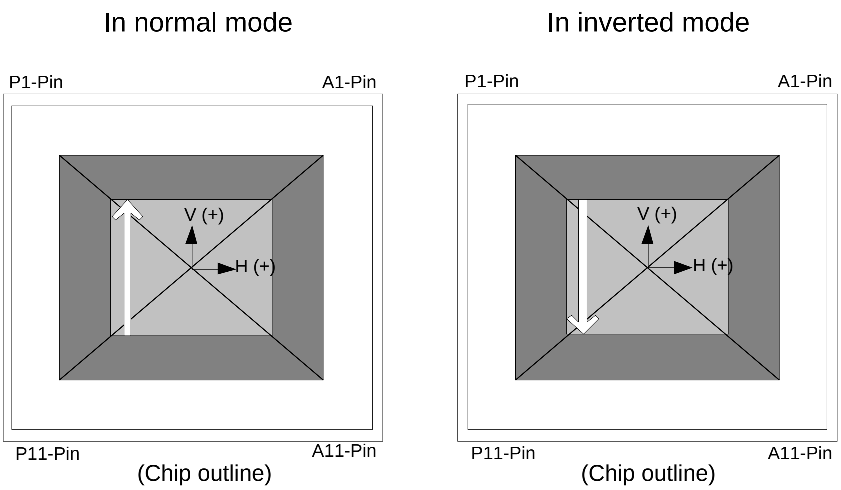
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I²C	bit		
BLKLEVEL [8:0]	BLKLEVEL [7:0]	0Ah (300Ah)	[7:0]	0F0h	000h to 1FFh
	BLKLEVEL [8]	0Bh (300Bh)	[0]		

Normal Operation and Inverted Operation

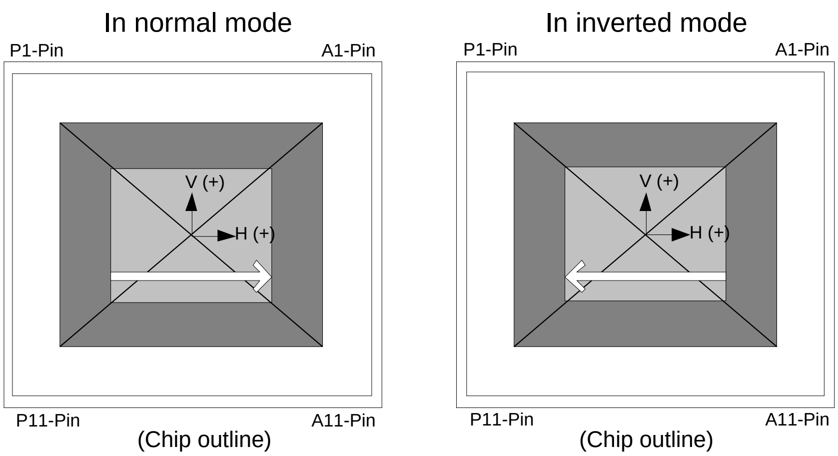
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and in horizontal direction can be switched by the HREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
VREVERSE	—	07h (3007h)	[0]	0h	0: Normal (Initial value) 1: Vertical Inverted
HREVERSE	—		[1]	0h	0: Normal (Initial value) 1: Horizontal Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - (SHS1 + 1) × (1H period)

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
*2 See "Operating Modes" for the 1H period.

In this section, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

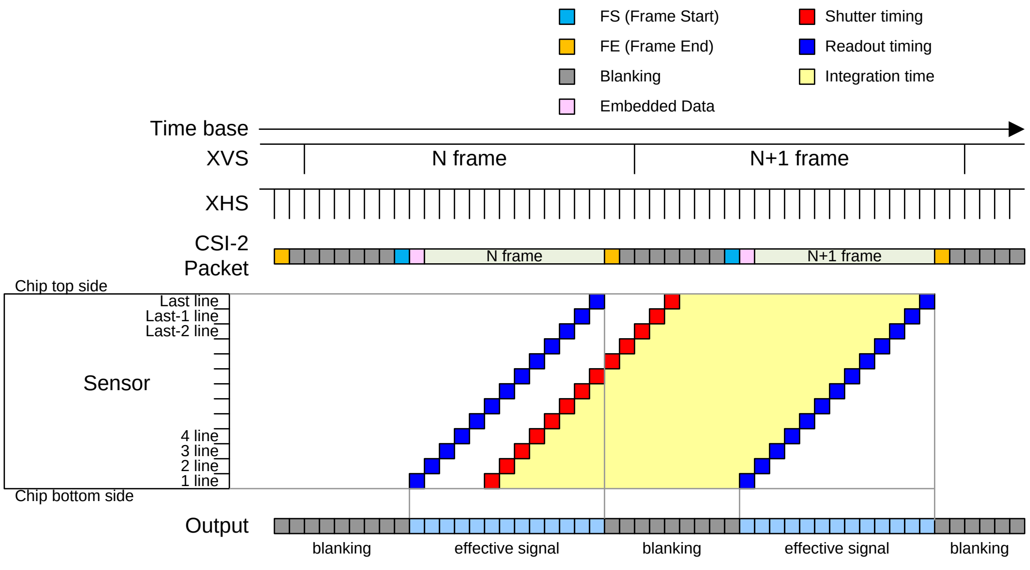


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS1 [17:0] register. Set SHS1 [17:0] to a value between 1 and (Number of lines per frame - 1). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register. The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 1H Units

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
SHS1 [17:0]	SHS1 [7:0]	20h (3020h)	[7:0]	00000h	Sets the shutter sweep time. 1 to (Number of lines per frame - 2) * 0 and number of lines per frame -1 setting is prohibited
	SHS1 [15:8]	21h (3021h)	[7:0]		
	SHS1 [17:16]	22h (3022h)	[1:0]		
VMAX [17:0]	VMAX [7:0]	18h (3018h)	[7:0]	00465h	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	VMAX [15:8]	19h (3019h)	[7:0]		
	VMAX [17:16]	1Ah (301Ah)	[1:0]		

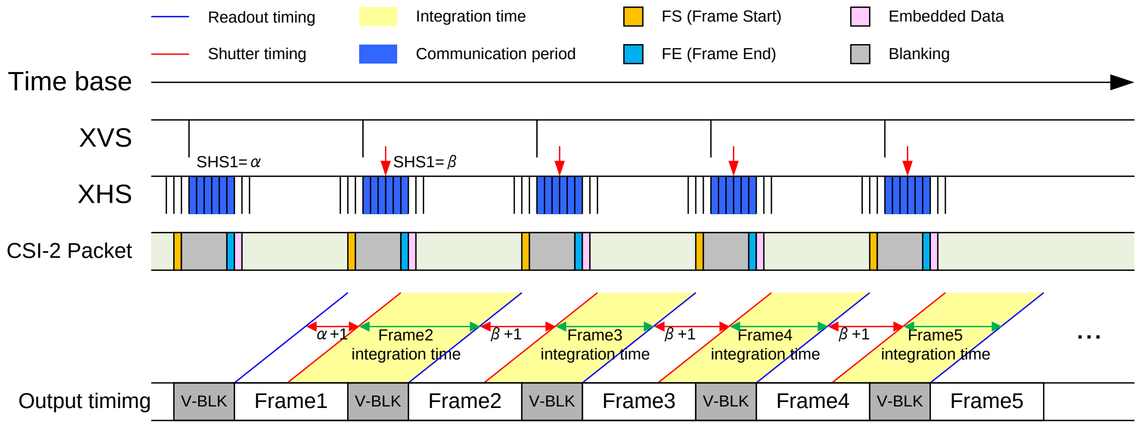


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [17:0] value compared to normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

Although the maximum value of long exposure operation changes in each modes, the maximum of long time exposure is approximately 1 s.
When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

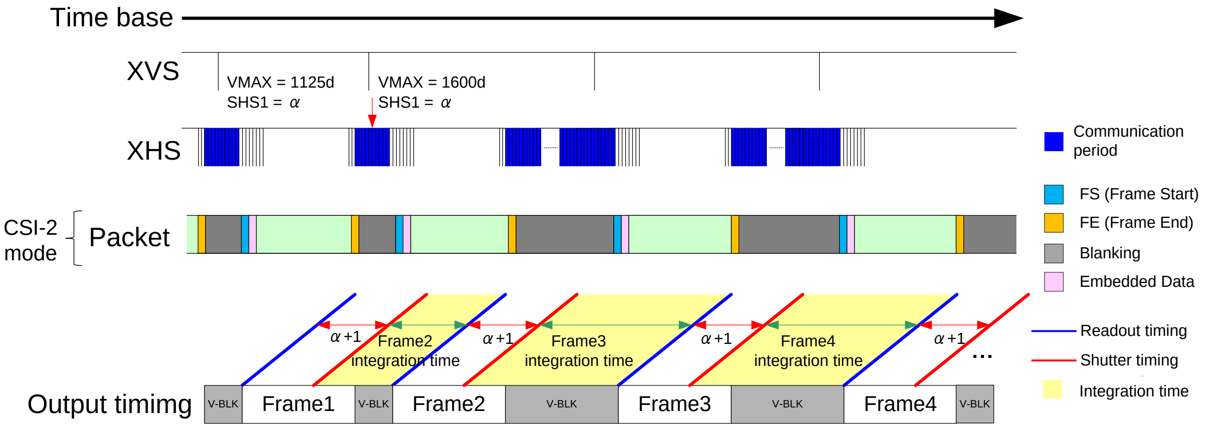


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Settings (In Full HD 1080p)

Operation	Sensor setting (register)		Integration time
	VMAX*	SHS1**	
Normal frame rate	1125	1123	1H
		⋮	⋮
		N	(1125 - (N + 1)) H
		⋮	⋮
		1	1123H

* In sensor master mode. In slave mode, the interval is the same as XVS input.
** The SHS1 setting value (N) is set between “1” and “the VMAX value (M) – 2”.

Signal Output

Output Pin Settings

The output formats of this sensor support the following modes.

Low voltage LVDS serial (2 ch / 4 ch switching) DDR output
CSI-2 serial (2 Lane / 4 Lane, RAW10 / RAW12) output

The switching for serial interface is made by the OMODE pin. Establish the OMODE pin status before canceling the system reset. (Do not switch this pin status during operation.) Each mode is set using the register OPORTSEL. The table below shows the output format settings.

List of Interface Switching

Pin name	Pin	Interface	Remarks
OMODE pin	Fixed to Low	CSI-2 serial	High: OVDD Low: GND
	Fixed to High	Low voltage LVDS serial	

List of Output Interface Setting Register

Register name	Register details (Chip ID = 02h)		Initial value	Setting value	Description
	Address ( ) : I²C	bit			
OPORTSEL [3:0]	46h (3046h)	[7:4]	Eh	Dh	Low voltage LVDS serial 2 ch DDR
				Eh	Low voltage LVDS serial 4 ch DDR
				N/A	CSI-2 serial 2Lane
				N/A	CSI-2 serial 4Lane

* In CSI-2 output, set registers that described in section “CSI-2 output setting”.

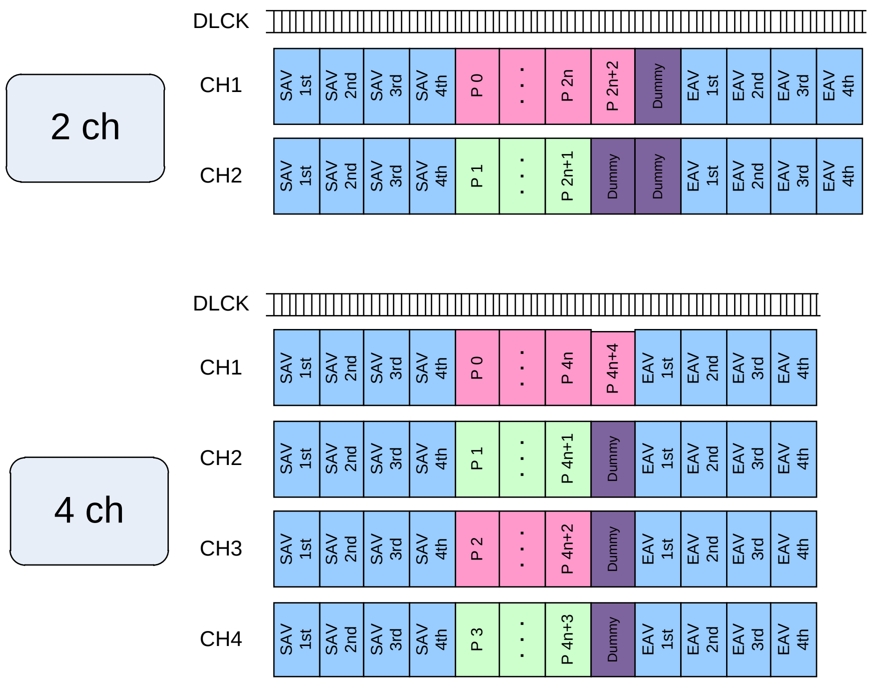
Each output pin is shown in the table below when setting low-voltage LVDS serial 2 ch / 4 ch output.

Output Pins for Low LVDS Serial

DOP/DOM	Low voltage LVDS serial DDR output	
	2 ch	4 ch
DLOMD	Hi-Z	Ch4 / M
DLOPD	Hi-Z	Ch4 / P
DLOMC	Ch2 / M	Ch2 / M
DLOPC	Ch2 / P	Ch2 / P
DLOMB	Ch1 / M	Ch1 / M
DLOPB	Ch1 / P	Ch1 / P
DLOMA	Hi-Z	Ch3 / M
DLOPA	Hi-Z	Ch3 / P

Low-voltage LVDS serial 2 ch / 4 ch output format is shown in the figure below.
When setting 2 ch, after four data of SAV is output in the order of CH1 and CH2 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 and CH2 respectively.
When setting 4 ch, after four data of SAV is output in the order of CH1, CH2, CH3 and CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1, CH2, CH3 and CH4 respectively.
Data is sent MSB first.

For details, see drive timing in each mode in the section of "Operation Mode".



Output Format of Low voltage LVDS Serial 2 ch / 4 ch
(Full HD 1080p)

CSI-2 output

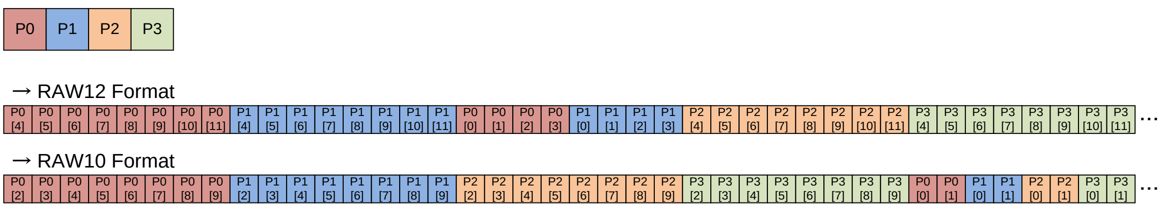
The output formats of this sensor support the following modes.

CSI-2 serial 2 Lane / 4 Lane, RAW10 / RAW12

The 2 Lane / 4 Lane serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 2 Lane / 4 Lane. The image data is output from the CSI-2 output pin. The DMO1P/DMO1N are called the Lane1 data signal, the DMO2P/DMO2N are called the Lane2 data signal, the DMO3P/DMO3N are called the Lane3 data signal, the DMO4P/DMO4N are called the Lane4 data signal. In addition, the clock signals are output from DMCKP/DMCKN of the CSI-2 pins.
In 2 Lane mode, data is output from Lane1 and Lane2. In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4. The bit rate maximum value is 891 Mbps / Lane.
The select of RAW10 / RAW12 is set by the register: CSI_DT_FMT [15:0] The number of output lanes is set by the register: CSI_LANE_MODE [1:0] and the number of lanes physically connected is set by PHYSICAL_LANE_NUM [1:0]. Unused lanes (when setting 2 lanes; DMO3P / DMO3N, DMO4P / DMO4N) are set to Hi-Z output by the setting. When the number of lanes more than CSI_LANE_MODE is set by PHYSICAL_LANE_NUM, unused lanes output signals conformed to MIPI standard.

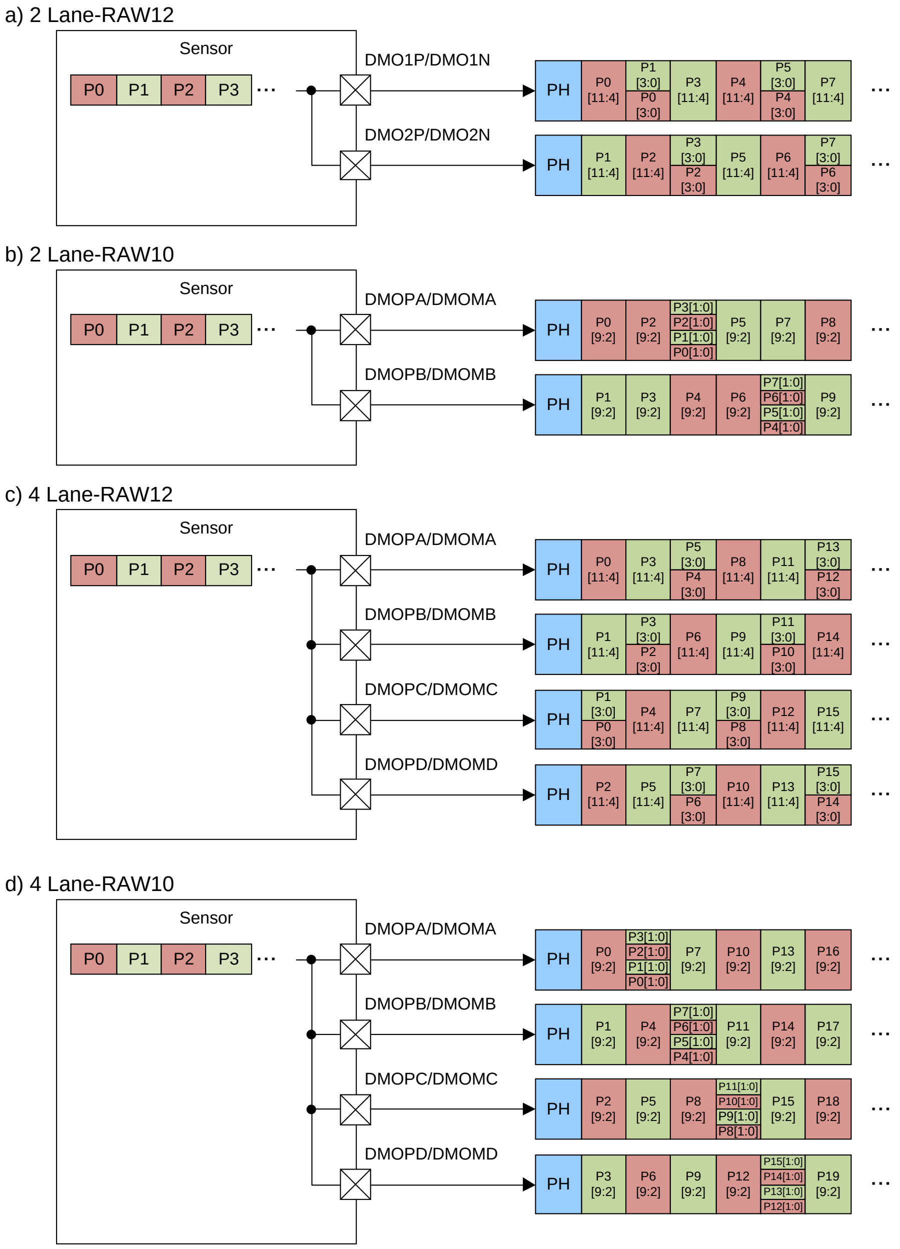
Register name	Register details (Chip ID = 06h)		Initial value	Setting value	Description
	Address ( ) : I^2C	bit			
CSI_DT_FMT [15:0]	41h (3441h)	[7:0]	0C0Ch	0A0Ah	RAW10
	42h (3442h)	[7:0]		0C0Ch	RAW12
PHYSICAL_LANE_NUM [1:0]	07h (3407h)	[1:0]	3h	0h	Setting prohibited
				1h	2Lane
				2h	Setting prohibited
				3h	4Lane
CSI_LANE_MODE [1:0]	43h (3443h)	[1:0]	3h	0h	Setting prohibited
				1h	2Lane
				2h	Setting prohibited
				3h	4Lane

The formats of RAW12 and RAW10 are shown below.



The Example of Format of RAW12 / RAW10

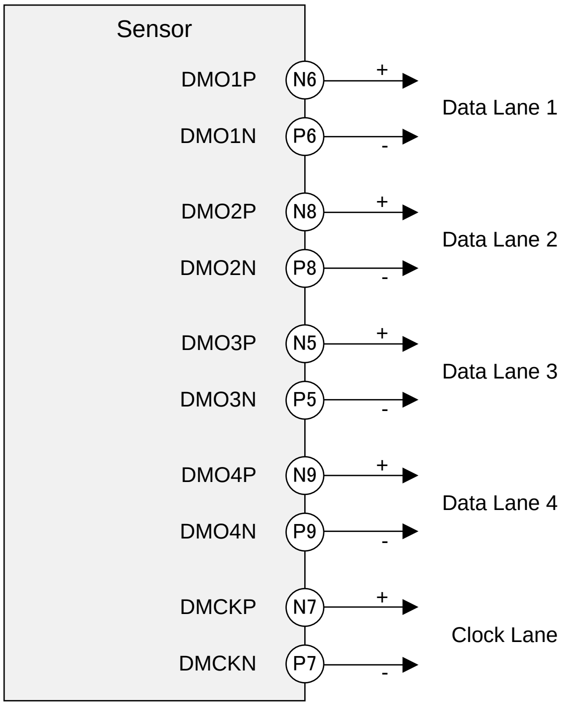
The each formal of 2 Lane and 4 Lane are shown below.



2 Lane / 4 Lane Output Format

MIPI Transmitter

Output pins (DMO1P, DMO1N, DMO2P, DMO2N, DMO3P, DMO3N, DMO4P, DMO4N, DMCKP, DMCKN) are described in this section.

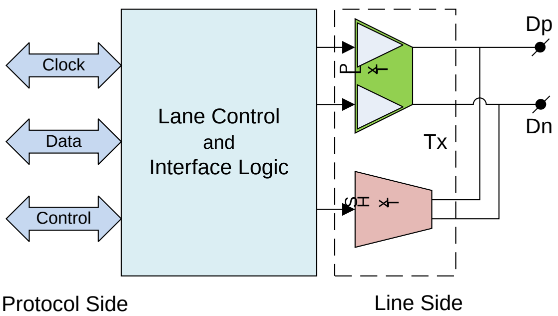


Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard

・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01.00
・MIPI Alliance Specification for D-PHY Version 1.00.00

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 891 Mbps / Lane.



Universal Lane Module Functions

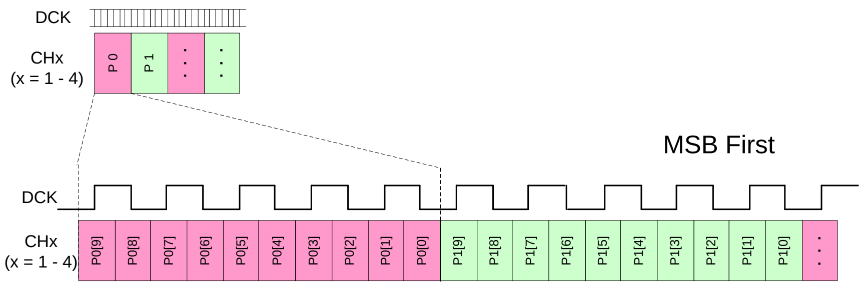
Output Pin Bit Width Selection

The output pin width can be selected from 10-bit or 12-bit output using the register ODBIT.
When low-voltage LVDS serial output, continuous data is output MSB first by 10-bit and 12-bit output setting respectively. 10-bits sync code are output when ODBIT = 0 (10-bit output), and 12-bit sync codes are output when ODBIT = 1 (12-bit output).

Output Pin Bit Width Selection Setting Register

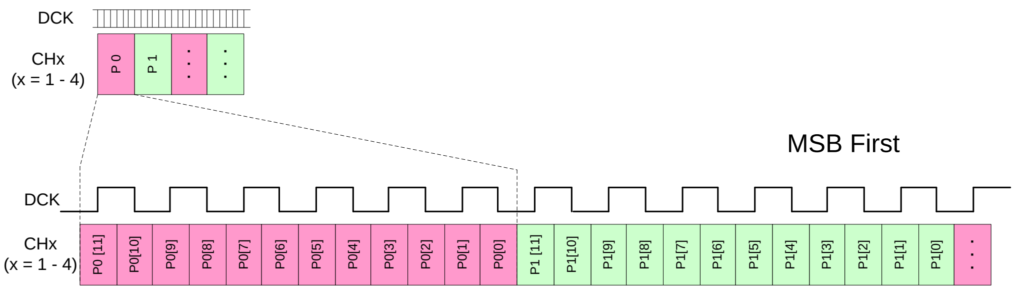
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
ODBIT	—	46h (3046h)	[0]	1h	0: 10 bit 1: 12 bit

ODBIT = 0 (Low voltage LVDS serial 10 bit output)



Example of Data format in low-voltage LVDS serial 10-bit output

ODBIT = 1 (Low voltage LVDS serial 12 bit output)



Example of Data format in low-voltage LVDS serial 12-bit output

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bits or 12 bits by the register ADBIT. See the section of “Operating Modes” for the correspondence with each mode.

List of Bit Width Selection

Register name	Register details *1: Chip ID = 02h *2: Chip ID = 03h			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
ADBIT	—	05h *1 (3005h)	[0]	1h	0: 10 bit 1: 12 bit
ADBIT1[7:0]	—	29h *2 (3129h)	[7:0]	1Dh	10 bit: 1Dh 12 bit: 00h
ADBIT2[7:0]	—	7Ch *2 (317Ch)	[7:0]	12h	10 bit: 12h 12 bit: 00h
ADBIT3[7:0]	—	ECh *2 (31ECh)	[7:0]	37h	10 bit: 37h 12 bit: 0Eh

Output Rate Setting

The sensor output rate is determined uniformly by the sensor operating mode and the output format. See the section of “Operating Modes” for the relationship between each setting and the frame rate, data rate and data bit rate. The registers related to mode setting are shown in the table below.

Related Registers for Setting Operation Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
WINMODE [2:0]	—	07h (3007h)	[6:4]	0h	0: Full HD 1080p 1: 720 p 4: Window cropping from Full HD 1080p
FRSEL [1:0]	—	09h (3009h)	[1:0]	1h	1: 60 frame / s 2: 30 frame / s 0,3: Setting prohibited

Output Signal Range

In sub LVDS output mode, the sensor output has 10 bit or 12 bit gray scale according to the setting. The output is not performed at full range and the range is the values shown in the table below
See the item of “Sync Codes” in the section of “Operating Modes” for the sync codes.

Output Gradation and Output Range (Low voltage LVDS Output)

Output gradation	Output value	
	Min.	Max.
10 bit	001h	3FEh
12 bit	001h	FFEh

In CSI-2 output mode, the sensor output has either a 10 bit or 12 bit gradation, but output is not performed over the full range, and the maximum output value is the 3FFh value (10 bit output) and the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh
12 bit	000h	FFFh

INCK Setting

The available operation mode varies according to INCK frequency. Input either 37.125 MHz or 74.25 MHz for INCK frequency. The INCK setting register and the list of INCK setting are shown in the table below.

INCK Setting Register

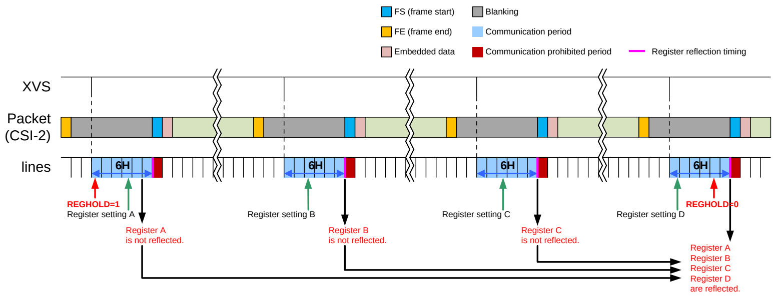
Register name	Register details *1: Chip ID = 02h *2: Chip ID = 03h *3: Chip ID = 06h			Initial value	INCK = 37.125 MHz			INCK = 74.25 MHz		
	Register	Address ( ) : I^2C	bit		1080p LVDS	1080p CSI-2	720p	1080p LVDS	1080p CSI-2	720p
INCKSEL1	—	5Ch *1 (305Ch)	[7:0]	0Ch	18h	18h	20h	0Ch	0Ch	10h
INCKSEL2	—	5Dh *1 (305Dh)	[7:0]	00h	00h	03h	00h	00h	03h	00h
INCKSEL3	—	5Eh *1 (305Eh)	[7:0]	10h	20h	20h	20h	10h	10h	10h
INCKSEL4	—	5Fh *1 (305Fh)	[7:0]	01h	01h	01h	01h	01h	01h	01h
INCKSEL5	—	5Eh *2 (315Eh)	[7:0]	1Bh	1Ah	1Ah	1Ah	1Bh	1Bh	1Bh
INCKSEL6	—	64h *2 (3164h)	[7:0]	1Bh	1Ah	1Ah	1Ah	1Bh	1Bh	1Bh
INCKSEL7	—	80h *3 (3480h)	[7:0]	92h	49h	49h	49h	92h	92h	92h

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register Hold Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
REGHOLD	—	01h (3001h)	[0]	0h	0: Invalid 1: Valid (Register hold)



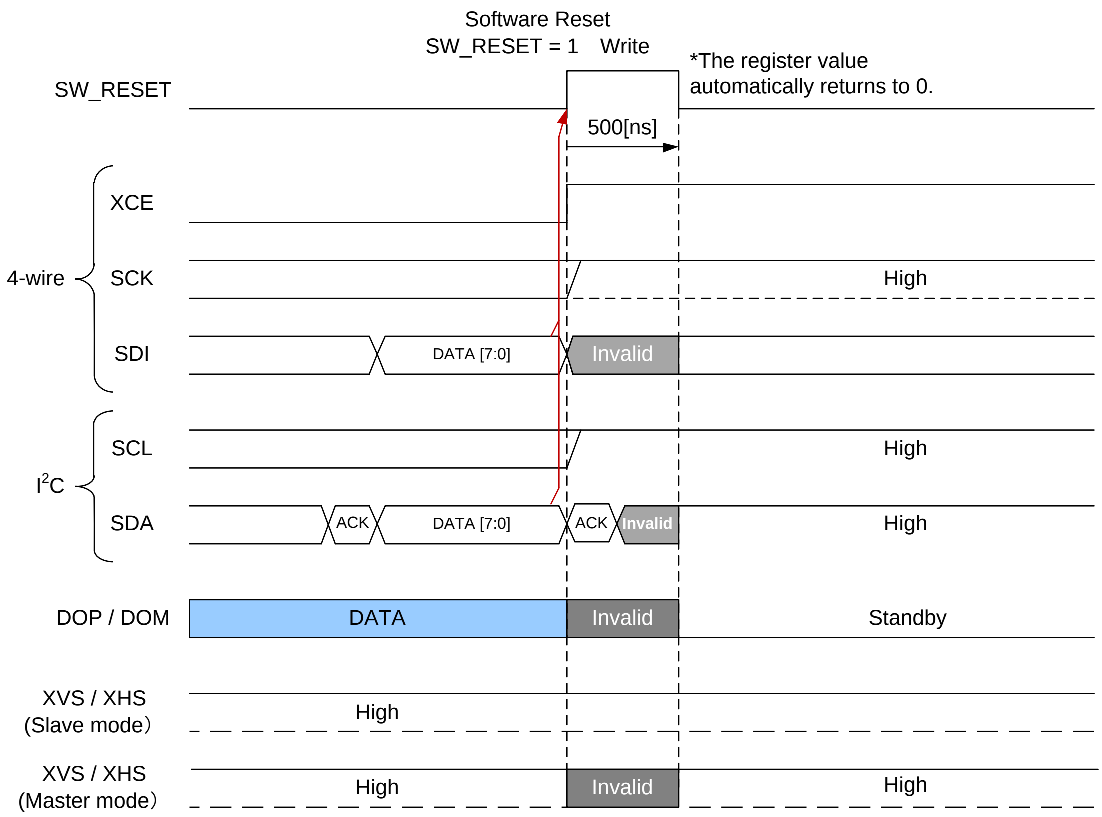
Register Hold Setting

Software Reset (Low voltage LVDS serial only)

This function is prohibited in CSI-2 output mode.
Software reset can be performed by register setting using the register SW_RESET.Sensor reset is performed by setting SW_RESET = 1. However, the communication to continuous address cannot use. The registers become initial state and standby 500 ns after setting SW_RESET = 1. The SW_RESET signal returns to "0" automatically.
The DLOPA-D/DLOMA-H/DCKP/DCKM terminal will be Hi-Z.
The XVS and XHS output High in master mode. Input High to the XVS and XHS before setting SW_RESET = 1 in slave mode. Follow the sequence in the item of "Standby Mode" to perform register initial setting and standby cancel from standby state.

Software Reset Register Setting

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I²C	bit		
SW_RESET	—	03h (3003h)	[0]	0h	0: Normal Operation 1: Reset



Software Reset

Mode Transitions

When changing the operating mode during sensor drive operation, set via sensor standby. However, these transitions that described below can be transitions without standby.

- ◆Change the number of vertical lines (In sensor master mode, change the VMAX. In sensor slave mode, change the period of XVS input.)
- ◆Horizontal and vertical scan direction. (When the vertical scan direction is changed, an invalid frame generates during transition.)
- ◆Change the HCG mode and LCG mode.
- ◆Change the mode between All-pixel scan and Window cropping. (However, It is case that transitions by not changing register HMAX and FRSEL. In addition, an invalid frame generates during transition.)

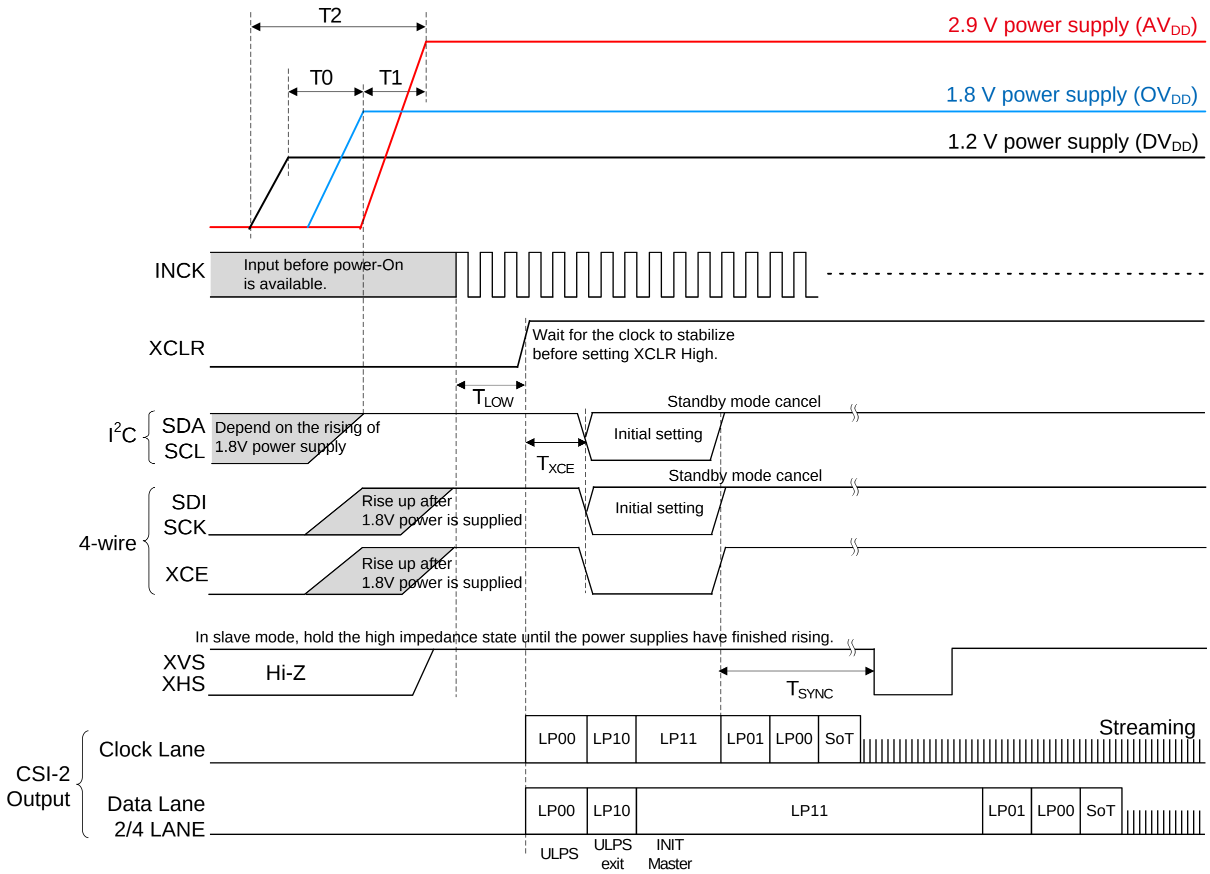
When changing input INCK frequency (register INCKSEL1, INCKSEL2, INCKSEL3, INCKSEL4, INCKSEL5, INCKSEL6, and INCKSEL7 change) or when operating mode transition that changes output bit width (register ODBIT) or output format (register OPORTSEL [3:0]), always start the operation via sensor standby after changing mode during standby following the standby cancel sequence.

When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Power-on and Power-off Sequence

Power-on sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 2.9 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. Start master clock (INCK) input after turning On the power supplies.
3. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.) In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}).
4. The system clear is applied by setting XCLR to High level. However, the maser clock needs to stabilize before setting the XCLR pin to High level.
5. Make the sensor setting by register communication after the system clear. A period of 20 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE. In I^2C communication, XCE is fixed to High.

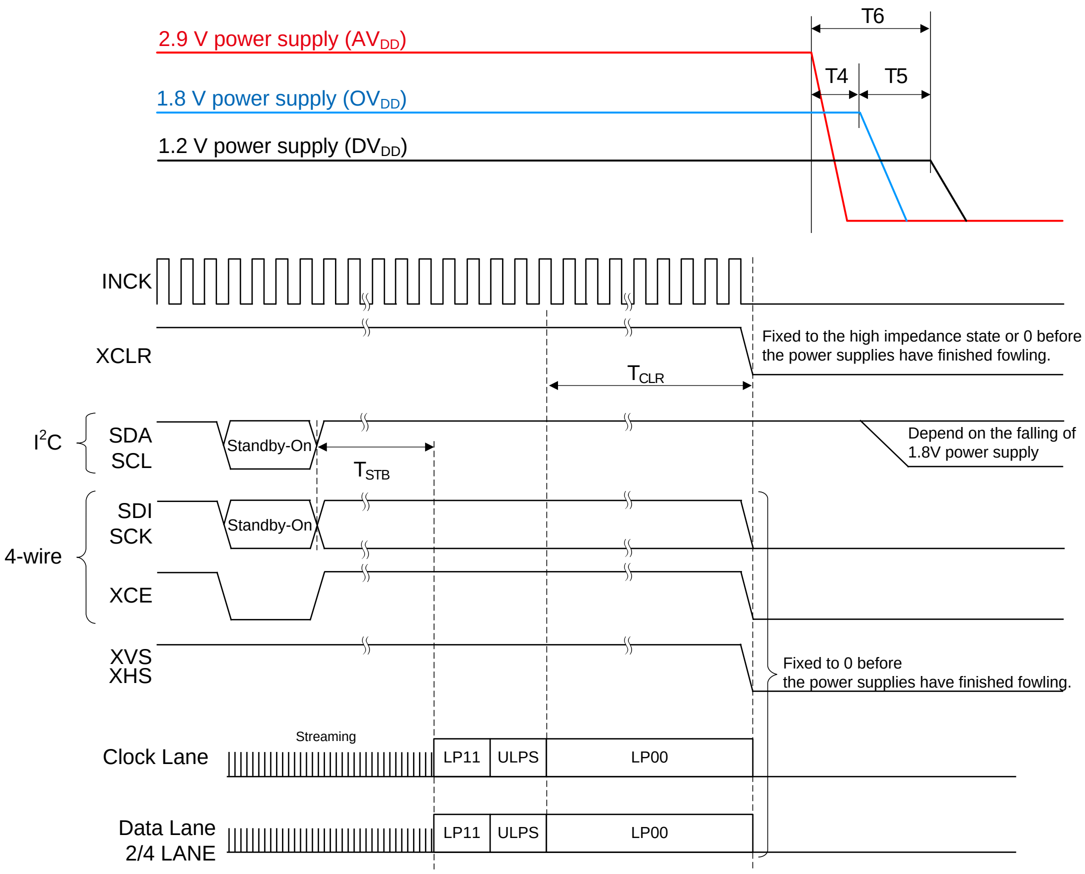


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 2.9 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
INCK active → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → Communication start	T_{XCE}	20	—	µs
Standby OFF (communication) → External input XHS,XVS (slave mode only)	T_{SYNC}	20	—	ms

Power-off sequence

Turn Off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, OMODE, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



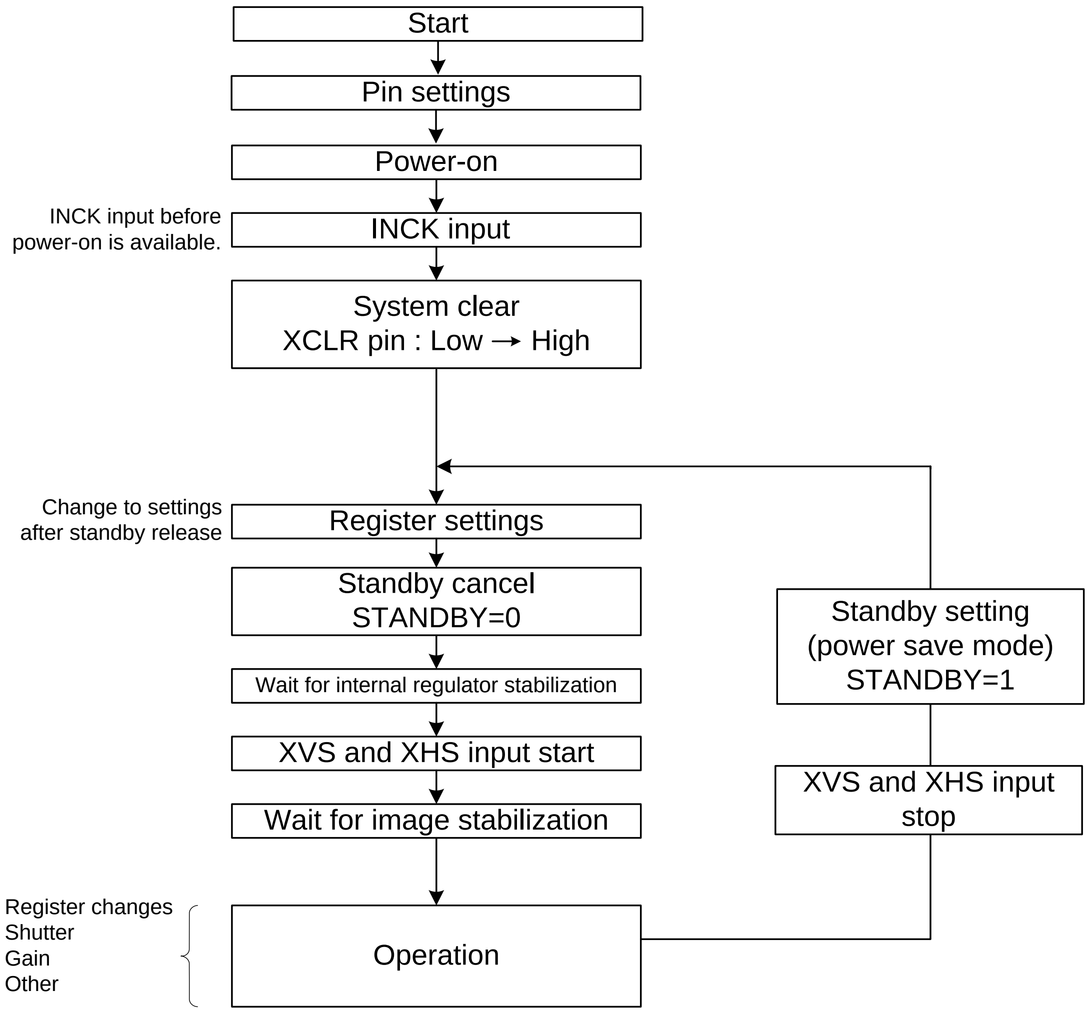
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
Standby ON (communication) → LP11 mode start	T_{STB}	Until FE		—
LP00 → XCLR falling	T_{CLR}	128	—	cycle
2.9 V power shut down → 1.8 V power shut down	T4	0	—	ns
1.8 V power shut down → 1.2 V power shut down	T5	0	—	ns
Shut down time of all power supply	T6	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

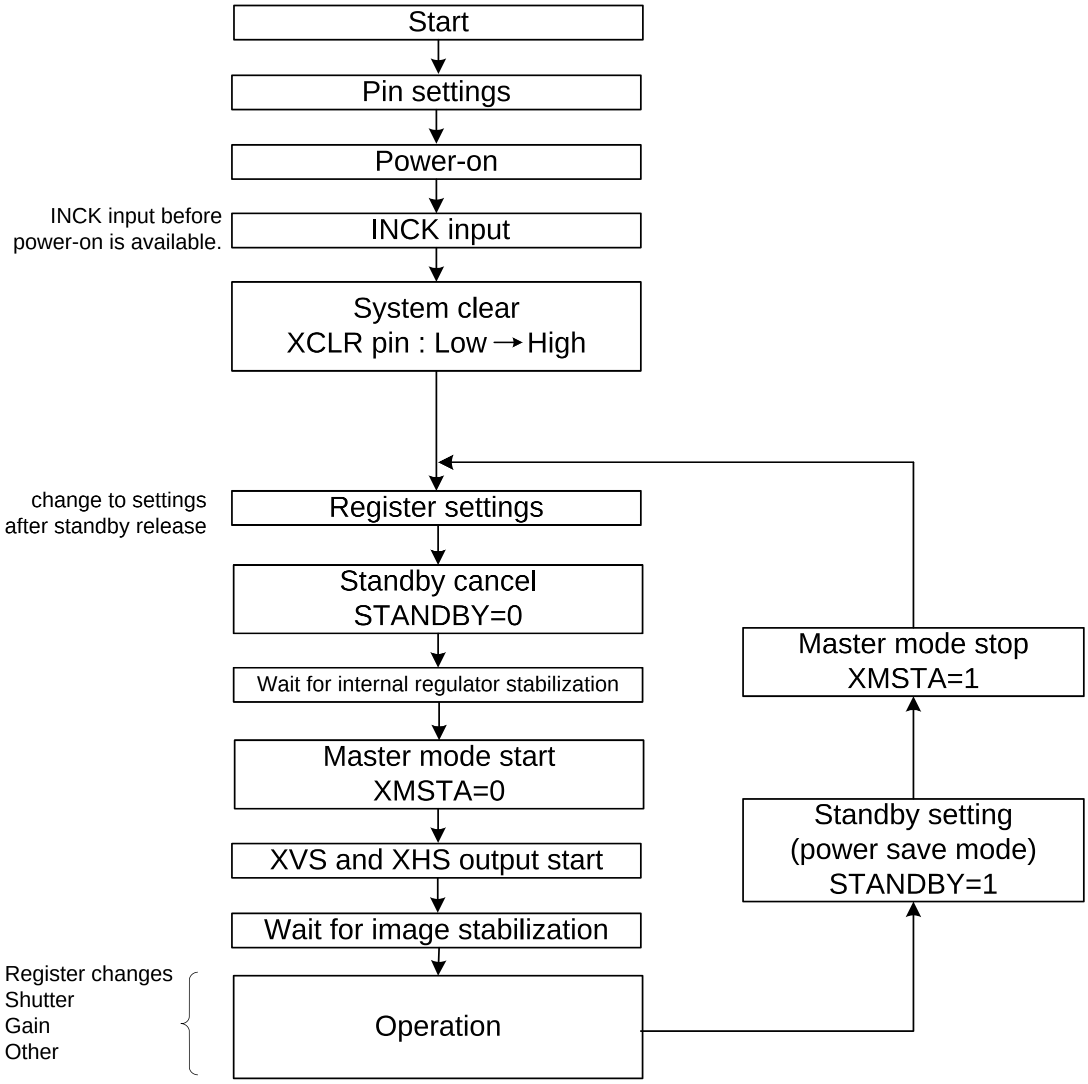
The figure below shows operating flow in sensor slave mode.
For details of "Power-on" to "Reset cancel", see the item of "Power-on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

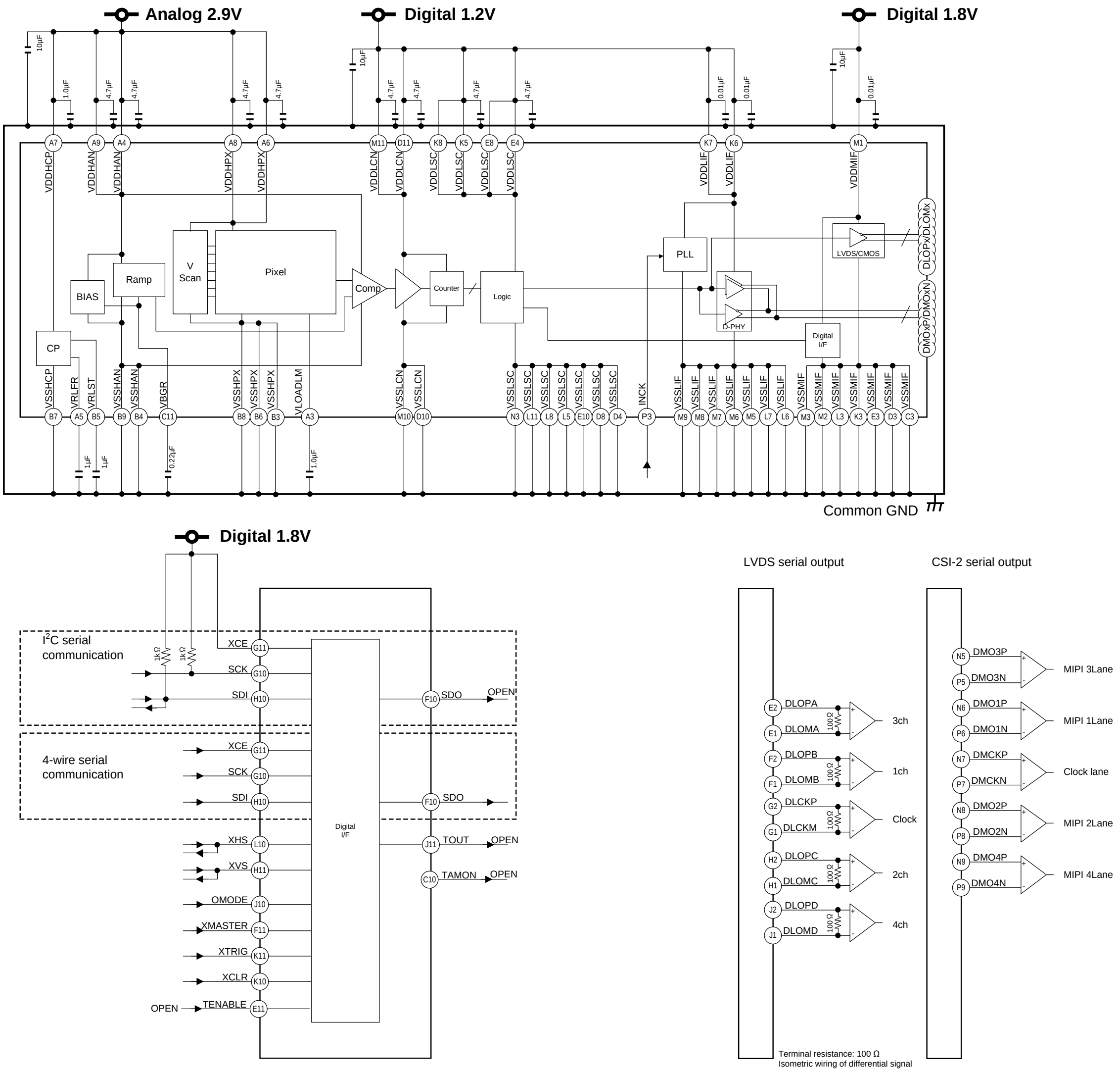
Setting Flow in Sensor Master Mode

The figure below shows operating flow in sensor master mode.
For details of "Power-on" to "Reset cancel", see the item of "Power on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
In master mode, “Master mode start” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

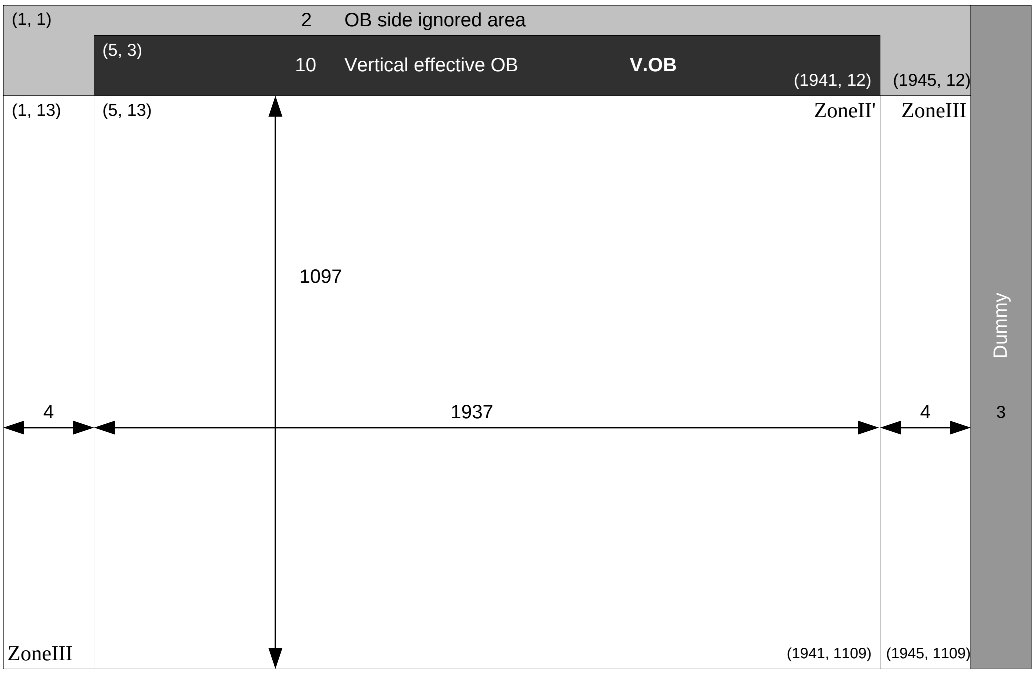
Spot Pixel Specifications

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 °C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		0 to II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	TBD% ≤ D	TBD	No evaluation criteria applied			1	
White pixels in the dark	TBD mV ≤ D	TBD		No evaluation criteria applied		2	1/30 s storage
Black pixels at signal saturated	D ≤ TBD mV	TBD	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C / LCG mode)	Annual number of occurrence
5.6 mV or higher	TBD pcs
10.0 mV or higher	TBD pcs
24.0 mV or higher	TBD pcs
50.0 mV or higher	TBD pcs
72.0 mV or higher	TBD pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

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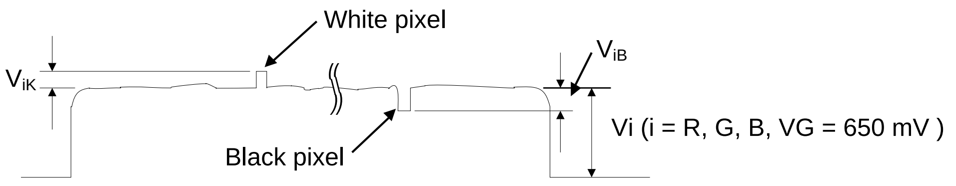
Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 650 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

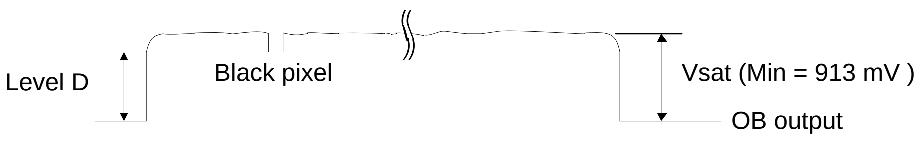
   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

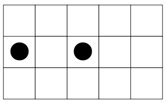
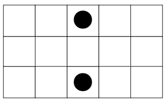


Signal output waveform of R/G/B channel

Spot Pixel Pattern Specification

White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

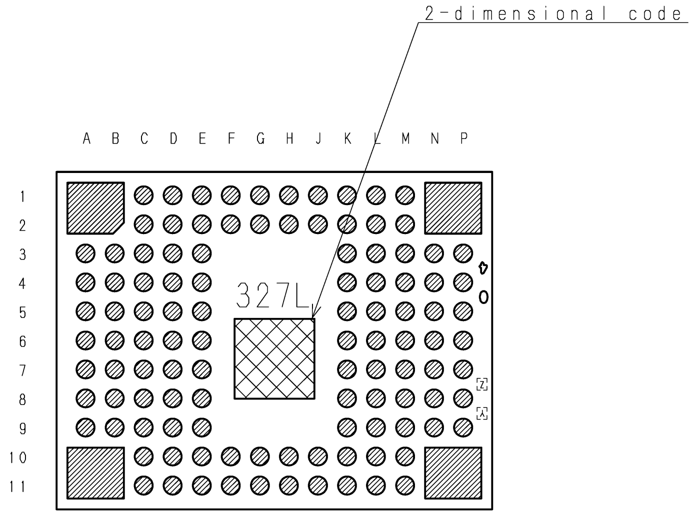
List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern 	It provides by color filter array described in the left.	White pixel Black pixel Bright pixel
1		Same color	Rejected
2		Same color	Rejected

Note) 1."●" shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated "Rejected" is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking

Tentative



Y : In English upper case character, One character
Z : Number, single number

DRAWING No. AM-※327LQR(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

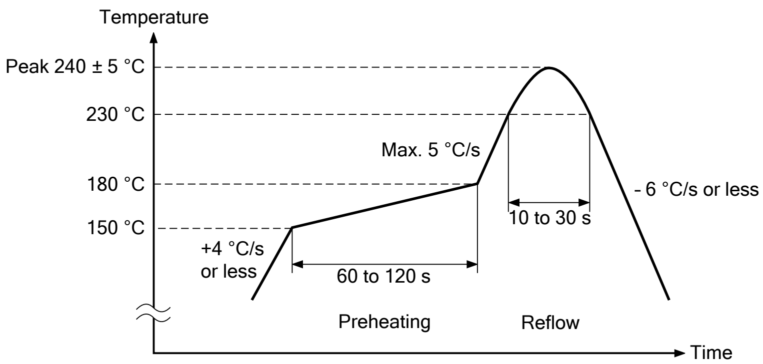
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package.
Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

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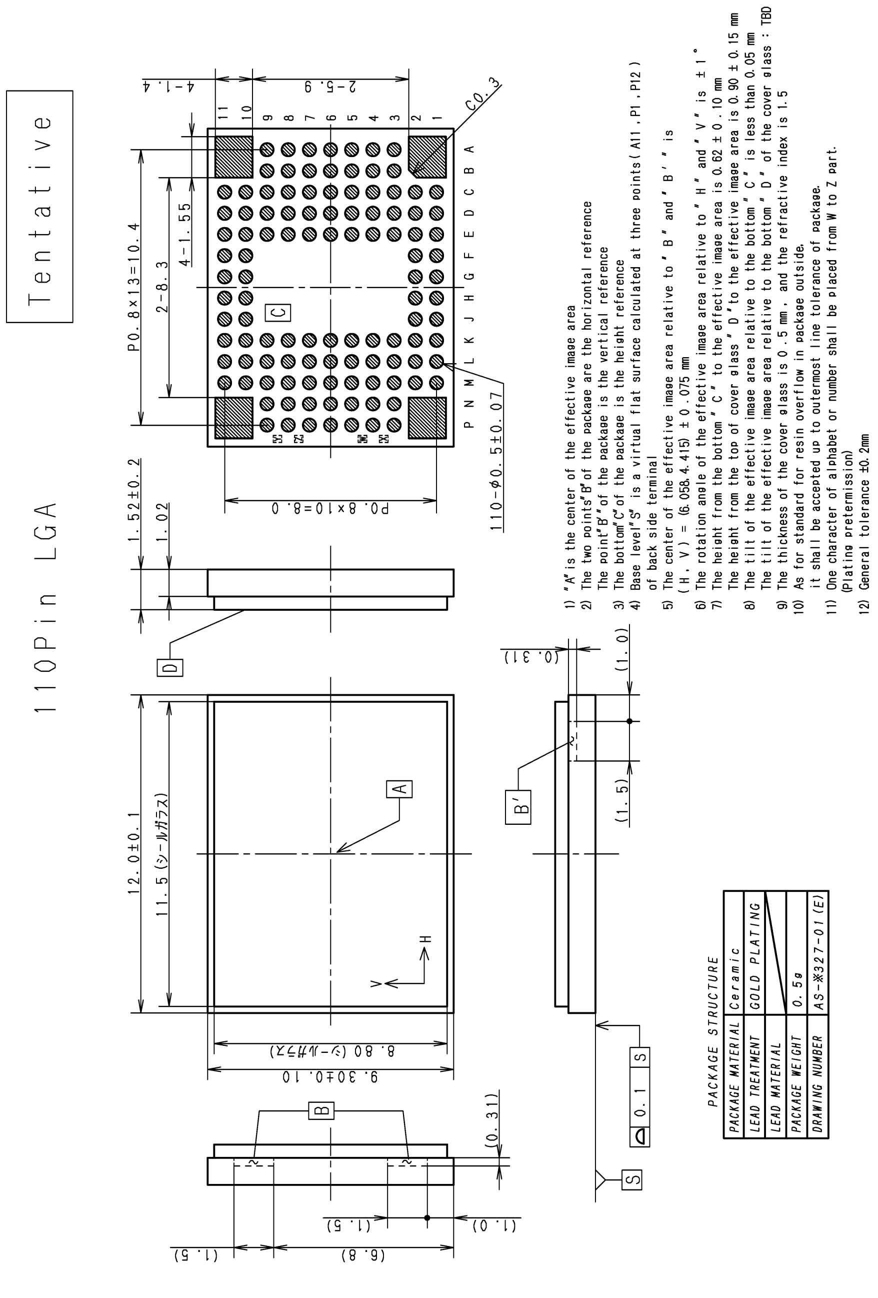
Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

Exmor R

* Exmor R is a trademark of Sony Corporation. The Exmor R is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type.

STARVIS

* STARVIS is a trademark of Sony Corporation. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for surveillance camera applications. It features a sensitivity of 2000 mV or more per 1 μm^2 (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

Revision History

Date of change	Ver	Page	Contain of Change
2017/02/23	0.1	—	First Edition
2017/05/25	0.2	85	Correction：d)2Lane-RAW10 -> d)4Lane-RAW10
		105	Correction：Package Outline