IMS1400M

High Performance 16K Static RAM MIL-STD-883C

FEATURES

- Full Military Temperature Operating Range (-55°C to +125°C)
- MIL-STD-883C Processing
- 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

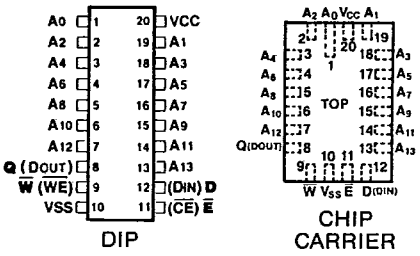
DESCRIPTION

The INMOS IMS1400M is a high performance 16Kx1 Static RAM processed in full compliance to MIL-STD-883C with access times as fast as 45nsec and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary NMOS technology.

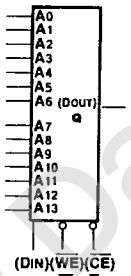
The IMS1400M features fully static operation requiring no external clocks or timing strobes with equal access and cycle times. Additionally, the IMS1400M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode reducing consumption to less than 165mW.

The IMS1400M is a high speed VLSI RAM intended for military applications which demand superior performance and reliability.

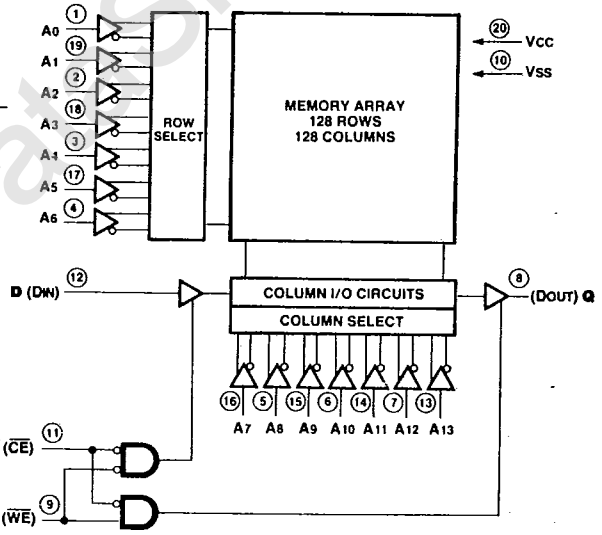
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0 - A13 ADDRESS INPUTS	VCC POWER (+5V)
W (WE) WRITE ENABLE	VSS GROUND
E (CE) CHIP ENABLE	
D (DIN) DATA INPUT	
Q (DOUT) DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias. . . . . −65°C to 135°C
Storage Temperature (Ambient). . . . . −65°C to 150°C
Power Dissipation. 1W
DC Output Current. 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \ge V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	µA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 16mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels. . . . . V_{SS} to 3V
Input Rise and Fall Times. 5ns
Input and Output Timing Reference Levels. 1.5V
Output Load. . . . . See Figure 1

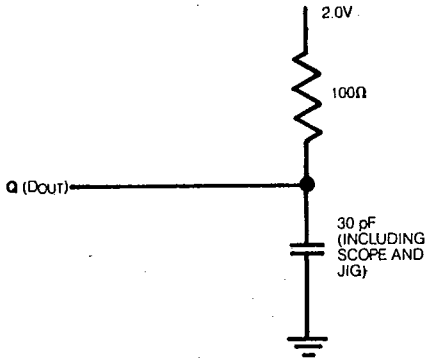
Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ TA ≤ 125°C) (Vcc = 5.0V ±10%)

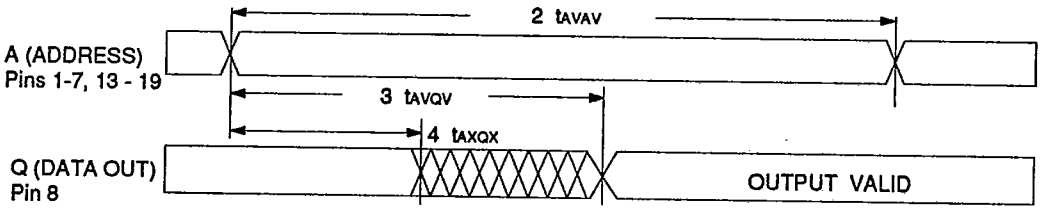
READ CYCLE

T-46-23-05

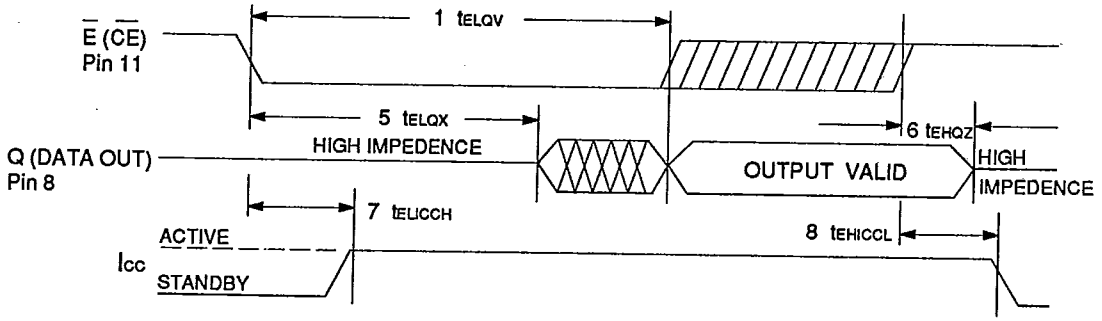
NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	tELQV	tACS	Chip Enable Access Time		45		55		70	ns	
2	tAVAV	tRC	Read Cycle Time	40		50		65		ns	c
3	tAVQV	tAA	Address Access Time		40		50		65	ns	d
4	tAXQX	tOH	Output Hold After Address Change	3		3		0		ns	
5	tELQX	tLZ	Chip Enable to Output Active	3		5		5		ns	
6	tEHQZ	tHZ	Chip Disable to Output Disable	0	25	0	30	0	40	ns	f
7	tELICCH	tPU	Chip Enable to Power Up	0		0		0		ns	j
8	tEHICCL	tPD	Chip Enable to Power Down	0	45	0	55	0	70	ns	j
		tT	Input Rise and Fall Times		50		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2 [c]



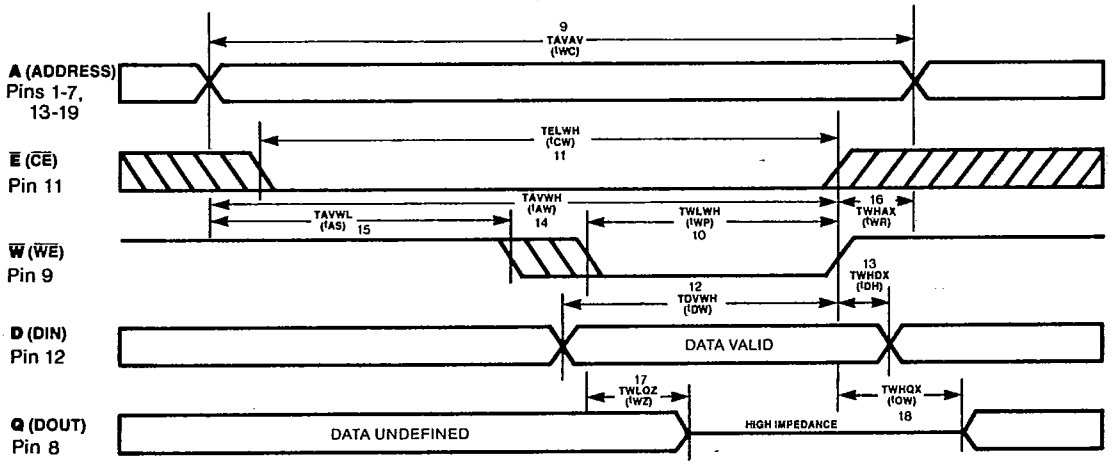
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		30		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		8		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	8		8		8		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	25	0	30	0	40	ns	g, j

Note f: Measured ±200mV from steady state output voltage.
Note g: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

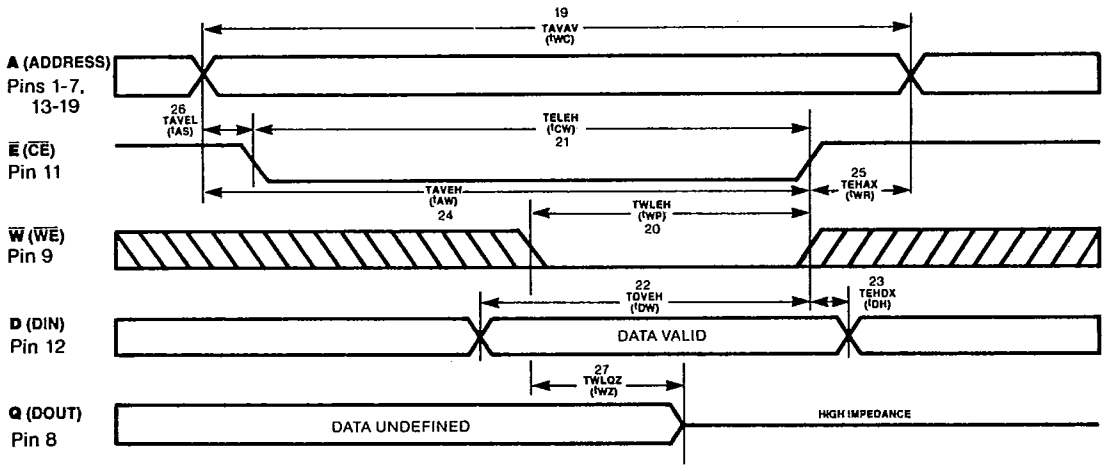
WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

T-46-23-05

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		10		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	−5		−5		−5		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1400M has two control inputs: Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), 14 address inputs, a data in (D_{IN}) and a data out (D_{OUT}).

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select one memory cell out of 16,385. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than ¼ of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the input (D_{IN}) is written into the selected cell, and the output (D_{OUT}) is in high impedance.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, D_{OUT} becomes active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, D_{OUT} remains in the high impedance state.

APPLICATION

To ensure proper operation of the extended temperature IMS1400M in a system environment, it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see Figure 2). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

Also, to prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry.

TERMINATION

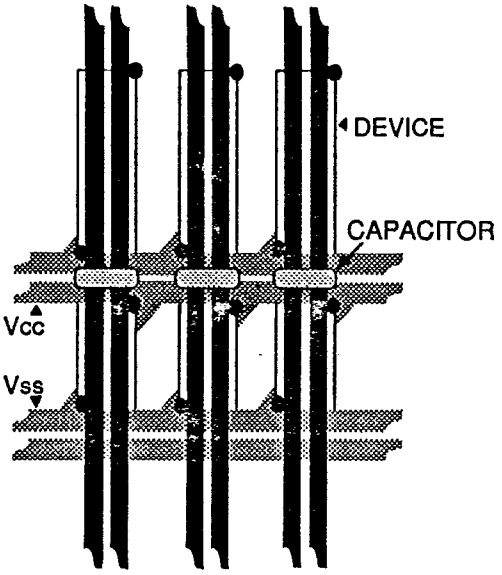
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

The use of proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are some of the most important, yet basic rules to be followed.

The rules are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1400M	45ns	CERAMIC DIP	IMS1400S-45M
	45ns	CERAMIC LCC	IMS1400N-45M
	55ns	CERAMIC DIP	IMS1400S-55M
	55ns	CERAMIC LCC	IMS1400N-55M
	70ns	CERAMIC DIP	IMS1400S-70M
	70ns	CERAMIC LCC	IMS1400N-70M