ILA6083

PWM Power Control with Interference Suppression

Description

ILA6083 is a PWM IC in bipolar technology for thecontrol of an N-channel power MOSFET used as a high side switch. The IC is ideal for the use in the brightness control (dimming) of lamps e.g., in dashboard applications.

Features

·Pulse width modulation up to 2 kHz clock frequency
·Protection against short circuit, load dump
over–voltage and reverse Vs
·Duty cycle 15 to 100% continuously
·Reduced internal pulse slope of lamp's voltage
·High side switch
·Interference and damage protection according to VDE 0839 and ISO/TR 7637/1.
·Charge pump noise suppressed
·Ground wire breakage protection
·Low interference voltage
Case: DIP 8

Block Diagram

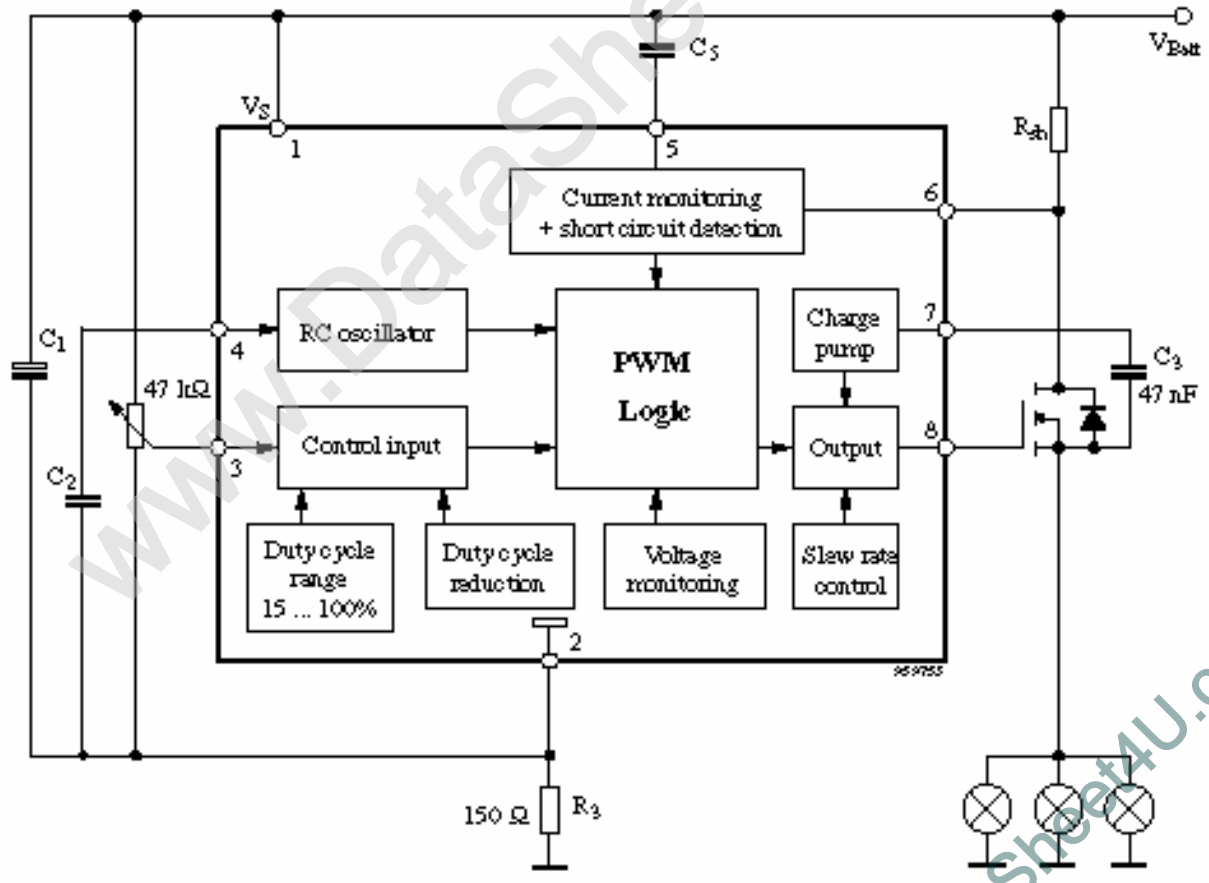
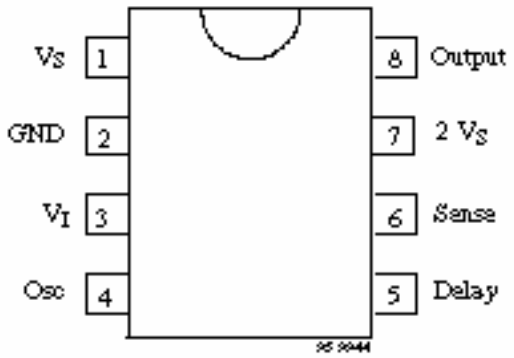


Figure 1. Block diagram with external circuit

Pin Description



Pin	Symbol	Function
1	V_S	Supply voltage V_S
2	GND	IC ground
3	V_I	Control input (duty cycle)
4	Osc	Oscillator
5	Delay	Short circuit protection delay
6	Sense	Current sensing
7	2 V_S	Voltage doubler
8	Output	Output

Functional Description

Supply Voltage, V_S or V_{Batt}, Pin 1

GND Pin 2

Control Input, Pin 3

The pulse width is controlled by means of an external potentiometer (47 kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 15 to 100%. It can be reduced by increasing the supply voltage as from V_{Batt} > 13 V. This produces a power reduction in the FET and increases the life time of lamps. It is possible to further restrict the duty cycle with the resistors R_1 and R_2.
Pin 3 is protected against short-circuit to V_{Batt} and ground GND (V_{Batt} ≤ 16.5 V).

Oscillator, Pin 4

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor, C_2. It is charged with a constant current, I, until the upper switching threshold is reached. A second current source is then activated which taps a double current, 2 I, from the charging current. The capacitor, C_2, is thus discharged by the current, I, until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

Example for oscillator frequency calculation:

$V_{I=100}$ $V_S \cdot \alpha_1$ $(V_{Batt}$ $I_S \cdot R_3) \cdot \alpha_1$

$V_{I<100}$ $V_S \cdot \alpha_2$ $(V_{Batt}$ $I_S \cdot R_3) \cdot \alpha_2$

V_{IL} $V_S \cdot \alpha_3$ $(V_{Batt}$ $I_S \cdot R_3) \cdot \alpha_3$

whereas

$V_{I=100}$ High switching threshold (100% duty cycle)

$V_{I<100}$ – High switching threshold(< 100% duty cycle)

V_{IL} Low switching threshold

α_1, α_2 and α_3 are fixed constant.

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

V_{Batt} = 12 V, I_S = 4 mA, R_3 = 150 Ω,
α_1 = 0.7, α_2 = 0.67 and α_3 = 0.28.

$V_{I=100}$ (12 V 4mA · 150Ω) · 0.7 ≈ 8 V

$V_{I<100}$ 11.4 V · 0.67 7.6 V

V_{IL} 11.4 V · 0.28 3.2 V

For a duty cycle of 100%, an oscillator frequency, f, is as follows:

$$f \quad \frac{I_{osc}}{2 \cdot (V_{I=100} \quad V_{IL}) \cdot C_2}$$, whereas C_2 68 nF and I_{osc} 45 µA

Therefore:

$$f \quad \frac{45\ \mu A}{2 \cdot (8\ V \quad 3.2\ V) \cdot 68\ nF} \quad 69\ Hz$$

For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f \quad \frac{I_{osc}}{2 \cdot (V_{I<100} \quad V_{IL}) \cdot C_2 + 2 \cdot V_{Batt} \cdot C_4}$$

whereas C_4 = 0. I = 45 µA and C_2 = 68 nF

$$\frac{45\ \mu A}{2 \cdot (7.6\ V \quad 3.2\ V) \cdot 68\ nF} \quad 75$$

But when C_4 = 1.8 nF, then

$$f - \frac{45\ \mu A}{2 \times (7.6\ V - 3.2\ V) \times 68\ nF + 2 \times 12\ V \times 1.8\ nF}$$

70 Hz

By selecting different values of C_2 and C_4, it is possible to have a range of oscillator frequency, f, from 10 to 2000 Hz as shown in the data sheet.

Output Slope Control

The slope of the lamp voltage is internally limited to reduce radio interference, by limitation of the open loop voltage gain of the PWM comparator.

This means the voltage rise on the lamp is proportional to the oscillator voltage increase at the switch over time multiplied with the corresponding amplification.

$dV_S/dt = \alpha_4 \cdot dV_4/dt =$
$2 \cdot \alpha_4 \cdot f \cdot (V_{TX} - V_{TL}) \cdot (V_{Batt} - I_S \cdot R_3)$
when
$f = 75$ Hz, $V_{TX} = V_{T < 100}$ and $\alpha_4 = 63$ $\{(63 \cdot R)/R\}$
we obtain
$dV_S/dt = 2 \cdot 63 \cdot 75 \cdot (0.67 - 0.28) \cdot (12 - 4\ mA \cdot 150)$
$= 42$ V/ms

With an external capacitor, C_4, the slope can be further reduced as follows:

$dV_S/dt = I/(C_4 + C_2/\alpha_4)$

when
$I = 45\ \mu A$, $C_4 = 1.8$ nF, $C_2 = 68$ nF and $\alpha_4 = 63$

then $dV_S/dt = 45\ \mu A/(1.8\ nF + 68\ nF/63) = 15.6$ V/ms

To damp oscillation tendencies, a resistance of 100 Ω in series with capacitance, C_4, is recommended.

Interference Suppression

"on board" radio reception according to VDE 0879 part 3/4.81
Test conditions:

Application circuit according to figure 2.

Load: nine 4 W lamps in parallel.

Duty cycle	= 18%
V_{Batt}	= 12 V
f_{Osc}	= 100 Hz

Overvoltage Detection

Stage 1:

If overvoltages $V_{Batt} > 20$ V (typ.) occur, the external transistor is switched off and on at $V_{Batt} < 18.5$ V (hysteresis).

Stage 2:

If $V_{Batt} > 28.5$ V (typ), the voltage limitation of the IC is reduced from 26 V to 20 V. The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between FET and lamps in the event of overvoltage pulses occuring (e.g. load dump). The short-circuit protection is not in operation. At V_{Batt} approx. < 23 V, the overvoltage detection stage 2 is switched off.

$V_{Lamp} = V_{Batt} - V_S - V_{GS}$
V_S = Supply voltage of the IC at overvoltage detection stage 2
V_{GS} = Gate – source voltage of the FET

Short-Circuit Protection and Current Sensing, Pins 5 and 6

1. Short-Circuit Detection and Time Delay, t_d

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ($V_{T2} \approx 90$ mV), the duty cycle is switched over to 100% and the capacitor C_5 is charged by a current source of 10 µA ($I_{dis} - I_{ch}$). The external FET is switched off after the cut-off threshold (V_{TL}) is reached. Renewed switching on of the FET is possible only after a power-on reset. The current source, I_{ch}, ensures that the capacitor C_5 is not charged by parasitic currents.

Time delay, t_d is as follows:

$t_d = C_5 \times V_{TL}/(I_{dis} - I_{ch})$

With $C_5 = 100$ nF and $V_{TL} = 10.4$ V, $I_{dis} = 13\ \mu A$, $I_{ch} = 3\ \mu A$, we have

$t_d \quad 100\ nF \cdot 10.4\ V\ /(13\ \mu A - 3\ \mu A)$
104 ms.

2. Current limitation:

The lamp current is limited by a control amplifier to protect the external power transistor. The voltage drop across an external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of $V_{T1} \approx 100$ mV. Owing to the difference $V_{T1} - V_{T2} \approx 10$ mV, it is ensured that current limitation

occurs only when the short-circuit detection circuit has responded.

After a power-on reset, the output is inactive for half an oscillator cycle. During this time the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short-circuit when the IC is switched on for the first time.

Charge Pump and Output, Pins 7 and 8

Output, Pin 8, is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor C_3 (bootstrapping). In addition, a trickle charge is generated by an integrated oscillator ($f_0 \approx 400$ kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

Undervoltage Detection

In the event of voltages of approximately $V_{Batt} < 5.0$ V, the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately $V_{Batt} \geq 5.4$ V.

Ground-Wire Breakage

To protect the FET in the case of ground-wire breakage, a 820 kΩ resistor between gate and source it is recommended to provide proper switch-off conditions.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_S	25	V
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	–40 to +110	°C
Storage temperature range	T_{stg}	–55 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	120	K/W

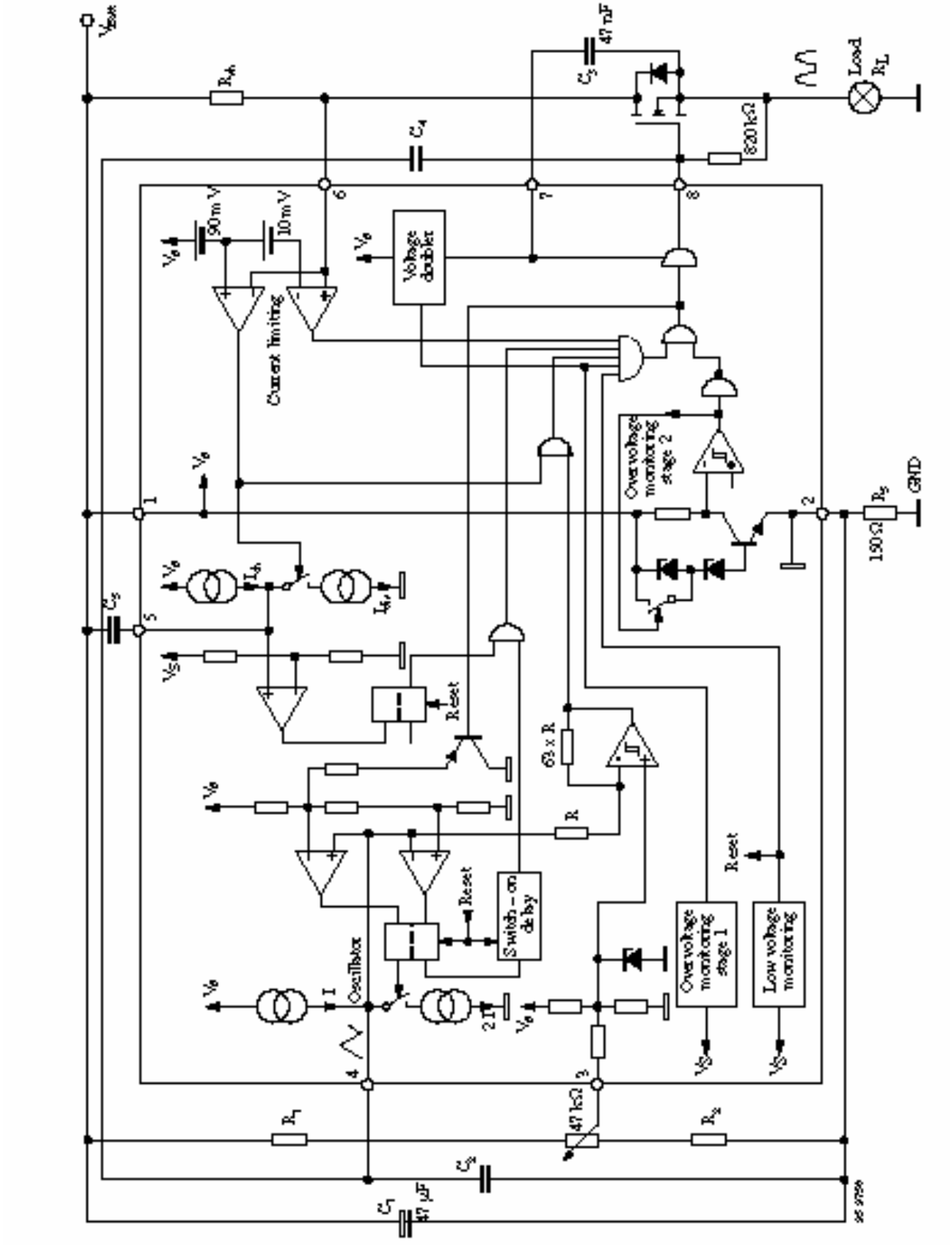
Electrical Characteristics

$T_{amb} = -40$ to +110°C, $V_{Batt} = 9$ to 16.5 V, (Basic function is guaranteed between 6.0 V to 9.0 V) reference point GND, unless otherwise specified (see figure 1).

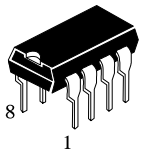
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Pin 1	I_S			7.9	mA
Supply voltage	Overvoltage detection, stage 1	V_{Batt}			25	V
Stabilized voltage	I_S = 10 mA Pin 1	V_Z	24.5		27.0	V
Battery undervoltage detection – on – off		V_{Batt}	 4.4 4.8	 5.0 5.4	 5.6 6.0	V

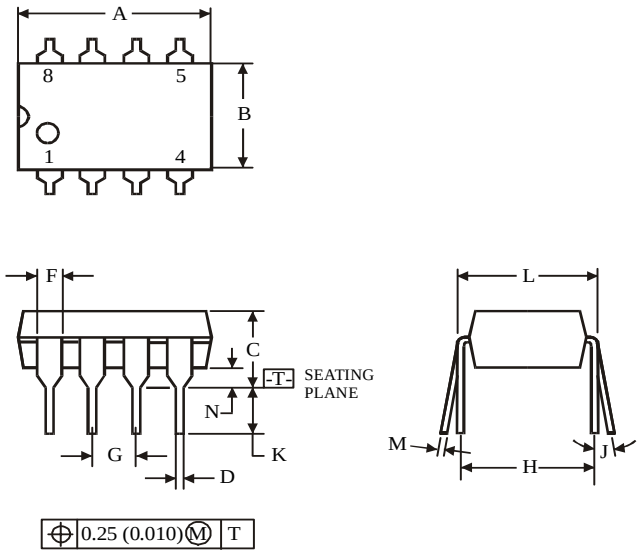
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Oscillator f = 10 to 2000 Hz	Pin 4					
Threshold cycle Upper	V_6 High, α_1 $\frac{V_{I1\infty}}{V_s}$	α_1	0.68	0.7	0.72	
	V_6 Low, α_2 $\frac{V_{I<1\infty}}{V_s}$	α_2	0.65	0.67	0.69	
Lower	α_3 $\frac{V_{I3}}{V_s}$	α_3	0.26	0.28	0.3	
Oscillator current	V_{Batt} = 12 V	$\pm I_{osc}$	34	45	54	µA
Frequency	C_4 open, C_2 = 68 nF, duty cycle = 50%	Δf	56	75	90	Hz
Battery overvoltage detection	Pin 8					
Stage 1:	Gate output: – switched off – switched on	V_{Batt}	18.3 16.7	20.0 18.5	21.7 20.3	V
Stage 2: Detection stage 2	 – on – off	V_{Batt}	25.5 19.5	28.5 23.0	32.5 26.5	V
Stabilized voltage	I_5 = 30 mA Pin 1	V_Z	18.5	20.0	21.5	V
Gate output	Pin 8					
Voltage	Low level	V_8	0.35	0.70	0.95	V
	V_{Batt} = 16.5 V, T_{amb} = 110°C, R_3 = 150 Ω				1.5	
	High level, duty cycle 100%	V_8		V_7		
Current	V_8 = Low level	I_8	1.0			mA
	V_8 = High level, $I_7 > \lvert I_8 \rvert$		–1.0			
Duty cycle	Min: C_2 = 68 nF Max: $V_{Batt} \leq$ 12.4 V V_{Batt} = 16.5 V, C_2 = 68 nF Pin 8	t_P/T	15 100 65	18 73	21 81	%
Short-circuit protection	Pin 6					
Short-circuit current regulation	$V_{T1} = V_S - V_6$	V_{T1}	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_6$	V_{T2}	75	90	105	mV
		$V_{T1} - V_{T2}$	3	10	30	
Short circuit recognition, V_{Batt} = 12 V	Pin 5					
Switched off threshold	$V_{TL} = V_S - V_5$	V_{TL}	10.2	10.4	10.6	V
Charge current		I_{ch}		13		µA
Discharge current		I_{dis}		3		µA
Capacitance current	$I_5 = I_{ch} - I_{dis}$	I_5	5	10	15	mA
Voltage doubler	Pin 7					
Voltage	Duty cycle 100%	V_7	2 V_S			
Oscillator frequency		f_7	280	400	520	kHz
Internal voltage limitation	I_7 = 5 mA or whichever is lower	V_7	26	27.5	30.0	V
			V_{S+14}	V_{S+15}	V_{S+16}	
Edge sleepness	$dv_8/dt = \alpha_4\ dV_4/dt$ dV_8/dt_{max}	α_4	53	63	72 130	V/ms

Application



N SUFFIX PLASTIC DIP
(MS – 001BA)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.