Integrated Device Technology, Inc.

64K x 16
32K x 16
CMOS STATIC RAM MODULE

IDT8MP624L
IDT8MP612L

FEATURES:

- High-density CMOS static RAM module 64K x 16 organization (IDT8MP624) or 32K x 16 option (IDT8MP612)
- Fast access time
  — 70ns (max.) over commercial temperature range
- Separate Upper byte (I/O_{6-16}) and Lower byte control allows for greater application flexibility
- Low-power consumption
- Offered in a vertically mounted 40-pin SIP (single in-line package) for maximum space-savings
- Cost-effective plastic SO's mounted on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

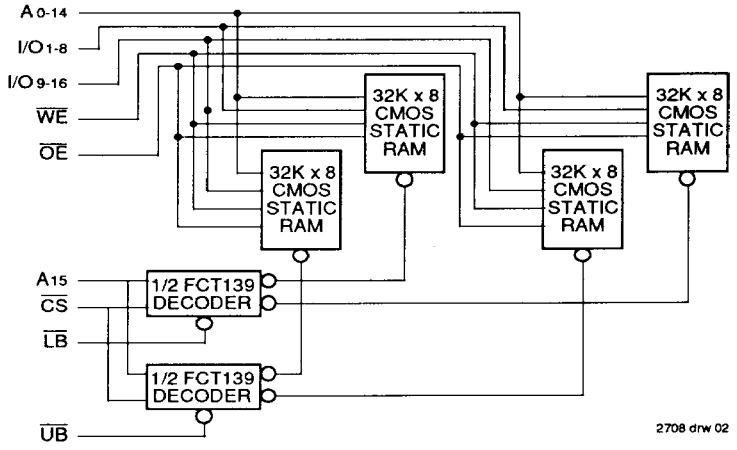
The IDT8MP624L/IDT8MP612L are high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four 32K x 8 static RAMs (IDT8MP624L) or two 32K x 8 static RAMs (IDT8MP612L) in plastic surface-mount packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP612L 32K x 16 option, A_{15} needs to be extremely grounded for proper operation.)

The IDT8MP624L/IDT8MP612L are available with access times as fast as 70ns for commercial temperature range, with maximum operating power consumption of only 825mW (64K x 16 option). The module also offers a full standby mode of 2.2mW (max.).

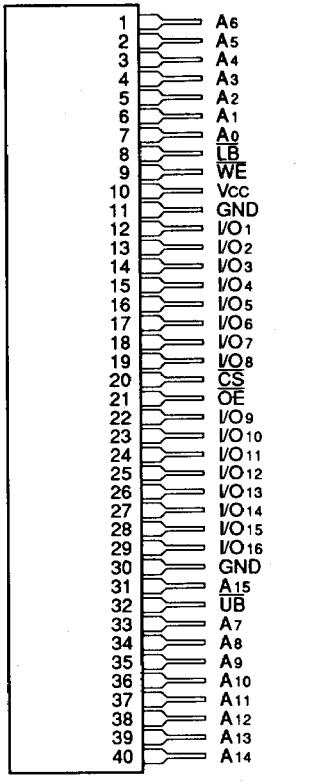
The IDT8MP624L/IDT8MP612L are offered in a 40-pin FR-4 SIP package. For the 32-pin JEDEC sidebrazed DIP, refer to the IDT8M624S/IDT8M612S.

All inputs and outputs of the IDT8MP624L/IDT8MP612L are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION[1]



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SIP
SIDE VIEW

NOTE:
1. For module dimensions, please refer to module drawing M39 (8MP624L) and M40 (8MP612L in the packaging section.
2. On the IDT8MP612L (32K x 16) option, A_{15} (Pin 31) requires external grounding for proper operation of the module.

PIN NAMES

A_{0-15}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

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NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT8MP624L Min.	IDT8MP624L Typ.(1)	IDT8MP624L Max.	IDT8MP612L Min.	IDT8MP612L Typ.(1)	IDT8MP612L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	—	20	80	—	20	80	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	—	80	150	—	80	150	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open, f = f_{MAX}	—	6	15	—	6	15	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	10	400	—	10	300	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1.0mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

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NOTE:
1. V_{CC} = 5V, T_A = +25°C

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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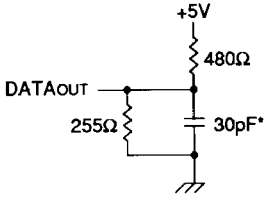

Figure 1. Output Load

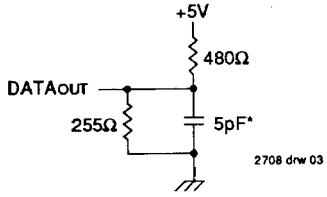

Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	IDT8MP624L70 IDT8MP612L70 Min.	Max.	IDT8MP624L85 IDT8MP612L85 Min.	Max.	IDT8MP624L100 IDT8MP612L100 Min.	Max.	Unit
Read Cycle								
tRC	Read Cycle Time	70	—	85	—	100	—	ns
tAA	Address Access Time	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	70	—	85	—	100	ns
tCLZ (1)	Chip Select to Output in Low Z	10	—	10	—	10	—	ns
tOE	Output Enable to Output Valid	—	40	—	50	—	60	ns
tOLZ (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
tCHZ (1)	Chip Select to Output in High Z	—	30	—	35	—	40	ns
tOHZ (1)	Output Disable to Output in High Z	—	30	—	35	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	ns
tPU (1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD (1)	Chip Deselect to Power Down Time	—	70	—	85	—	100	ns
Write Cycle								
tWC	Write Cycle Time	70	—	85	—	100	—	ns
tCW	Chip Select to End of Write	65	—	75	—	90	—	ns
tAW	Address Valid to End of Write	65	—	75	—	90	—	ns
tAS	Address Setup Time	5	—	5	—	5	—	ns
tWP	Write Pulse Width	60	—	70	—	80	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	ns
tWHZ (1)	Write Enable to Output in High Z	—	30	—	35	—	40	ns
tDW	Data to Write Time Overlap	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time	5	—	5	—	5	—	ns
tOW (1)	Output Active from End of Write	5	—	5	—	5	—	ns

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NOTE:
1. This parameter is guaranteed by design but not tested.

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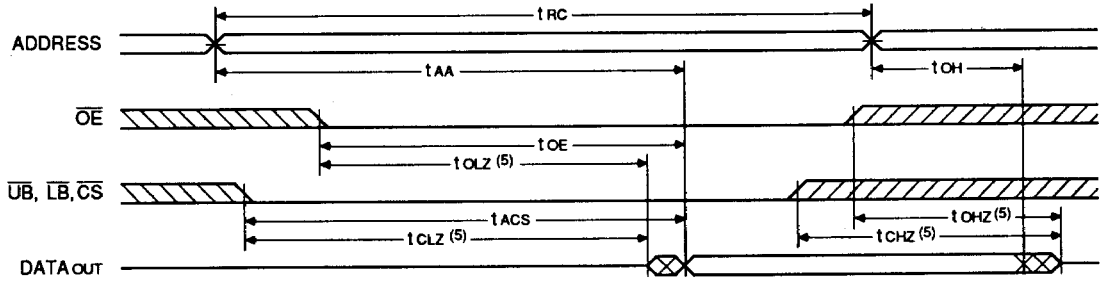
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



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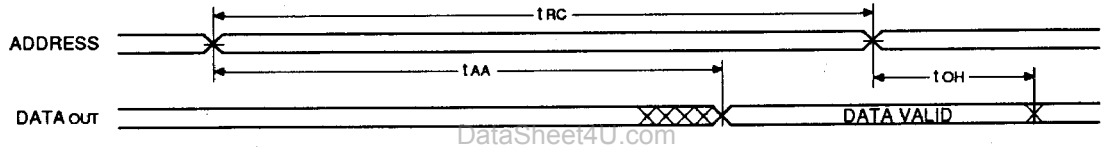
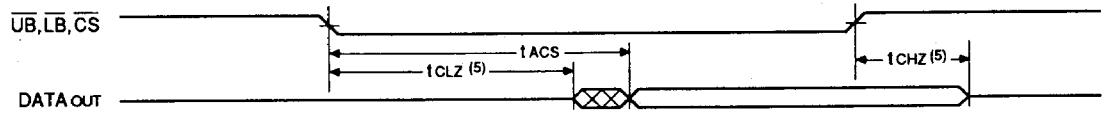
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2708 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



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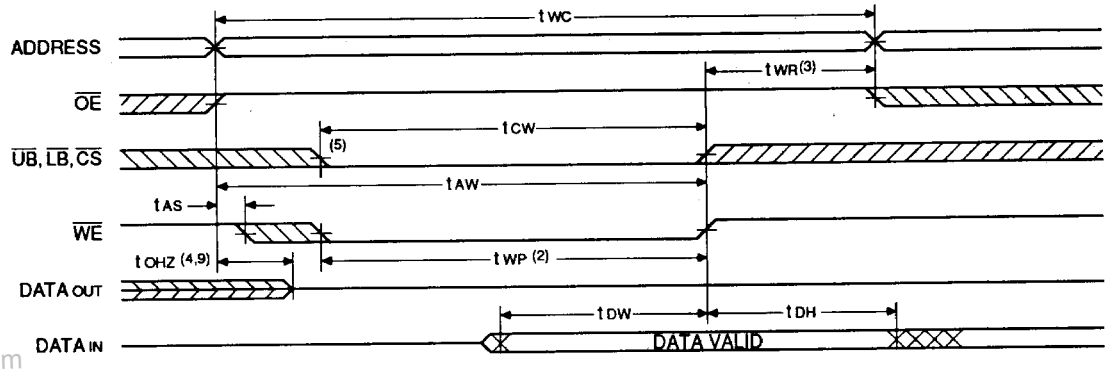
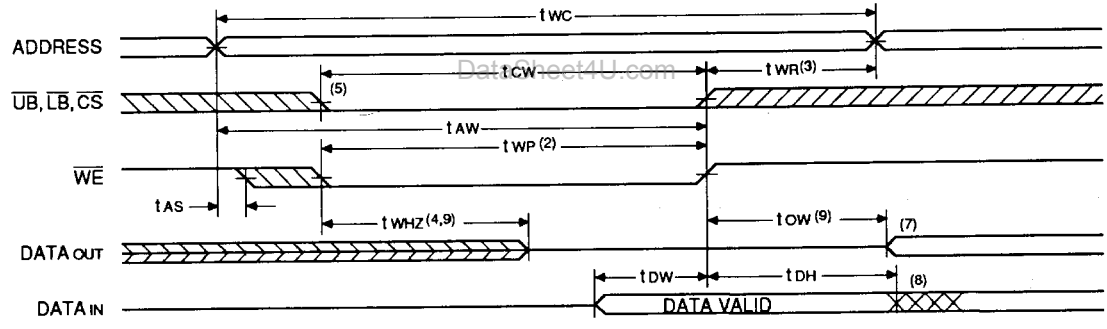
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL and $\overline{UB}$, $\overline{LB}$ = VIL for x16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2708 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



2708 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ or $\overline{UB}$ and $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS}$, $\overline{UB}$ and $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$, $\overline{UB}$ and $\overline{UB}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	DOUT 1-16	Active
Lower Byte Read	L	H	L	L	H	DOUT 1-8	Active (XB)
Upper Byte Read	L	L	H	L	H	DOUT 9-16	Active (XB)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (XB)
Upper Byte Read	L	L	H	H	H	High Z	Active (XB)
Write	L	L	L	X	L	DIN 1-16	Active
Lower Byte Read	L	H	L	X	L	DIN 1-8	Active (XB)
Upper Byte Read	L	L	H	X	L	DIN 9-16	Active (XB)

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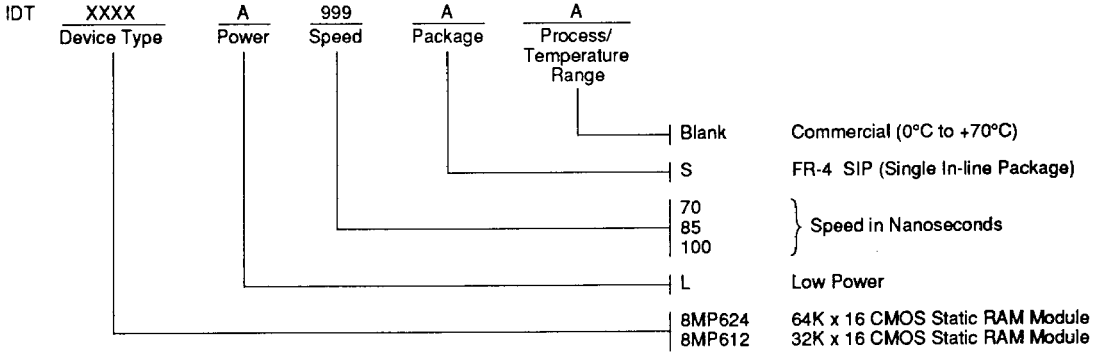
CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

2708 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



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