Dual Synchronous Ethernet Line Card PLL

Short Form Datasheet
IDT82V3396

FEATURES

HIGHLIGHTS

- Dual PLL chip:
  - Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
  - Exceeds GR-253-CORE (OC-12) and ITU-T G.813 (STM-4) jitter generation requirements
  - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for 1 Gigabit and 10 Gigabit Ethernet applications

MAIN FEATURES

- Employs PLL architecture to feature excellent jitter performance and minimize the number of external components
- Integrates 2 DPLLs; one can be used on the transmit path and the other on the receive path
- Supports programmable DPLL bandwidth: 18 Hz, 35 Hz, 70 Hz and 560 Hz
- Provides OUT1~OUT6 output clock frequencies up to 644.53125 MHz
  - Includes 25MHz, 125 MHz and 156.25 MHz for CMOS outputs
  - Includes 25.78125MHz, 128.90625 MHz and 161.1328125 MHz for CMOS outputs
  - Includes 25MHz, 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential outputs
  - Includes 25.78125 MHz, 128.90625 MHz, 161.1328125 MHz, 322.265625 MHz and 644.53125 MHz for differential outputs
- Provides IN1~IN6 input clock frequencies cover from 2 kHz to 156.25 MHz
- Supports Forced or Automatic operating mode switch controlled by an internal state machine. It supports Free- Run, Locked and Holdover modes
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides a 2 kHz, 4 kHz, or 8 kHz frame sync input signal, and a 2 kHz or 8 kHz frame sync output signals
- Provides a 1PPS sync input signal and a 1PPS sync output signal
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262. ITU-T G.813 and ITU-T G.783 Recommendations

OTHER FEATURES

- I2C and Serial microprocessor interface modes
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 72-pin QFN package, green package options available

APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipment
- Synchronous Ethernet equipment
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipment
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipment

DESCRIPTION

The IDT82V3396 Dual Synchronous Ethernet Line Card PLL is used to synchronize line cards in Synchronous Ethernet and SONET/SDH equipment, and in wireless base stations. The two independent timing paths allow the device to simultaneously synchronize transmit interfaces with the selected system backplane clock, and provide a recovered clock from a selected receive interface to the system backplane.

The IDT82V3396 accepts up to 6 input references operating at common Ethernet, SONET/SDH and PDH frequencies as well as other frequencies. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. The active reference for each of the two Digital PLLs (DPLLs) is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors.

The two IDT82V3396 timing paths are defined by independent DPLLs with embedded clock synthesizers. Both DPLLs support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode the DPLLs generate clocks based on the master clock alone. In Locked mode the DPLLs filter reference clock jitter with one of the following selectable bandwidths: 18 Hz, 35 Hz, 70 Hz or 560 Hz. In Locked mode the long-term DPLL frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies for short periods.

The IDT82V3396 requires a 12.8 MHz master clock for its reference monitors and other digital circuitry. The frequency accuracy of the master clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the master clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode.

The clocks synthesized by the IDT82V3392 DPLLs can be passed through one of the two independent jitter attenuating APLLs (for jitter sensitive applications). Any of the DPLL or APLL clocks can be routed through a mux to any of the six clock outputs via independent output dividers.

The IDT82V3392 accepts sync pulse inputs that are associated with input references; the sync pulses can have frequencies of 1 Hz, 2 kHz or 8 kHz. The device aligns its output sync pulses with the selected input sync pulse.

All IDT82V3392 read/write registers are accessed through a SPI/I2C microprocessor interface.

FUNCTIONAL BLOCK DIAGRAM

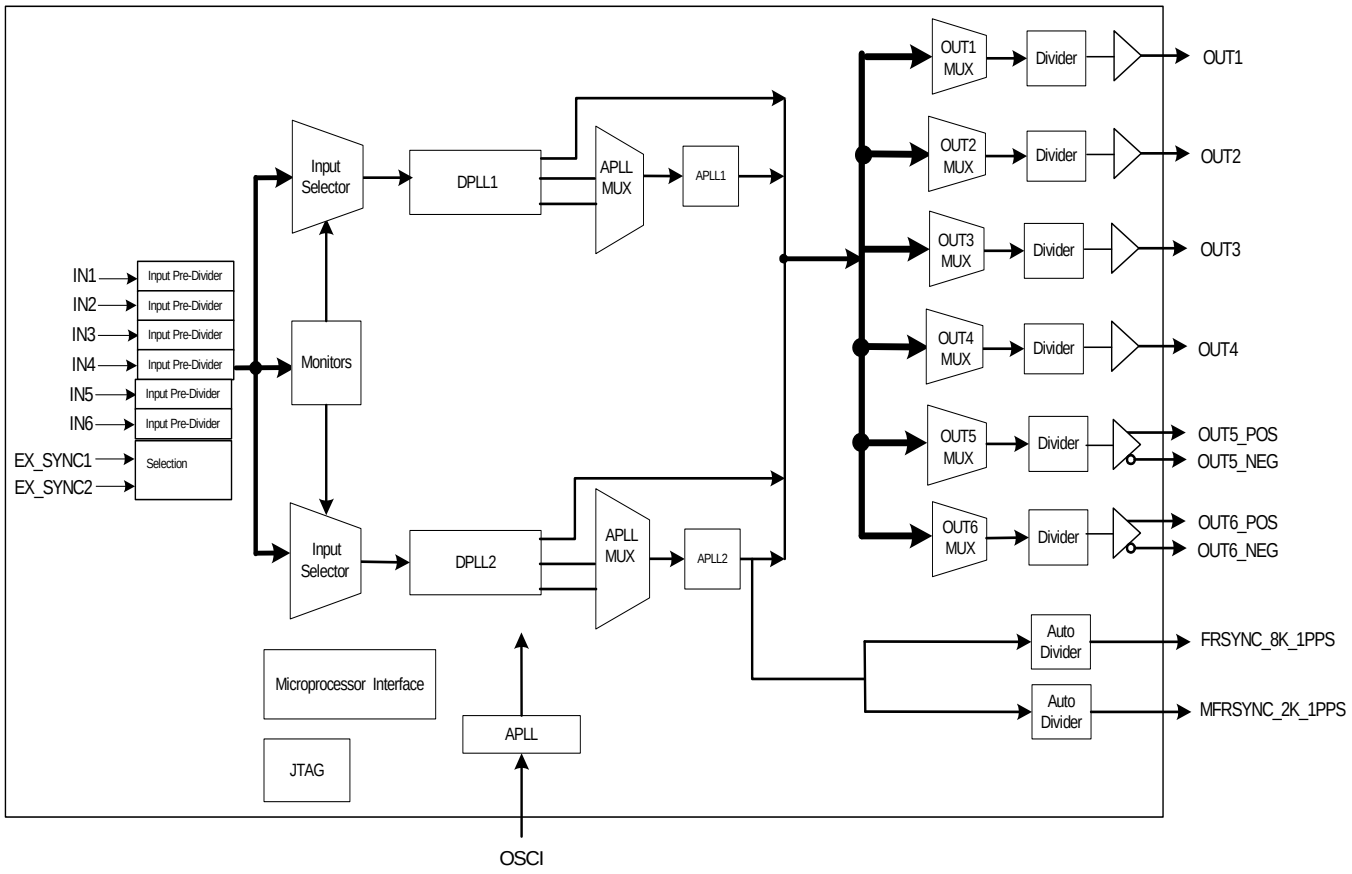


Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

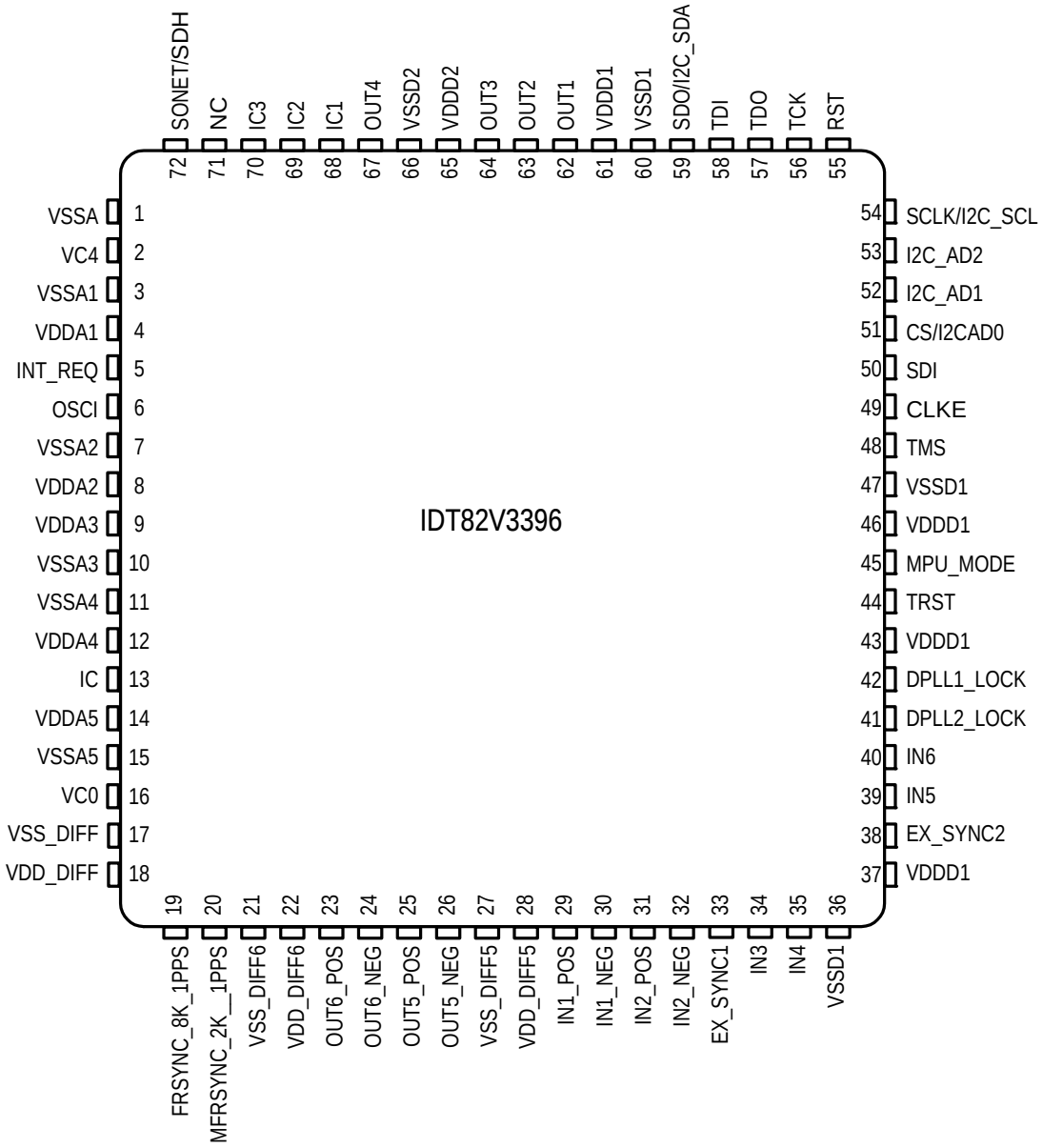


Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description [1, 2]
Global Control Signal				
OSCI	6	I	CMOS	OSCI: Crystal Oscillator Master Clock A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
SONET/SDH	72	I pull-down	CMOS	SONET/SDH: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect.
RST	55	I pull-up	CMOS	RST: Reset A low pulse of at least 50 µs on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
Frame Synchronization Input Signal				
EX_SYNC1	33	I pull-down	CMOS	EX_SYNC1: External Sync Input 1 A 2 kHz, 4 kHz, 8 kHz, or 1PPS signal is input on this pin.
EX_SYNC2	38	I pull-down	CMOS	EX_SYNC2: External Sync Input 1 A 2 kHz, 4 kHz, 8 kHz, or 1PPS signal is input on this pin.
Input Clock				
IN1_POS IN1_NEG	29 30	I	PECL/LVDS	IN1_POS / IN1_NEG: Positive / Negative Input Clock 1 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, or 156.25 MHz is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported.
IN2_POS IN2_NEG	31 32	I	PECL/LVDS	IN2_POS / IN2_NEG: Positive / Negative Input Clock 2 A 2kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, or 156.25 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported.
IN3	34	I pull-down	CMOS	IN3: Input Clock 3 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN4	35	I pull-down	CMOS	IN4: Input Clock 4 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN5	39	I pull-down	CMOS	IN5: Input Clock 5 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
IN6	40	I pull-down	CMOS	IN6: Input Clock 6 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
Output Frame Synchronization Signal				
FRSYN-C_8K_1PPS	19	O	CMOS	FRSYNC_8K_1PPS: 8 kHz Frame Sync Output An 8 kHz signal or a 1PPS sync signal is output on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1, 2]
MFRSYN-C_2K_1PPS	20	O	CMOS	MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output A 2 kHz signal or a 1PPS sync signal is output on this pin.
Output Clock				
OUT1 OUT2 OUT3 OUT4	62 63 64 67	O	CMOS	OUT1 ~ OUT4: Output Clock 1 ~ 4 A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 25MHz, 25.78125 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz or 156.25 MHz or 161.1328125 MHz clock is output on these pins.
OUT5_POS OUT5_NEG	25 26	O	PECL/LVDS	OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5 A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz, 156.25 MHz, 161.1328125 MHz, 311.04 MHz, 312.5 MHz, 322.265625 MHz, 622.08 MHz, 625 MHz or 644.53125 MHz clock is differentially output on these pair of pins.
OUT6_POS OUT6_NEG	23 24	O	PECL/LVDS	OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz, 156.25 MHz, 161.1328125 MHz, 311.04 MHz, 312.5 MHz, 322.265625 MHz, 622.08 MHz, 625 MHz or 644.53125MHz clock is differentially output on these pair of pins.
VC4	2	O	Analog	VC4: T4 APLL VC Output External RC filter
VC0	16	O	Analog	VC0: T0 APLL VC Output External RC filter
Lock Signal				
DPLL2_LOCK	41	O	CMOS	DPLL2_LOCK This pin goes high when DPLL2 is locked
DPLL1_LOCK	42	O	CMOS	DPLL1_LOCK This pin goes high when DPLL1 is locked
Microprocessor Interface				
CS / I2C_AD0	51	I/O pull-up	CMOS	CS: Chip Selection In Serial mode, this pin is an input.A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over. I2C_AD0: Device Address Bit 0 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
INT_REQ	5	O	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).
MPU_MODE	45	I pull-down	CMOS	MPU_MODE: Microprocessor Interface Mode Selection The device supports 2 microprocessor interface modes: I2C and Serial. During reset, these pins determine the default value of the MPU_SEL_CNFG[0] bit(b0, 7FH) as follows: 0: I2C mode 1: Serial mode After reset, these pins are general purpose inputs. The microprocessor interface mode is selected by the MPU_SEL_CNFG[0] bits (b0, 7FH). After reset de-assertion, wait 10 μs for the mode to be active. The value of this pin is always reflected by the MPU_PIN_STS[0] bits (b0, 02H).

Table 1: Pin Description (Continued)

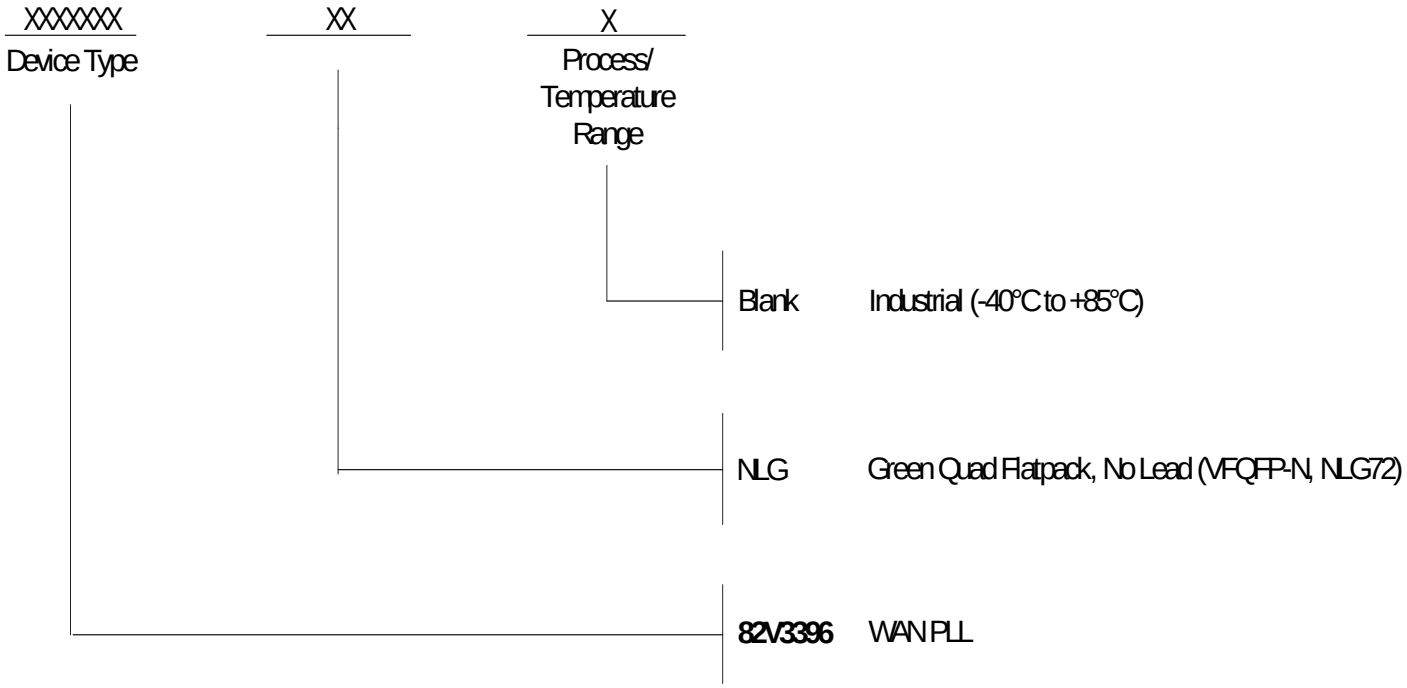
Name	Pin No.	I/O	Type	Description [1, 2]
CLKE	49	I/O pull-down	CMOS	CLKE: SCLK Active Edge Selection In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge.
SDI	50	I/O pull-down	CMOS	SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK.
SDO / I2C_SDA	59	I/O pull-down	CMOS	SDO: Serial Data Output In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. I2C_SDA: Serial Data Input/Output In I2C mode, this pin is used as the input/output for the serial data.
I2C_AD1	52	I pull-up	CMOS	I2C_AD1: Device Address Bit 1 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. In Serial mode, this pin should be connected to ground.
I2C_AD2	53	I pull-up	CMOS	I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. In Serial mode, this pin should be connected to ground.
SCLK / I2C_SCL	54	I pull-down	CMOS	SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. I2C_SCL: Serial Clock Line In I2C mode, the serial clock is input on this pin.
JTAG (per IEEE 1149.1)				
TRST	44	I pull-down	CMOS	TRST: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
TMS	48	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
TCK	56	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
TDI	58	I pull-up	CMOS	TDI: JTAG Test Data Input The test data are input on this pin. They are clocked into the device on the rising edge of TCK.
TDO	57	O	CMOS	TDO: JTAG Test Data Output The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH).
Power & Ground				
VDDD1	37,43, 46, 61	Power	-	VDDD1: Digital Core Power.
VDDD2	65	Power	-	VDDD2: CMOS CLK Output Power

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1, 2]
VDD_DIFF	18	Power	-	VDD_DIFF: Differential I/O Power Supply
VDD_DIFF6	22	Power	-	VDD_DIFF6: Differential I/O Power Supply
VDD_DIFF5	28	Power	-	VDD_DIFF5: Differential I/O Power Supply
VSSD1	36, 47, 60	Ground	-	VSSD1: Digital Core Ground
VSSD2	66	Ground	-	VSSD2: CMOS CLK Output Ground
VSS_DIFF	17	Ground	-	VSS_DIFF: Differential I/O Ground
VSS_DIFF6	21	Ground	-	VSS_DIFF6: Differential I/O Ground
VSS_DIFF5	27	Ground	-	VSS_DIFF5: Differential I/O Ground
VSSA	1	Ground	-	VSSA: Common Ground
VSSA1 VSSA2 VSSA3 VSSA4 VSSA5	3 7 10 11 15	Ground	-	VSSAn: T4 & T0 APLL Ground
VDDA1 VDDA2 VDDA3 VDDA4 VDDA5	4 8 9 12 14	Power	-	VDDAn: T4 & T0 APLL Power
Others				
IC IC1 IC2 IC3	13 68 69 70	-	-	IC: Internal Connected Internal Use. These pins should be left open for normal operation.
NC	71	-	-	NC: Not Connected

Note:
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.
2. The contents in the brackets indicate the position of the register bit/bits.
3. N x 8 kHz: $1 \leq N \leq 19440$.
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24
6. N x 13.0 MHz: N = 1, 2
7. N x 3.84 MHz: N = 1, 2, 4, 8

ORDERING INFORMATION



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