CMOS PARALLEL IN-OUT FIFO MODULE 8K x 9-BIT & 16K x 9-BIT

ADVANCE INFORMATION
IDT7M205
IDT7M206

Integrated Device Technology, Inc.

FEATURES:

- First-In, First-Out memory module
- 8K x 9 organization (IDT7M205)
- 16K x 9 organization (IDT7M206)
- Low power consumption
  - —Active: 900mW (typ.)
  - —Power Down: 50mW (typ.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- High-performance CEMOS™ technology
- Pin compatible with IDT7201 and Mostek MK4501, but with 16 times word depth (IDT7M205) or 32 times (IDT7M206)
- Module available with semiconductor components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

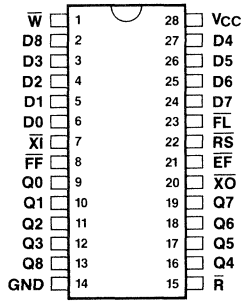
The IDT7M205/206 are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7203 (2K x 9) or four IDT7204 (4K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high-performance CEMOS technology. These devices utilize a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 75ns (13MHz) for commercial and 80ns (12.5MHz) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

IDT's military FIFO modules have semiconductor components 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



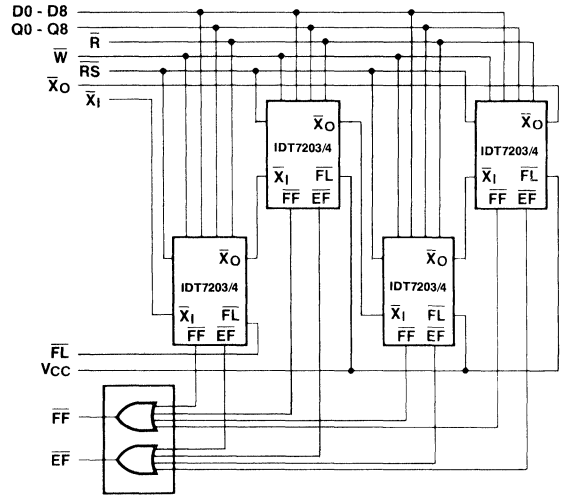
SSD7M203-001

DIP
TOP VIEW

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATA IN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATA OUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

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