

IDT LA-1 NSE System Level Architecture Model for Intel® IXA SDK Microengine Development Environment

Product Brief IDT75K134SLM

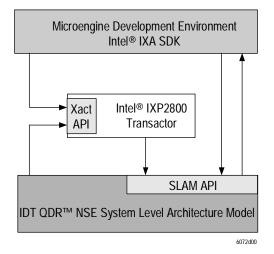
Introduction

Evolving network speeds require critical functions, such as forwarding and classification, to migrate towards dedicated hardware devices. IDT has introduced a family of network search engines with a LA-1 interface that connects seamlessly to network processors such as Intel's newest network processors. These devices accelerate search functions required for applications such as Access Control Lists (ACL), Flow Caching and Forwarding.

To further accelerate time to market, IDT provides IDT75K134SLM, System Level Architecture Model (SLAM), a cycle- and data-accurate simulation model allowing customers to evaluate packet-processing solutions in a simulation environment prior to system availability, thus, lowering cost and increasing performance.

The SLAM, supplied as a Windows TM 2000 DLL (dynamic-link library), fits into the Microengine Development Environment of the latest Intel® Internet Exchange Architecture (IXA) Software Development Kit, as shown in the Simulation System Block Diagram.

Figure 1.0 Simulation System Block Diagram



Features List

- The IDT75K134SLM is a full simulation model of the IDT LA-1 NSE, network search engine with a seamless LA-1 interface to Intel's IXP2400 and IXP2800 network processors. The SLAM implementation is both cycle- and data-accurate.
- The LA-1 interface conforms to Intel's Foreign Object Model interface for the Microengine Development Environment in the latest Intel® IXA SDK
- The SLAM simulates all of the LA-1 NSE's internal registers & Ternary Content Addressable Memory (CAM) core
- The SLAM supports all LA-1 NSE commands, including:
 - Standard Lookup
 - Multi-Hit Lookup
 - Multi-Database Lookup
 - Re-Issue Multi-Database Lookup
 - Multi-Hit Invalidate
 - Learn (per Database)
 - Read/Write internal resources
- ◆ The SLAM supports the following features:
 - Multiple contexts
 - Database configuration
 - A pool of 72-bit Global Mask registers
 - Indirection SRAM™
 - Aging
 - Error and warning messages for illegal or improper instruction combinations
 - Debug option, which allows the logging of events and error messages
- SLAM initialization module allows model customization
 - System hardware configuration
 - Search machine device cascade depth
 - Associated data SRAM support
 - Debug on/off and verbosity settings
- System Requirements
 - Microsoft Windows[™] 2000
 - 128 MB of RAM



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