



HIGH-SPEED 2K x 8 FourPort™ STATIC RAM

IDT7052S/L

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- ◆ **High-speed access**
 - Commercial: 20/25/35ns (max.)
 - Industrial: 25ns (max.)
 - Military: 25/35ns (max.)
- ◆ **Low-power operation**
 - IDT7052S
 - Active: 750mW (typ.)
 - Standby: 7.5mW (typ.)
 - IDT7052L
 - Active: 750mW (typ.)
 - Standby: 1.5mW (typ.)
- ◆ **True FourPort memory cells which allow simultaneous access of the same memory locations**
- ◆ **Fully asynchronous operation from each of the four ports: P1, P2, P3, P4**
- ◆ **Versatile control for write-inhibit: separate $\overline{\text{BUSY}}$ input to control write-inhibit for each of the four ports**

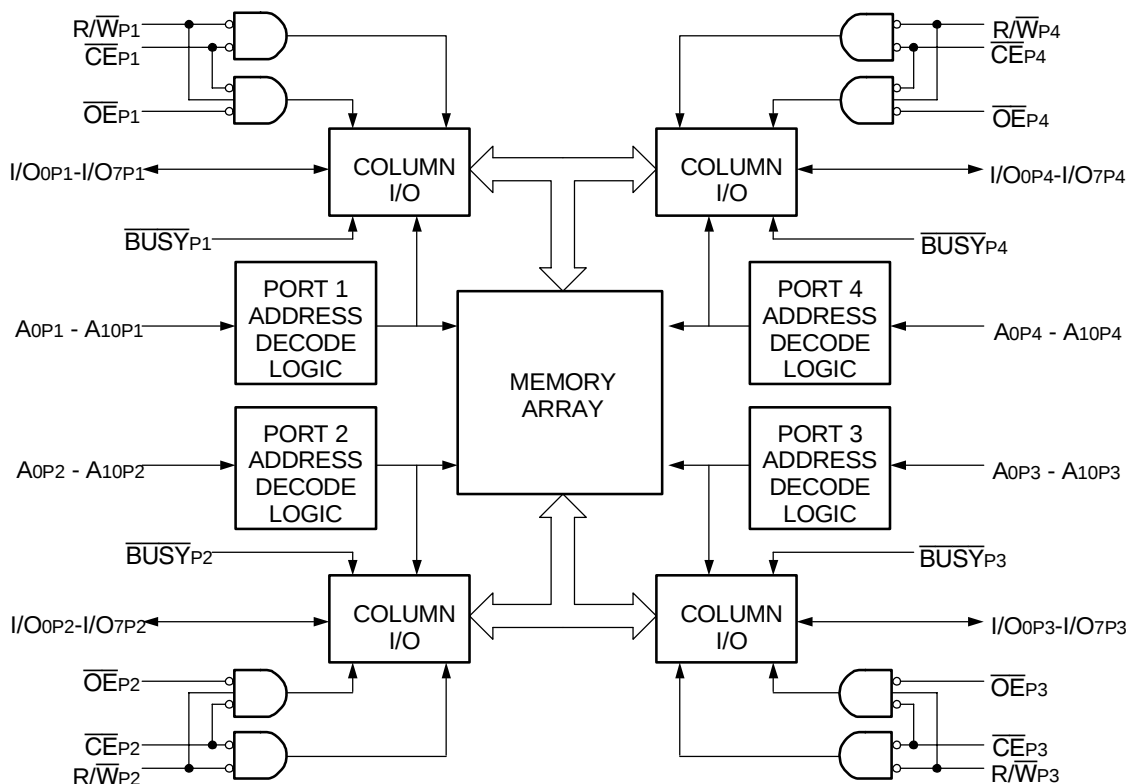
- ◆ **Battery backup operation—2V data retention**
- ◆ **TTL-compatible; single 5V ($\pm 10\%$) power supply**
- ◆ **Available in 120 pin Thin Quad Flatpacks and 108 pin PGA**
- ◆ **Military product compliant to MIL-PRF-38535 QML**
- ◆ **Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds**
- ◆ **Green parts available, see ordering information**

Description

The IDT7052 is a high-speed 2K x 8 FourPort™ Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7052 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those

Functional Block Diagram



2674 drw 01

JUNE 2018

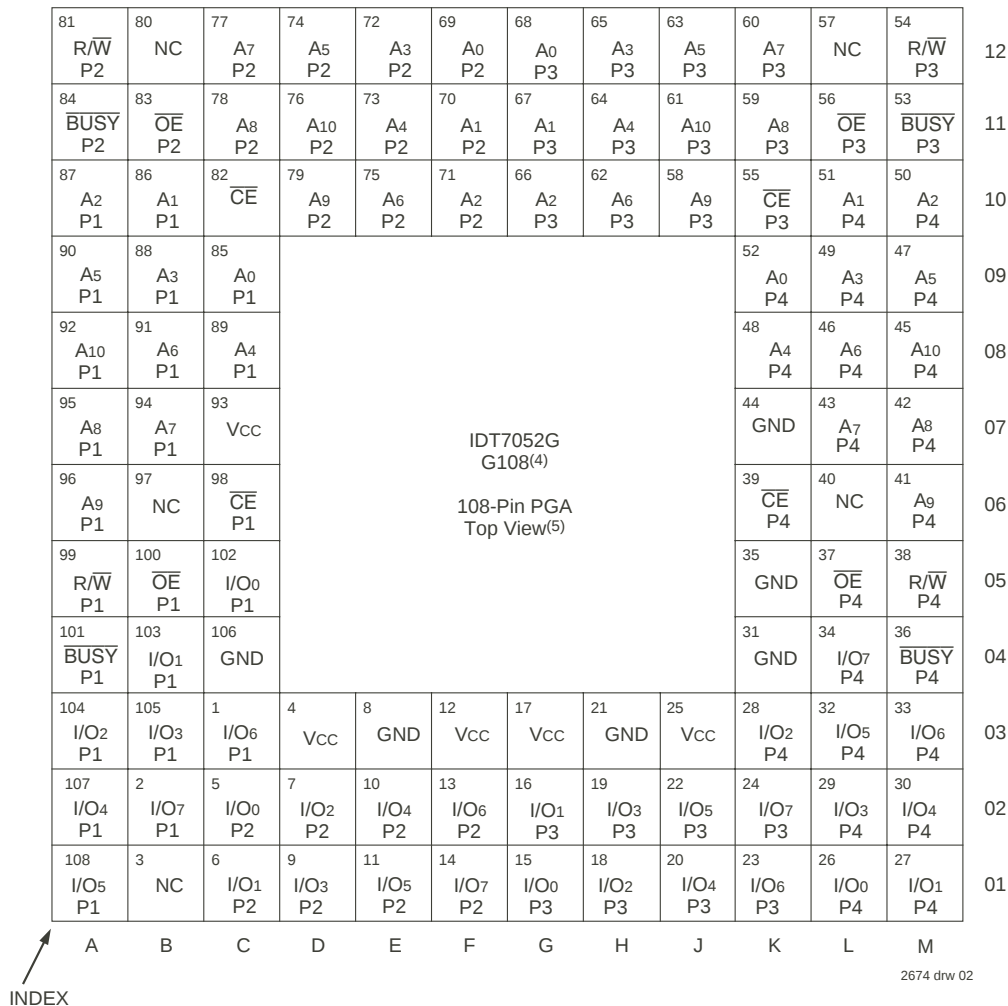
systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7052 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using CMOS high-performance technology, this FourPort SRAM typically operates on only 750mW of power. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50μW from a 2V battery.

The IDT7052 is packaged in a ceramic 108-pin Pin Grid Array (PGA) and 120-pin Thin Quad Flatpack (TQFP). Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

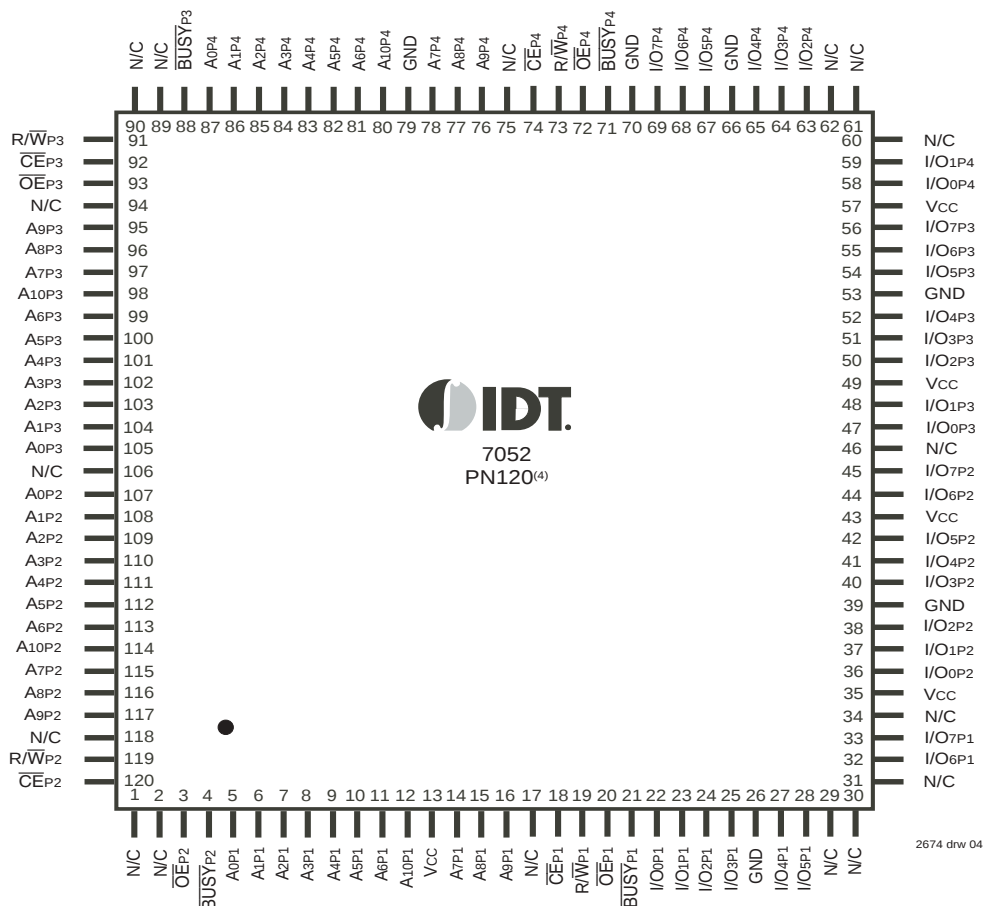
Pin Configurations^(1,2,3)



NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 1.21 in x 1.21 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations^(1,2,3) (con't.)



NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. PN120-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

Pin Configurations^(1,2)

Symbol	Pin Name
A0 P1 - A10 P1	Address Lines - Port 1
A0 P2 - A10 P2	Address Lines - Port 2
A0 P3 - A10 P3	Address Lines - Port 3
A0 P4 - A10 P4	Address Lines - Port 4
I/O0 P1 - I/O7 P1	Data I/O - Port 1
I/O0 P2 - I/O7 P2	Data I/O - Port 2
I/O0 P3 - I/O7 P3	Data I/O - Port 3
I/O0 P4 - I/O7 P4	Data I/O - Port 4
R/W P1	Read/Write - Port 1
R/W P2	Read/Write - Port 2
R/W P3	Read/Write - Port 3
R/W P4	Read/Write - Port 4
GND	Ground
CE P1	Chip Enable - Port 1
CE P2	Chip Enable - Port 2
CE P3	Chip Enable - Port 3
CE P4	Chip Enable - Port 4
OE P1	Output Enable - Port 1
OE P2	Output Enable - Port 2
OE P3	Output Enable - Port 3
OE P4	Output Enable - Port 4
BUSY P1	Write Disable - Port 1
BUSY P2	Write Disable - Port 2
BUSY P3	Write Disable - Port 3
BUSY P4	Write Disable - Port 4
Vcc	Power

NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply

2674 tbl 01

Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz) TQFP only

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	VIN = 0V	9	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

2674 tbl 03

NOTES:

1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-65 to +150	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2674 tbl 02

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2674 tbl 04

NOTE:

1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2674 tbl 05

NOTES:

1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,5) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Condition	Version	7052X20 Com'l Only		7052X25 Com'l, Ind & Military		7052X35 Com'l & Military		Unit	
				Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.		
Icc1	Operating Power Supply Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = 0^{(3)}$	COM'L.	S L	150 150	300 250	150 150	300 250	150 150	300 250	mA
			MIL. & IND.	S L	— —	— —	150 150	360 300	150 150	360 300	
Icc2	Dynamic Operating Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(4)}$	COM'L.	S L	240 210	370 325	225 195	350 305	210 180	335 290	mA
			MIL. & IND.	S L	— —	— —	225 195	400 340	210 180	395 330	
Isb	Standby Current (All Ports - TTL Level Inputs)	$\overline{CE} = V_{IH}$ $f = f_{MAX}^{(4)}$	COM'L.	S L	70 60	95 80	45 40	85 70	40 35	75 60	mA
			MIL. & IND.	S L	— —	— —	45 40	115 85	40 35	110 80	
Isb1	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(3)}$	COM'L.	S L	1.5 0.3	15 1.5	1.5 0.3	15 1.5	1.5 0.3	15 1.5	mA
			MIL. & IND.	S L	— —	— —	1.5 0.3	30 4.5	1.5 0.3	30 4.5	

2674 tbl 06

NOTES:

- 'X' in part number indicates power rating (S or L).
- $V_{CC} = 5V$, $T_A = +25^\circ C$ and are not production tested.
- $f = 0$ means no address or control lines change.
- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- For the case of one port, divide the appropriate current above by four.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	7052S		7052L		Unit
			Min.	Max.	Min.	Max.	
I _L	Input Leakage Current ⁽¹⁾	$V_{CC} = 5.5V, V_{IN} = 0V$ to V_{CC}	—	10	—	5	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}, V_{OUT} = 0V$ to V_{CC}	—	10	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = 4mA	—	0.4	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2674 tbl 07

NOTE:

- At $V_{CC} \leq 2.0V$ input leakages are undefined.

Data Retention Characteristics Over All Temperature Ranges⁽⁴⁾

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

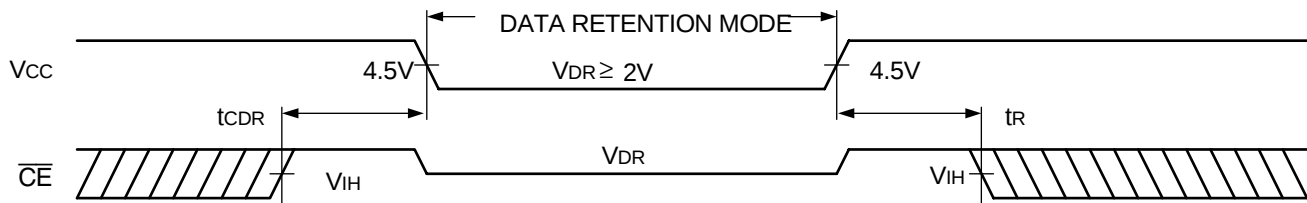
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = 2V$	2.0	—	—	V
I_{CDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	Com'l.	25	600	μA
			Mil. & Ind.	25	1800	
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R^{(3)}$	Operation Recovery Time		$t_{RC}^{(2)}$	—	—	ns

2674 tbl 08a

NOTES:

- $V_{CC} = 2V$, $T_A = +25^\circ C$
- t_{RC} = Read Cycle Time
- This parameter is guaranteed but not production tested.
- Industrial temperature: For other speeds, packages and powers contact your sales office.

Low V_{CC} Data Retention Waveform



2674 drw 05

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2674 tbl 08b

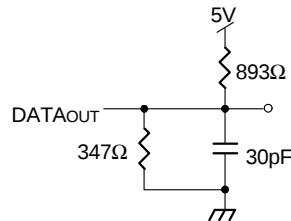


Figure 1. AC Output Test Load

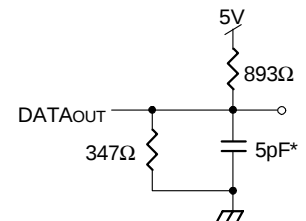


Figure 2. Output Test Load
(for t_{LZ} , t_{HZ} , t_{WZ} , t_{OW})

*Including scope and jig

2674 drw 06

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽³⁾

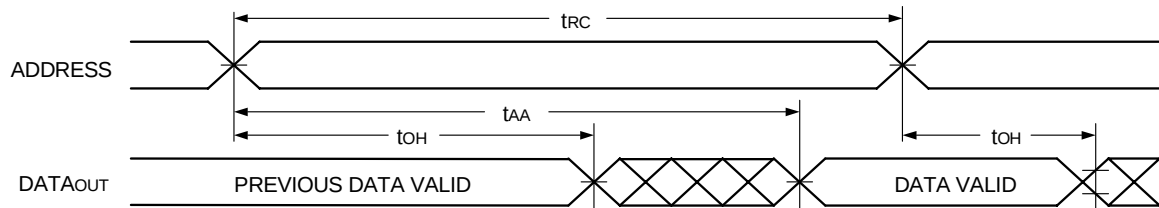
Symbol	Parameter	7052X20 Com'l Only		7052X25 Com'l, Ind & Military		7052X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	ns
t _{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t _{AOE}	Output Enable Access Time	—	10	—	15	—	25	ns
t _{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	5	—	5	—	5	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	12	—	15	—	15	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	20	—	25	—	35	ns

NOTES:

1. Transition is measured 0mV from Low or High-Impedance voltage with the Output Test Load (Figure 2)
2. This parameter is guaranteed by device characterization but is not production tested.
3. 'X' in part number indicates power rating (S or L)

2674 tbl 09

Timing Waveform of Read Cycle No. 1, Any Port⁽¹⁾

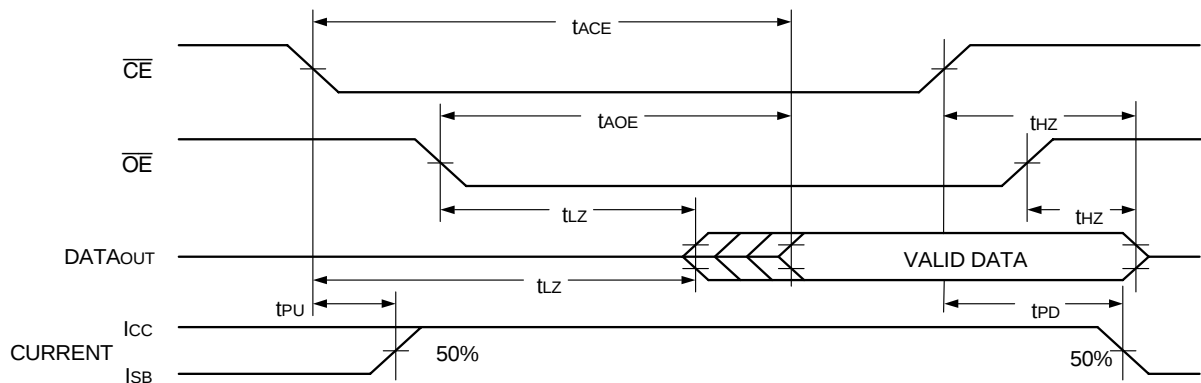


2674 drw 07

NOTE:

1. $R/\overline{W} = V_{IH}$, $\overline{OE} = V_{IL}$ and $\overline{CE} = V_{IL}$.

Timing Waveform of Read Cycle No. 2, Any Port^(1,2)



2674 drw 08

NOTES:

1. $R/\overline{W} = V_{IH}$ for Read Cycles.
2. Addresses valid prior to or coincident with $\overline{CE}$ transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁷⁾

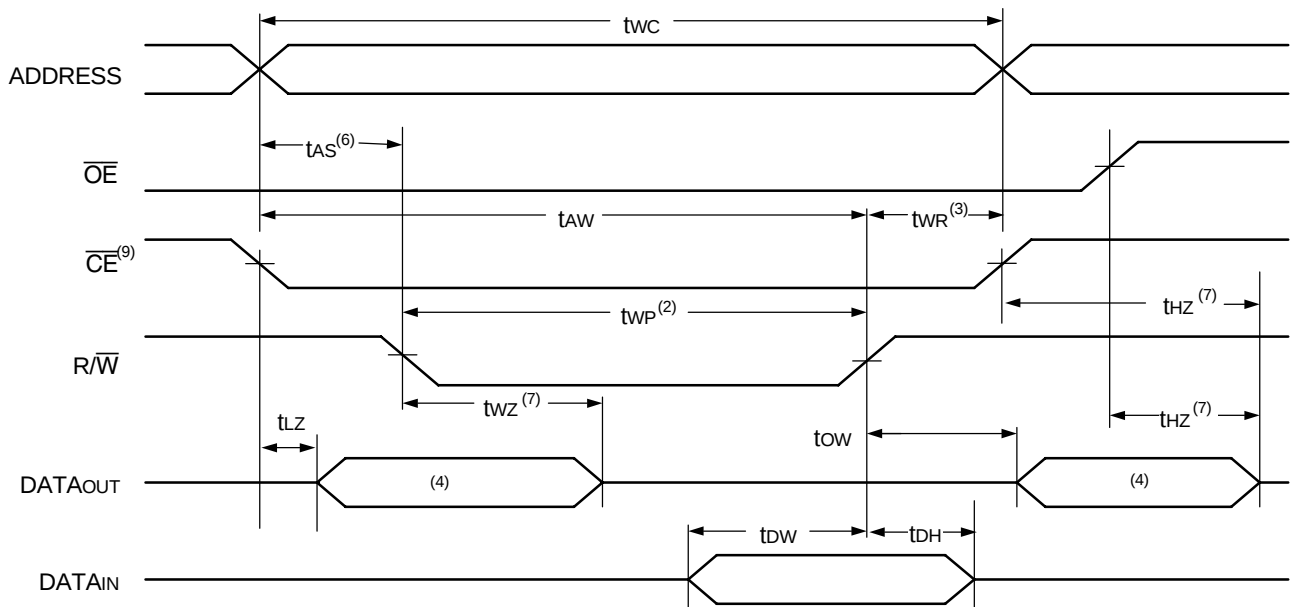
Symbol	Parameter	7052X20 Com'l Only		7052X25 Com'l & Military		7052X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	20	—	25	—	35	—	ns
tEW	Chip Enable to End-of-Write ⁽³⁾	15	—	20	—	30	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width ⁽³⁾	15	—	20	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	20	—	ns
tHZ	Output High-Z Time ^(1,2)	—	15	—	15	—	15	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z ^(1,2)	—	12	—	15	—	15	ns
tOW	Output Active from End-of-Write ^(1,2)	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay ⁽⁴⁾	—	35	—	45	—	55	ns
tWDD	Write Data Valid to Read Data Delay ⁽⁴⁾	—	30	—	35	—	45	ns
BUSY INPUT TIMING								
tWB	Write to $\overline{\text{BUSY}}$ ⁽⁵⁾	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{\text{BUSY}}$ ⁽⁶⁾	15	—	15	—	20	—	ns

2674 tbl 10

NOTES:

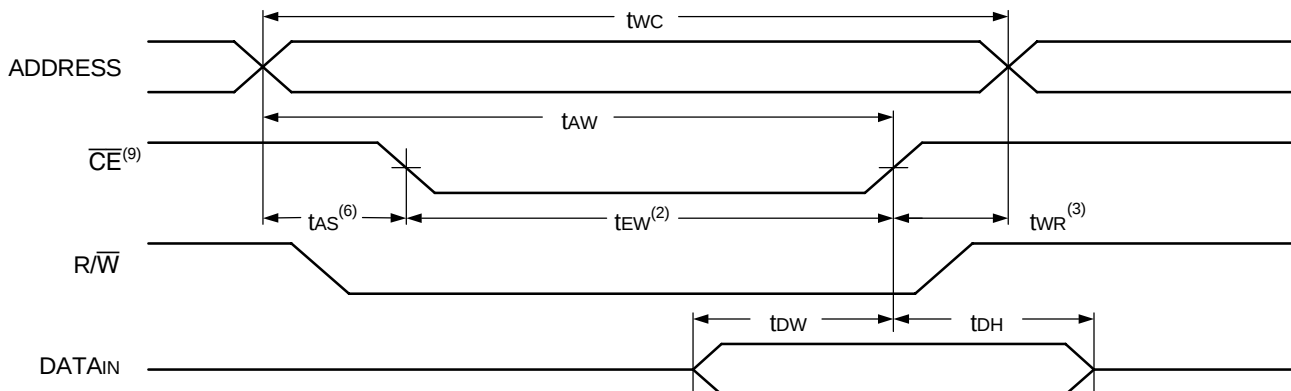
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. If $\overline{\text{OE}} = \text{V}_{\text{IL}}$ during a $\text{R}/\overline{\text{W}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}} = \text{V}_{\text{IH}}$ during an $\text{R}/\overline{\text{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}. Specified for $\overline{\text{OE}} = \text{V}_{\text{IH}}$ (refer to "Timing Waveform of Write Cycle", Note 8).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. To ensure that the write cycle is inhibited on port "A" during contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
6. To ensure that a write cycle is completed on port "A" after contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
7. 'X' in part number indicates power rating.

Timing Waveform of Write Cycle No. 1, R/W Controlled Timing^(5,8)



2674 drw 09

Timing Waveform of Write Cycle No. 2, CE Controlled Timing^(1, 5)

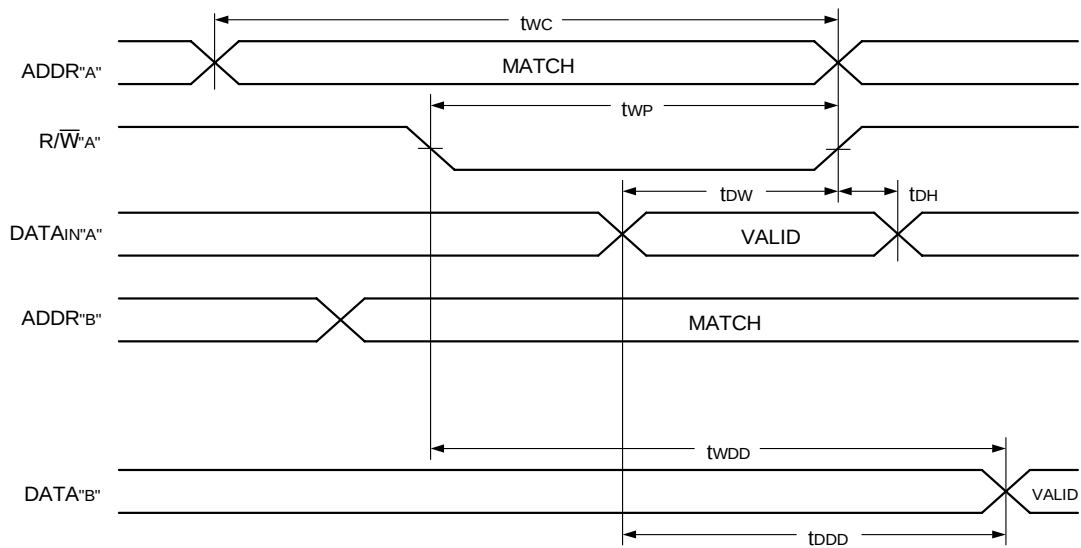


2674 drw 10

NOTES:

1. $R/\overline{W}$ or $\overline{CE} = V_{IH}$ during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE} = V_{IL}$ and a $R/\overline{W} = V_{IL}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $R/\overline{W} = V_{IH}$ to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE} = V_{IL}$ transition occurs simultaneously with or after the $R/\overline{W} = V_{IL}$ transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or $R/\overline{W}$.
7. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed but is not production tested.
8. If $\overline{OE} = V_{IL}$ during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{OW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{OW} . If $\overline{OE} = V_{IH}$ during an $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

Timing Waveform of Write with Port-to-Port Read^(1,2,3)

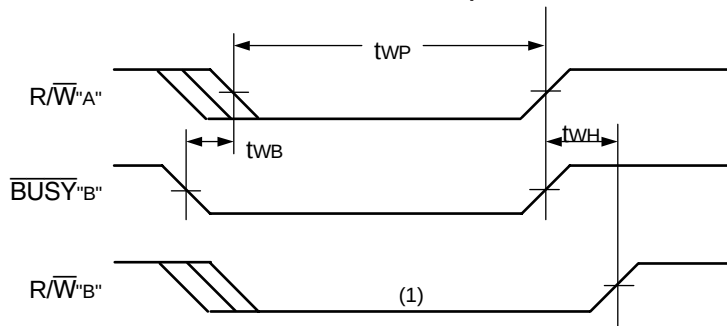


2674 drw 11

NOTES:

1. Assume $\overline{\text{BUSY}}$ input = V_{IH} and $\overline{\text{CE}} = V_{IL}$ for the writing port.
2. $\overline{\text{OE}} = V_{IL}$ for the reading ports.
3. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

Timing Waveform of Write with **BUSY** Input



2674 drw 12

NOTE:

1. $\overline{\text{BUSY}}$ is asserted on Port "B" blocking $\overline{\text{R/W}}\text{'B'}$ until $\overline{\text{BUSY}}\text{'B'}$ goes HIGH.

Functional Description

The IDT7052 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{\text{CE}} = V_{IH}$). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{\text{OE}}$). In the read mode, the port's $\overline{\text{OE}}$ turns on the output drivers when set LOW. READ/ WRITE conditions are illustrated in the table below.

Truth Table I – Read/Write Control⁽³⁾

Any Port ⁽¹⁾				Function
R/W	$\overline{\text{CE}}$	$\overline{\text{OE}}$	D0-7	
X	H	X	Z	Port Deselected: Power-Down
X	H	X	Z	$\overline{\text{CE}}\text{P1}=\overline{\text{CE}}\text{P2}=\overline{\text{CE}}\text{P3}=\overline{\text{CE}}\text{P4}=V_{IH}$ Power Down Mode ISB or ISB1
L	L	X	DATAin	Data on port written into memory ⁽²⁾
H	L	L	DATAout	Data in memory output on port
X	X	H	Z	Outputs Disabled

2674 tbl 11

NOTES:

1. "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care, "Z" = High Impedance
2. If $\overline{\text{BUSY}} = V_{IL}$, write is blocked.
3. For valid write operation, no more than one port can write to the same address location at the same time.

Ordering Information

XXXX	A	999	A	A	A	A		
Device Type	Power	Speed	Package		Process/ Temperature Range			
							Blank 8	Tube or Tray Tape and Reel
							Blank J ⁽¹⁾	Commercial (0°C to +70°C) Industrial (-40°C to +85°C) Military (-55°C to +125°C) Compliant to MIL-PRF-38535 QML
							B	
							G ⁽²⁾	Green
							G	108-Pin Pin Grid Array (G108)
							PF	120-Pin Thin Quad Plastic Flatpack (PN120)
							20	Commercial Only Commercial, Industrial & Military Commercial & Military
							25	
							35	
							L	Low Power
							S	Standard Power
							7052	16K (2K x 8) FourPort RAM

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NOTES:

1. Industrial temperature range is available. For specific speeds, packages and powers contact your sales office.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

01/18/99:	Initiated datasheet document history Converted to new format Cosmetic typographical corrections Added additional notes to pin configurations
06/04/99:	Changed drawing format Page 1 Corrected DSC number
11/10/99:	Replaced IDT logo
11/18/99:	Page 10 Fixed typo in caption for $\overline{\text{BUSY}}$ Input waveform
05/23/00:	Page 4 Increased storage temperature parameter Clarified TA parameter Page 5 DC Electrical parameters—changed wording from "open" to "disabled" Changed $\pm 200\text{mV}$ to 0mV in notes
10/22/01:	Pages 2 & 3 Added date revision for pin configurations Page 5, 7 & 8 Added Industrial temp to column heading for 25ns speed to DC & AC Electrical Characteristics Page 11 Added Industrial temp offering to 25ns ordering information Page 4, 5, 7 & 8 Removed Industrial temp footnote from all tables Page 1 & 11 Replace ™ logo with ® logo
07/24/06:	Page 1 Added green availability to features Page 11 Added green indicator to ordering information
01/19/09:	Page 11 Removed "IDT" from orderable part number
02/05/15:	Page 2 Removed IDT in reference to fabrication Page 2, 3 & 11 The package codes G108-1 & PN120-1 changed to G108 & PN120 respectively to match standard package codes Page 11 Added Tape and Reel to Ordering Information Page 1 & 3 Removed 132-pin PQF offering from the Features & the pin configuration Page 11 Removed the 132-pin PQF package from the Ordering Information

Datasheet Document History (con't)

07/08/16:	Page 3	Changed diagram for the PN120 pin configuration by rotating package pin labels and pin numbers 90 degrees counter clockwise to reflect pin 1 orientation and added pin 1 dot at pin 1 Added the IDT logo to the PN120 pin configurations and changed the text to be in alignment with new diagram marking specs and removed the date revision indicator from all pin configurations
06/07/18:		Updated footnote references for PN120 pin configuration by removing footnote 4 & 5 Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018



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