



Integrated Device Technology, Inc.

HIGH-SPEED 1K x 8 FourPort™ STATIC RAM

IDT7050S
IDT7050L

FEATURES:

- High-speed access
 - Military: 30/35/45ns (max.)
 - Commercial: 25/30/35/45ns (max.)
- Low-power operation
 - IDT7050S
 - Active: 750mW (typ.)
 - Standby: 10mW (typ.)
 - IDT7050L
 - Active: 750mW (typ.)
 - Standby: 1.5mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{\text{BUSY}}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V ($\pm 10\%$) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available, tested to military electrical specification

DESCRIPTION:

The IDT7050 is a high-speed 1K x 8 FourPort static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort static RAM offers increased system performance in multiprocessor systems

that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

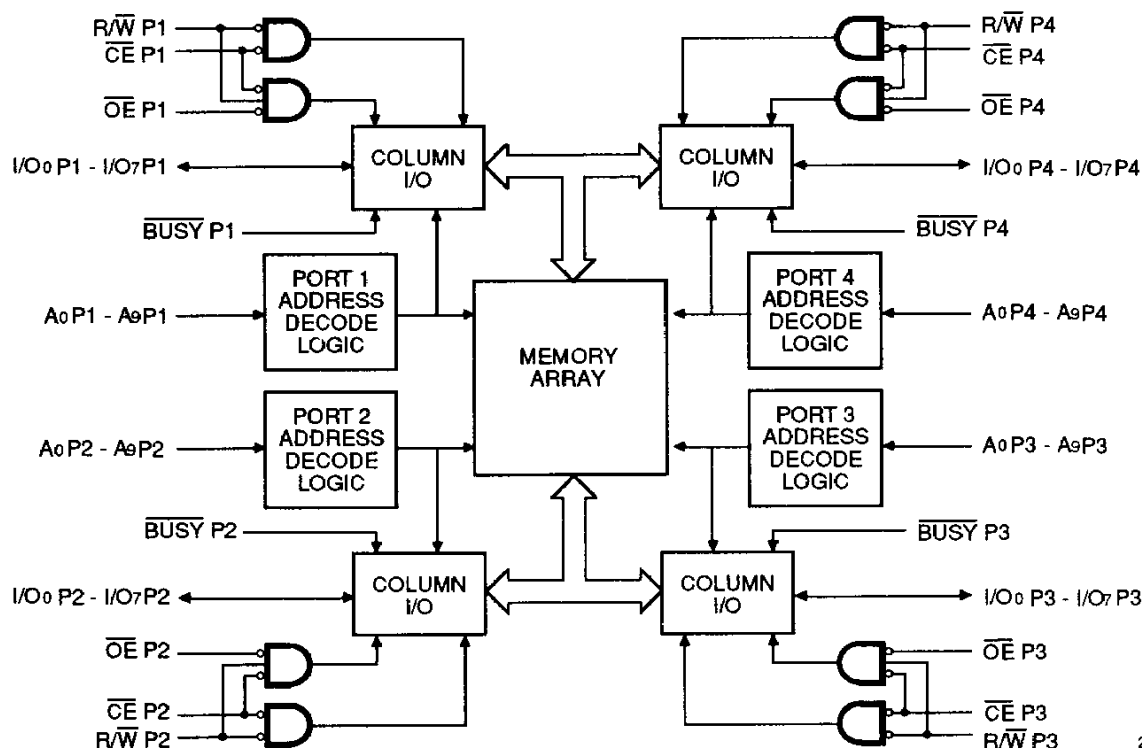
The IDT7050 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7050 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{\text{CE}}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM typically operates on only 750mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50μW from a 2V battery.

The IDT7050 is packaged in a ceramic 108-pin PGA and a plastic 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2698 drw 01

FourPort is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

81 R/W P2	80 NC	77 A7 P2	74 A5 P2	72 A3 P2	69 A0 P2	68 A0 P3	65 A3 P3	63 A5 P3	60 A7 P3	57 NC	54 R/W P3	12
84 BUSY P2	83 OE P2	78 A8 P2	76 NC	73 A4 P2	70 A1 P2	67 A1 P3	64 A4 P3	61 NC	59 A8 P3	56 OE P3	53 BUSY P3	11
87 A2 P1	86 A1 P1	82 CE P2	79 A9 P2	75 A6 P2	71 A2 P2	66 A2 P3	62 A6 P3	58 A9 P3	55 CE P3	51 A1 P4	50 A2 P4	10
90 A5 P1	88 A3 P1	85 A0 P1	IDT7050 G108-1 ^(1,2,3) TOP VIEW						52 A0 P4	49 A3 P4	47 A5 P4	09
92 NC	91 A6 P1	89 A4 P1							48 A4 P4	46 A6 P4	45 NC	08
95 A6 P1	94 A7 P1	93 VCC							44 GND	43 A7 P4	42 A8 P4	07
96 A9 P1	97 NC	98 CE P1							39 CE P4	40 NC	41 A9 P4	06
99 R/W P1	100 OE P1	102 I/O0 P1							35 GND	37 OE P4	38 R/W P4	05
101 BUSY P1	103 I/O1 P1	106 GND							31 GND	34 I/O7 P4	36 BUSY P4	04
104 I/O2 P1	105 I/O3 P1	1 I/O6 P1	4 VCC	8 GND	12 VCC	17 VCC	21 GND	25 VCC	28 I/O2 P4	32 I/O5 P4	33 I/O6 P4	03
107 I/O4 P1	2 I/O7 P1	5 I/O0 P2	7 I/O2 P2	10 I/O4 P2	13 I/O6 P2	16 I/O1 P3	19 I/O3 P3	22 I/O5 P3	24 I/O7 P3	29 I/O3 P4	30 I/O4 P4	02
108 I/O5 P1	3 NC	6 I/O1 P2	9 I/O3 P2	11 I/O5 P2	14 I/O7 P2	15 I/O0 P3	18 I/O2 P3	20 I/O4 P3	23 I/O6 P3	26 I/O0 P4	27 I/O1 P4	01
A	B	C	D	E	F	G	H	J	K	L	M	

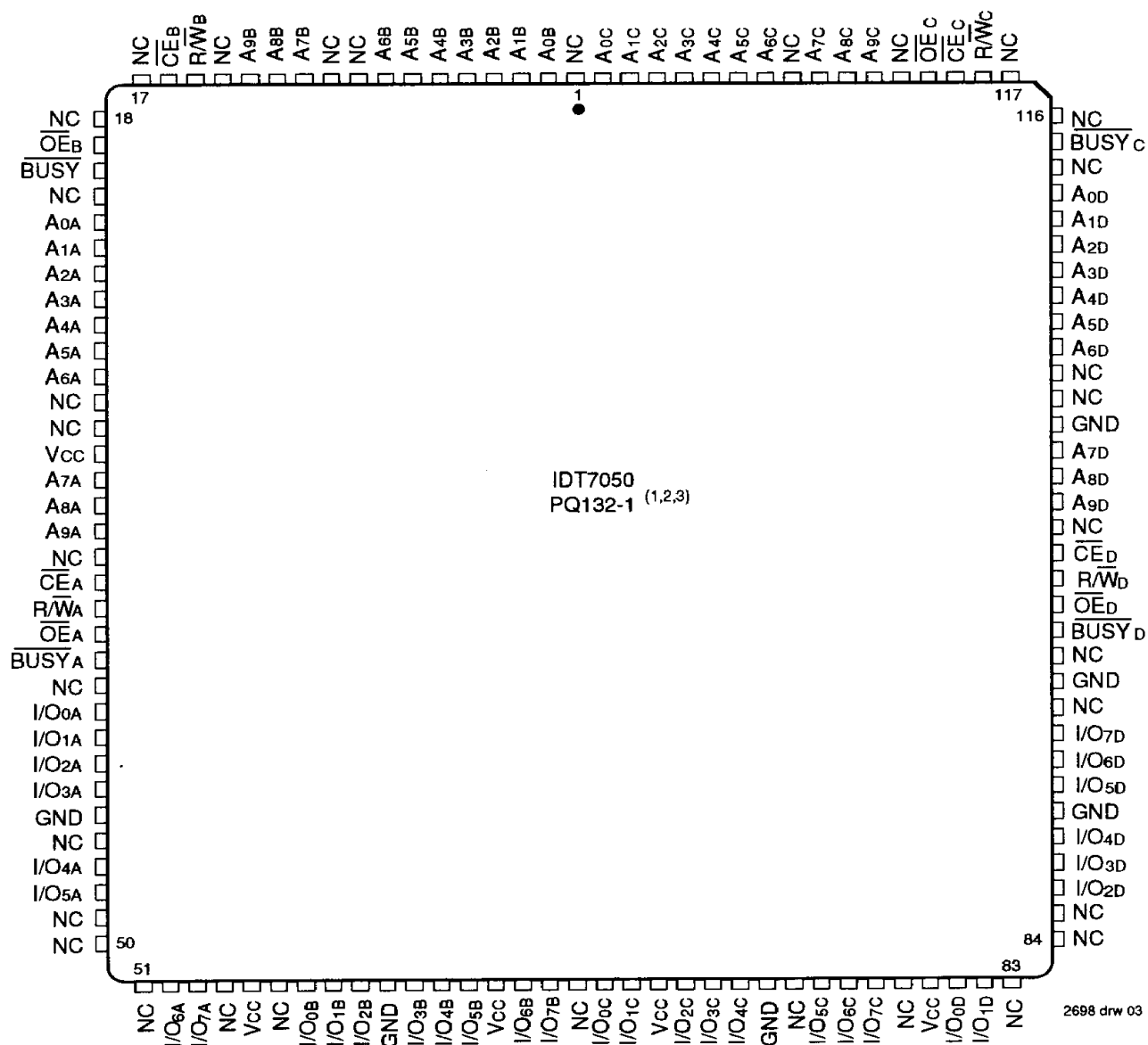
Pin 1
Designator

NOTES:

1. All VCC pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no - connect pin.

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2698 drw 02



NOTES:

1. All VCC pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no - connect pin.

PIN CONFIGURATIONS

Symbol	Pin Name
A0 P1 – A9 P1	Address Lines – Port 1
A0 P2 – A9 P2	Address Lines – Port 2
A0 P3 – A9 P3	Address Lines – Port 3
A0 P4 – A9 P4	Address Lines – Port 4
I/O0 P1 – I/O7 P1	Data I/O – Port 1
I/O0 P2 – I/O7 P2	Data I/O – Port 2
I/O0 P3 – I/O7 P3	Data I/O – Port 3
I/O0 P4 – I/O7 P4	Data I/O – Port 4
R/W P1	Read/Write – Port 1
R/W P2	Read/Write – Port 2
R/W P3	Read/Write – Port 3
R/W P4	Read/Write – Port 4
GND	Ground
CE P1	Chip Enable – Port 1
CE P2	Chip Enable – Port 2
CE P3	Chip Enable – Port 3
CE P4	Chip Enable – Port 4
OE P1	Output Enable – Port 1
OE P2	Output Enable – Port 2
OE P3	Output Enable – Port 3
OE P4	Output Enable – Port 4
BUSY P1	Write Disable – Port 1
BUSY P2	Write Disable – Port 2
BUSY P3	Write Disable – Port 3
BUSY P4	Write Disable – Port 4
Vcc	Power

2698 tbl 01

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:

2698 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOU = 0V	11	pF

NOTE:

2698 tbl 03

- This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2698 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

2698 tbl 05

- VIL (min.) = -3.0V for pulse width less than 20ns.
- VTERM must not exceed Vcc + 0.5V.

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	IDT7050S		IDT7050L		Unit
			Min.	Max.	Min.	Max.	
$ I_{LI} $	Input Leakage Current ⁽⁷⁾	$V_{CC} = 5.5V, V_{IN} = 0V \text{ to } V_{CC}$	—	10	—	5	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE} = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	—	10	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = 4mA$	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	2.4	—	V

2698 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE^(1, 2, 6) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Condition	Version	IDT7050x25 ⁽³⁾		IDT7050x30		IDT7050x35		IDT7050x45		Unit	
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
Icc1	Operating Power Supply Current (All Ports Active)	$\overline{CE} \leq V_{IL}$ Outputs Open $f = 0^{(4)}$	MIL.	S	—	—	150	360	150	360	150	360	mA
				L	—	—	150	300	150	300	150	300	
			COM'L.	S	150	300	150	300	150	300	150	300	
				L	150	250	150	250	150	250	150	250	
Icc2	Dynamic Operating Current (All Ports Active)	$\overline{CE} \leq V_{IL}$ Outputs Open $f = f_{MAX}^{(5)}$	MIL.	S	—	—	220	400	210	395	195	390	mA
				L	—	—	190	335	180	330	170	325	
			COM'L.	S	225	350	220	340	210	335	195	330	
				L	195	305	190	295	180	290	170	285	
ISB	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE} \geq V_{IH}$ $f = f_{MAX}^{(5)}$	MIL.	S	—	—	45	115	40	110	35	105	mA
				L	—	—	40	85	35	80	30	75	
			COM'L.	S	60	85	45	80	40	75	35	70	
				L	50	70	40	65	35	60	30	55	
ISB1	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(4)}$	MIL.	S	—	—	1.5	30	1.5	30	1.5	30	mA
				L	—	—	.3	4.5	.3	4.5	.3	4.5	
			COM'L.	S	1.5	15	1.5	15	1.5	15	1.5	15	
				L	.3	1.5	.3	1.5	.3	1.5	.3	1.5	

NOTES:

2698 tbl 07

- "X" in part number indicates power rating (S or L).
- $V_{CC} = 5V, T_A = +25^\circ C$ for Typ.
- $0^\circ C$ to $+70^\circ C$ temperature range only.
- $f = 0$ means no address or control lines change.
- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
- For the case of one port, divide the appropriate current by four.
- At $V_{CC} \leq 2.0V$ input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V$

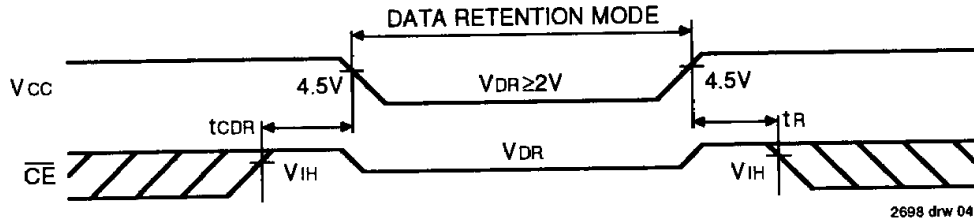
Symbol	Parameter	Test Condition		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = 2V$		2.0	—	—	V
ICCDR	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	25	1800	μA
			COM'L.	—	25	600	
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time			0	—	—	ns
$t_{R}^{(3)}$	Operation Recovery Time			$t_{RC}^{(2)}$	—	—	ns

NOTES:

2698 tbl 08

- $V_{CC} = 2V, T_A = +25^\circ C$
- t_{RC} = Read Cycle Time
- This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2698 tbl 09

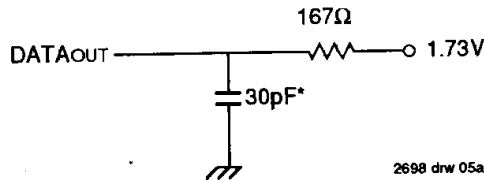


Figure 1. Equivalent Output Load

*Including scope and jig

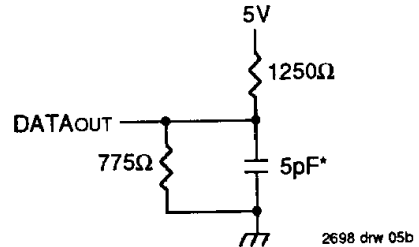


Figure 2. Output Load
(for tLZ, tHZ, tWZ, tOW)

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

OPERATING TEMPERATURE AND SUPPLY VOLTAGE

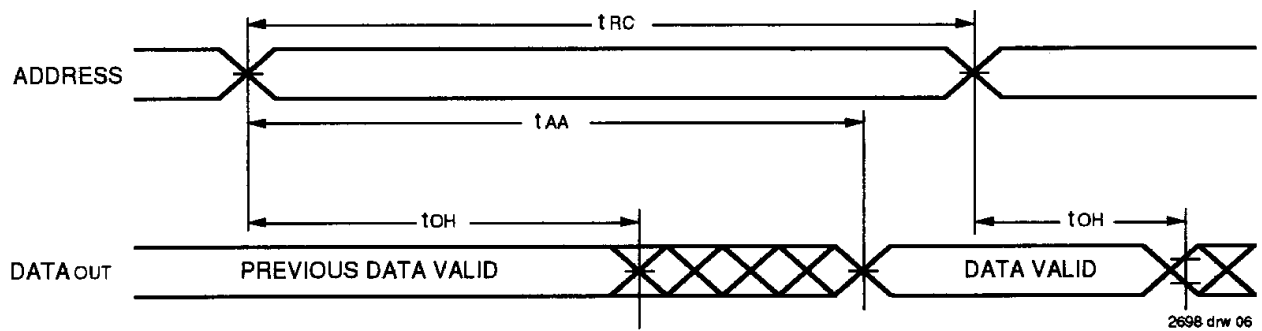
Symbol	Parameter	IDT7050S25 ^(1,3) IDT7050L25 ^(1,3)		IDT7050S30 IDT7050L30		IDT7050S35 IDT7050L35		IDT7050S45 IDT7050L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time ^(1, 2)	3	—	3	—	5	—	5	—	ns
tHZ	Output High Z Time ^(1, 2)	—	15	—	15	—	15	—	20	ns
tPU	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time ⁽²⁾	—	20	—	30	—	50	—	50	ns

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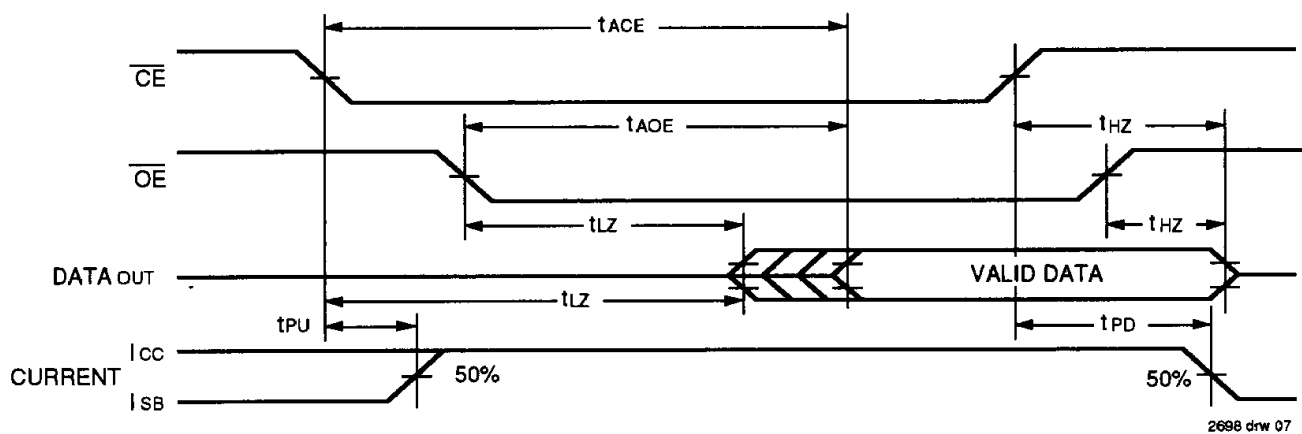
NOTES:

1. Transition is measured $\pm 500\text{mV}$ from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT^(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT^(1, 3)



NOTES:

1. R/W is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

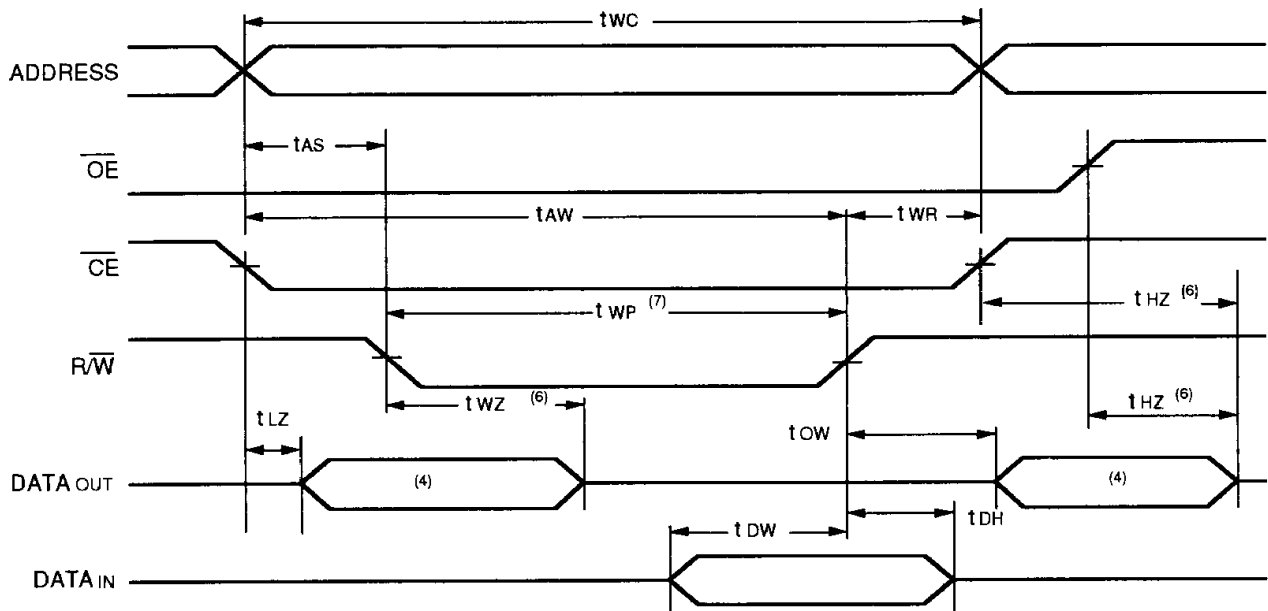
Symbol	Parameter	IDT7050S25 ⁽⁷⁾ IDT7050L25 ⁽⁷⁾		IDT7050S30 IDT7050L30		IDT7050S35 IDT7050L35		IDT7050S45 IDT7050L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width ⁽³⁾	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	5	—	ns
tdW	Data Valid to End of Write	15	—	15	—	20	—	20	—	ns
thZ	Output High Z Time ^(1, 2)	—	15	—	15	—	15	—	20	ns
tdH	Data Hold Time	0	—	0	—	0	—	0	—	ns
twZ	Write Enabled to Output in High Z ^(1, 2)	—	15	—	15	—	15	—	20	ns
tOW	Output Active from End of Write ^(1, 2)	0	—	0	—	0	—	0	—	ns
twDD	Write Pulse to Data Delay ⁽⁴⁾	—	45	—	50	—	55	—	65	ns
tdDD	Write Data Valid to Read Data Delay ⁽⁴⁾	—	35	—	40	—	45	—	55	ns
BUSY INPUT TIMING										
twB	Write to BUSY ⁽⁵⁾	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁶⁾	15	—	20	—	20	—	20	—	ns

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NOTES:

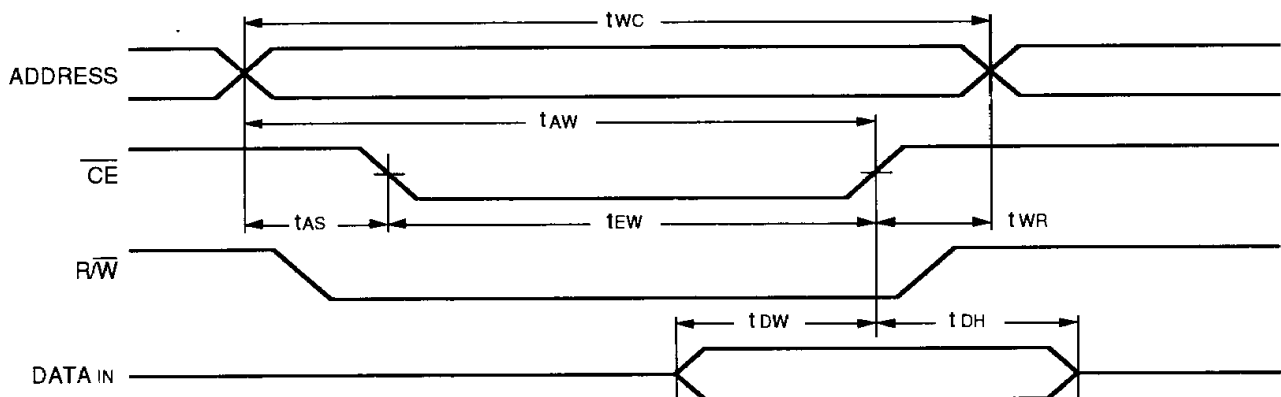
1. Transition is measured $\pm 500\text{mV}$ from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for OE at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{R/\overline{W}}$ CONTROLLED TIMING^(1, 2, 3, 7)



2698 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING^(1, 2, 3, 5)

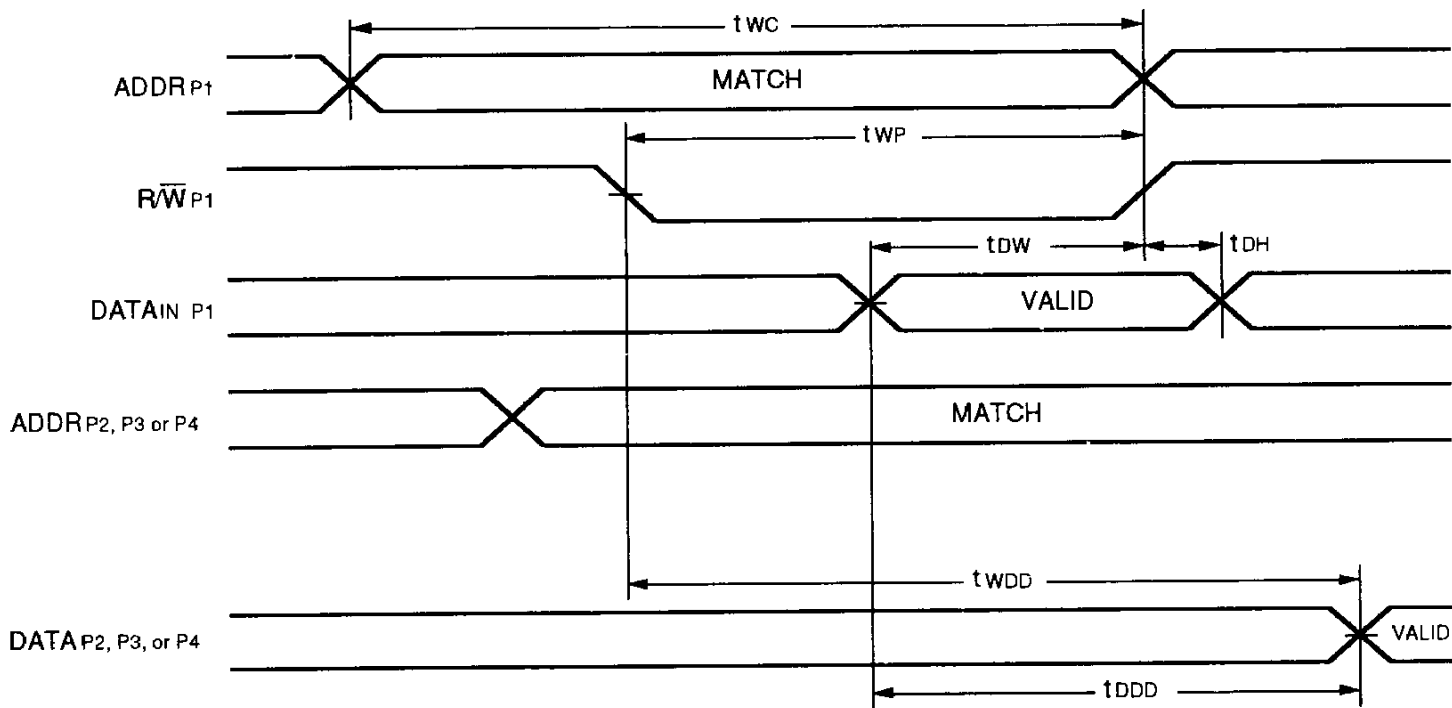


2698 drw 09

NOTES:

1. $\overline{R/\overline{W}}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{ew} or t_{wp}) of a low $\overline{CE}$ and a low $\overline{R/\overline{W}}$.
3. t_{wr} is measured from the earlier of $\overline{CE}$ or $\overline{R/\overline{W}}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the $\overline{R/\overline{W}}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a $\overline{R/\overline{W}}$ controlled write cycle, the write pulse width must be the larger of t_{wp} or ($t_{wz} + t_{dw}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{dw} . If $\overline{OE}$ is high during an $\overline{R/\overline{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{wp} .

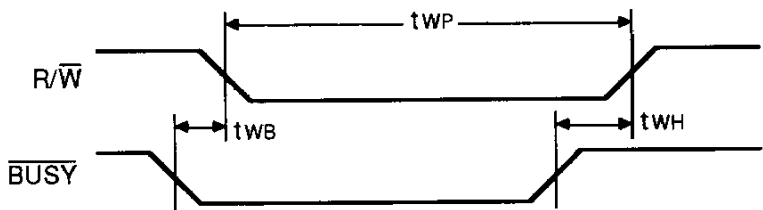
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY^(1, 2, 3)



2698 drw 10

- NOTES:
- 1. Assume $\overline{\text{BUSY}}$ input at HI and $\overline{\text{CE}}$ at LO for the writing port.
 - 2. Write cycle parameters should be adhered to in order to ensure proper writing.
 - 3. Device is continuously enabled for any of the reading ports which has its $\overline{\text{OE}}$ at LO.

TIMING WAVEFORM OF WRITE WITH $\overline{\text{BUSY}}$ INPUT



2698 drw 11

FUNCTIONAL DESCRIPTION

The IDT7050 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{\text{CE}}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{\text{OE}}$). In the read mode, the port's $\overline{\text{OE}}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

TABLE I – READ/WRITE CONTROL

Any Port ⁽¹⁾				Function
R/W	$\overline{\text{CE}}$	$\overline{\text{OE}}$	D0-7	
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{\text{CE}}_{\text{P1}} = \overline{\text{CE}}_{\text{P2}} = \overline{\text{CE}}_{\text{P3}} = \overline{\text{CE}}_{\text{P4}} = \text{H}$ Power Down Mode, ISB1 or ISB
L	L	X	DATA _{IN}	Data on port written into memory ^(2, 3)
H	L	L	DATA _{OUT}	Data in memory output on port
X	X	H	Z	High impedance outputs

- NOTES:
- 1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
 - 2. If $\overline{\text{BUSY}} = \text{LOW}$, data is not written.
 - 3. For valid write operation, no more than one port can write to the same address location at the same time.

2698 tbl 12