Integrated Device Technology, Inc.

HIGH-SPEED CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74AHCT299

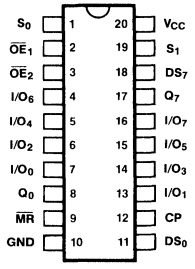
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 8-input universal shift register
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT299 is an 8-bit universal shift register built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0-Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS



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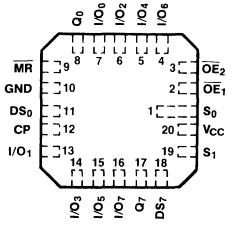
DIP
TOP VIEW



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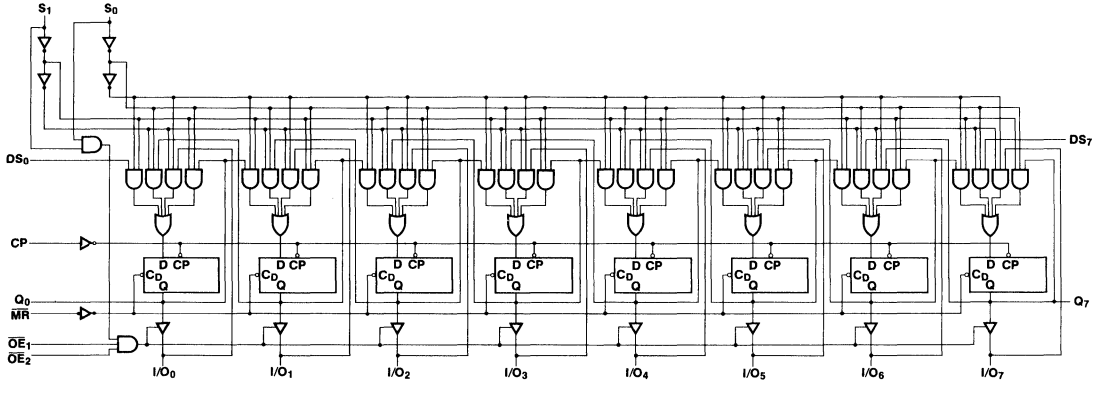
LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -200µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND One Bit Toggling at f_i = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.65	3.4	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND Eight Bits Toggling at f_i = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			V_{IN} = 3.4V V_{IN} = GND	—	2.88	9.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Rising Edge)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌠	Parallel Load; $I/O_N \rightarrow Q_N$
H	L	H	⌠	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌠	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50 pf R_L = 500 Ω	9.0	3.5	13.0	—	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_N		8.0	4.0	15.0	—	15.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		9.0	4.5	13.0	—	15.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_N		9.0	6.5	15.0	—	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ to I/O_N		10.0	3.5	14.0	—	18.0	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ to I/O_N		7.5	2.0	10.0	—	12.0	ns
t_S	Setup Time HIGH or LOW S_0 or S_1 to CP		4.0	8.5	—	8.5	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	1.0	—	1.0	—	ns
t_S	Setup Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		1.5	5.5	—	5.5	—	ns
t_H	Hold Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		0	3.0	—	4.0	—	ns
t_W	CP Pulse Width HIGH or LOW		8.0	8.0	—	8.0	—	ns
t_W	$\overline{MR}$ Pulse Width Low		8.0	8.0	—	8.0	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		8.0	8.0	—	8.0	—	ns