Integrated Device Technology Inc

HIGH-SPEED CMOS UP/DOWN BINARY COUNTER

IDT54/74AHCT193

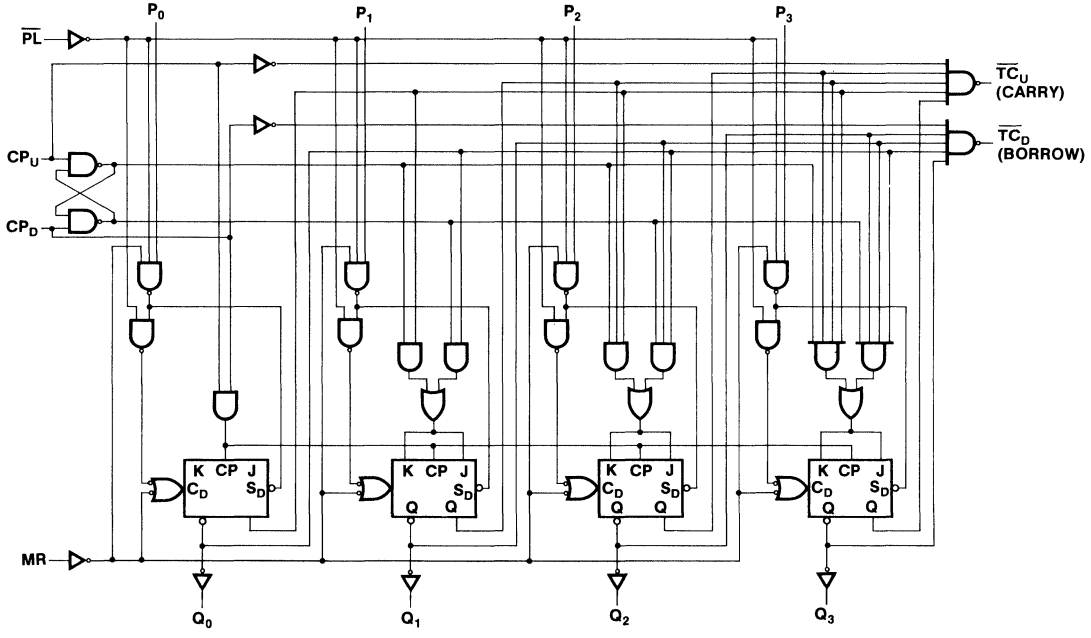
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μ max.)
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT193 is an up/down modulo-16 binary counter built using advanced CEMOS™, a dual metal CMOS technology. Separate Count-up and Count-down Clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count-up and Terminal Count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset ($\overline{MR}$) inputs asynchronously override the clocks.

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT193-001

5

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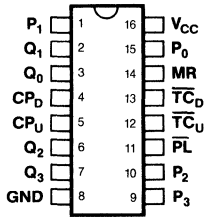
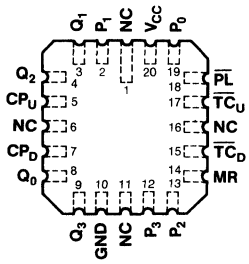
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = –55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	–5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		–60	–100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –150µA	V_{HC}	V_{CC}	—	
			I_{OH} = –1.0mA MIL.	2.4	4.3	—	
			I_{OH} = –2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP_U} = f_{CP_D} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ MR = V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ MR = V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	—	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	1.1	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP} + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Count Clock or Load Clock Frequency
   f_i = P_{0-3} Input Frequency (Load)
   N_i = Number of P_{0-3} Inputs at f_i (Load)
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P_{0-3}	Parallel Data Inputs
Q_{0-3}	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↓	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN..	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	C_L = 50pF R_L = 500Ω	—	4.0	16.0	4.0	19.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		—	4.0	17.0	4.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		—	4.0	17.0	4.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		—	6.0	28.0	6.0	31.0	ns
t_{PHL}	Propagation Delay MR to Q_n		—	6.0	28.0	6.0	31.0	ns
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$		—	6.0	28.0	6.0	31.0	ns
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$		—	6.0	28.0	6.0	31.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$		—	6.0	28.0	6.0	31.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$		—	4.0	17.0	4.0	20.0	ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$		—	20.0	—	25.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$		—	5.0	—	5.0	—	ns
$t_W(L)$	$\overline{PL}$ Pulse Width, LOW		—	20.0	—	25.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW		—	15.0	—	20.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW (Change of Direction)		—	15.0	—	20.0	—	ns
$t_W(H)$	MR Pulse Width, HIGH		—	10.0	—	10.0	—	ns
t_{REC}	Recovery Time $\overline{PL}$ to CP_U or CP_D		—	15.0	—	20.0	—	ns
t_{REC}	Recovery Time MR to CP_U or CP_D		—	15.0	—	20.0	—	ns